via6522\_x12

© 2019-2022 Robert Finch

# Overview

The via6522 is a versatile interface adapter 12-bit peripheral core that is register compatible with a 6522. It may also be configured to operate as an eight-bit peripheral.

# Features

* 12-bit port data width
* 3 24-bit Timers
* 1 12-bit shift register

# Differences From the Stock 6522

The default data width is twelve bits.

There is a third timer register driven by its own independent clock. There are six additional registers to support the third timer. Timer 3 counts up.

The reset input (rst\_i) is active high.

The IRQ output (irq\_o) is not open collector and is active high.

There is only a single active high circuit select (cs\_i).

# Registers

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Reg | Bits | Moniker |  | Comment |
| 0 | 12 | PB | Port B I/O |  |
| 1 | 12 | PA | Port A I/O | handshaking |
| 2 | 12 | PBDDR | Port B data direction |  |
| 3 | 12 | PADDR | Port A data direction |  |
| 4 | 12 | T1CL | Timer 1 count low |  |
| 5 | 12 | T1CH | Timer 1 count high |  |
| 6 | 12 | T1LL | Timer 1 latch low |  |
| 7 | 12 | T1LH | Timer 1 latch high |  |
| 8 | 12 | T2CL | Timer 2 count low |  |
| 9 | 12 | T2CH | Timer 2 count high |  |
| 10 | 12 | SR | Shift register |  |
| 11 | 12 | ACR | Auxiliary control register |  |
| 12 | 12 | PCR | Peripheral control register |  |
| 13 | 12 | IFR | Interrupt flag register |  |
| 14 | 12 | IER | Interrupt enable register |  |
| 15 | 12 | PA | Port A I/O | no handshaking |
| 16 | 12 | T3CL | Timer 3 count low |  |
| 17 | 12 | T3CH | Timer 3 count high |  |
| 18 | 12 | T3LL | Timer 3 latch low |  |
| 19 | 12 | T3LH | Timer 3 latch high |  |
| 20 | 12 | T3CMPL | Timer 3 compare low |  |
| 21 | 12 | T3CMPH | Timer 3 compare high |  |

## PB (Reg 0)

Operates in the same manner as the 6522 port B but is 12-bits wide rather than 8-bits. If port B input latching is enabled, then input data on port B is latched by an active transition of the selected handshaking signal. Otherwise input data is reflected directly by reading the port register.

## PA (Reg 1)

Operates in the same manner as the 6522 port A but is 12-bits wide rather than 8-bits. If port A input latching is enabled, then input data on port A is latched by an active transition of the selected handshaking signal. Otherwise input data is reflected directly by reading the port register.

## PBDDR (Reg 2)

Operates in the same manner as the 6522 port B ddr but is 12-bits wide rather than 8-bits. Each bit that is set in this register set the corresponding port B I/O to an output. Each bit that is clear in this register sets the port B I/O to an input. The default value in this register at reset is zero, making all port B I/O’s inputs.

## PADDR (Reg 3)

Operates in the same manner as the 6522 port A ddr but is 12-bits wide rather than 8-bits. Each bit that is set in this register set the corresponding port A I/O to an output. Each bit that is clear in this register sets the port A I/O to an input. The default value in this register at reset is zero, making all port A I/O’s inputs.

## T1CL (Reg 4)

Similar function to the reg 4 of the 6522. Provides read access to the low order 12-bits of timer 1. Acts as a latch for the low 12-bits of the value to be loaded into the timer.

## T1CH (Reg 5)

Similar in function to register 5 of the 6522. When the timer is in 24-bit mode writing this register transfers bit 0 to 11 of the timer 1 latch to bits 0 to 11 of the timer and transfers input data bits 0 to 11 to counter bits 12 to 23 of the timer.

## T1LL (Reg 6)

Similar in function to register 6 of the 6522. Provides access to the timer 1 low order latches.

## T1LH (Reg 7)

Similar in function to register 7 of the 6522. Provides access to the timer 1 high order latches.

## T2CL (Reg 8)

Similar in function to register 8 of the 6522. Provides access to timer 2 low order latch / count.

## T2CH (Reg 9)

Similar in function to register 9 of the 6522. Provides access to timer 2 high order latch / count.

## SR (Reg 10)

Similar in function to register 10 of the 6522. The shift register is 12-bits wide. Data is shifted into bit zero and out of bit eleven in a manner analogous to the eight-bit operation.

## ACR (Reg 11)

The low order eight bits of the register mirror the 6522 function.

|  |  |
| --- | --- |
| Bits | Function |
| 0 | port a input latch enable |
| 1 | port b input latch enable |
| 2 to 4 | shift register mode |
| 5 | timer 2 mode |
| 6 to 7 | timer 1 mode |
| 8 | timer 3 mode (1 = continuous, 0 = pulse) |
| 9 to 11 | reserved |
|  |  |

|  |  |
| --- | --- |
| Timer 2 Mode | Operation |
| 0 | count down bus clock |
| 1 | count down negative edges of PB6 |

## PCR (Reg 12)

The low order eight bits of the register mirror the 6522 function. Only eight bits of this register are implemented.

|  |  |
| --- | --- |
| Bits |  |
| 0 | CA1 mode |
| 1 to 3 | CA2 mode |
| 4 | CB1 mode |
| 5 to 7 | CB2 mode |
| 8 to 11 | reserved |

## IFR (Reg 13)

The interrupt flag register mostly mirrors the operation of the interrupt flag register in the 6522. There is one extra bit (bit 7) which indicates a timer 3 interrupt.

|  |  |
| --- | --- |
| Bits | Source |
| 0 | ca2 active transition |
| 1 | ca1 active transition |
| 2 | shift register |
| 3 | cb2 active transition |
| 4 | cb1 active transition |
| 5 | timer 1 underflow |
| 6 | timer 2 underflow |
| 7 | timer 3 underflow |
| 8 to 10 | reserved |
| 11 | set if any interrupt is present |
|  |  |

## IER (Reg 14)

This register mirrors the function of the IER register in the 6522. There is one extra bit assigned as interrupt enable for timer 3 (bit 7 of the IER).

## T3CMPL (Reg 20)

This register contains the low order byte of the value to compare timer 3 against. When timer 3 counts past the value contained in the T3CMP register its interrupt flag will be set. If timer 3 interrupts are enable an interrupt will be signalled.

## T3CMPH (Reg 21)

This register contains the high order byte of the value to compare timer 3 against.

# Ports

|  |  |  |  |
| --- | --- | --- | --- |
| Signal | I/O | Wid | Purpose |
| rst\_i | I | 1 | reset |
| clk\_i | I | 1 | bus clock input |
| wc\_clk\_i | I | 1 | Timer #3 clock input (wall clock) |
| cs\_i | I | 1 | circuit/core select |
| irq\_o | O | 1 | interrupt request |
|  | WISHBONE SIGNALS | | |
| cyc\_i | I | 1 | bus cycle valid |
| stb\_i | I | 1 | data transfer strobe |
| ack\_o | O | 1 | data transfer acknowledge |
| we\_i | I | 1 | write enable |
| adr\_i | I | 5 | address bits (selects register) |
| dat\_i | I | 12 | data input bus (ground bits 8 to 31 if using as an 8-bit peripheral) |
| dat\_o | O | 12 | data output bus |
|  | Port A | | |
|  |  |  |  |
| pa\_o | O | 12 | port A output |
| pa\_i | I | 12 | port A input |
| pa\_t | O | 12 | port A tri-state control |
| ca1 | I | 1 | CA1 input |
| ca2\_i | I | 1 | CA2 input |
| ca2\_o | O | 1 | CA2 output |
| ca2\_t | O | 1 | CA2 tri-state control |
|  | Port B | | |
| pb\_o | O | 12 | port B output |
| pb\_i | I | 12 | port B input |
| pb\_t | O | 12 | port B tri-state control |
| cb1\_i | I | 1 | CB1 input |
| cb1\_o | O | 1 | CB1 output |
| cb1\_t | O | 1 | CB1 tri-state control |
| cb2\_i | I | 1 | CB2 input |
| cb2\_o | O | 1 | CB2 output |
| cb2\_t | O | 1 | CB2 tri-state control |
|  | Timer Output | | |
| t1\_if | O | 1 | timer #1 interrupt flag output |
| t2\_if | O | 1 | timer #2 interrupt flag output |
| t3\_if | O | 1 | timer #3 interrupt flag output |