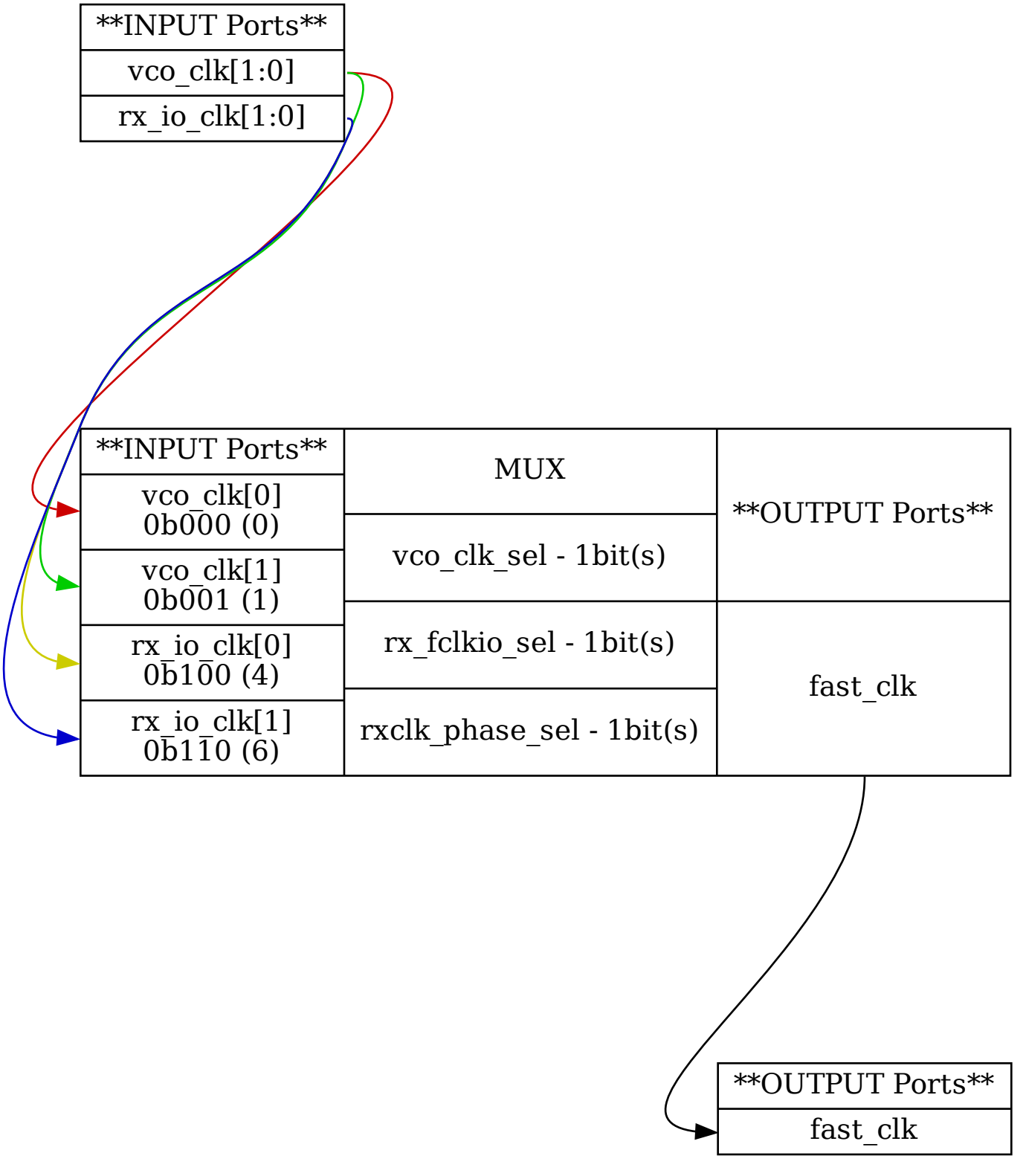
INPUT Ports
vco_clk[1:0]
rx_io_clk[1:0]
INPUT Ports
vco_clk[0]
0b000 (0)
vco_clk[1]
0b001 (1)
rx_io_clk[0]
0b100 (4)
rx_io_clk[1]
0b110 (6)
MUX
vco_clk_sel - 1bit(s)
rx_fclkio_sel - 1bit(s)
rxclk_phase_sel - 1bit(s)
OUTPUT Ports
fast_clk
OUTPUT Ports
fast_clk