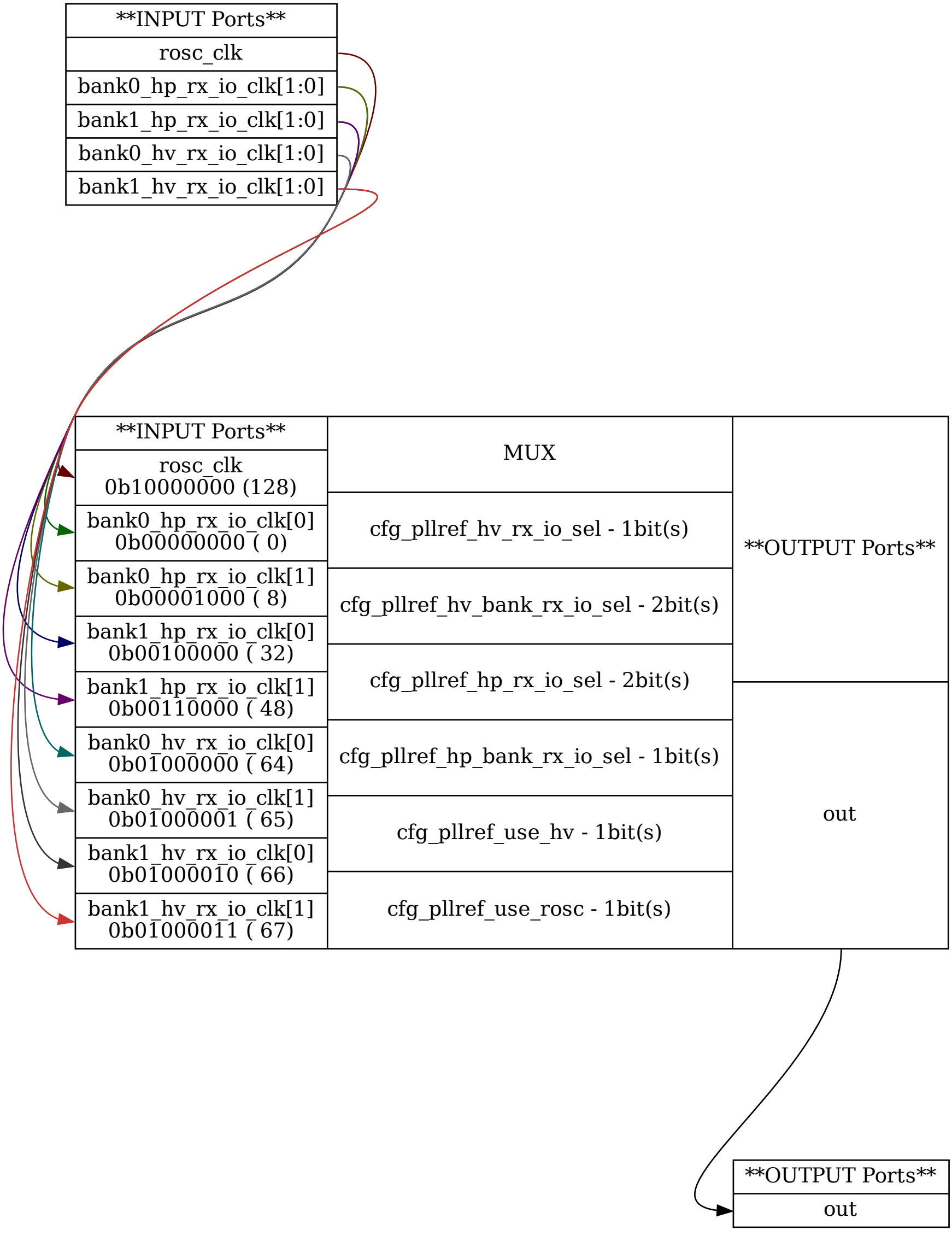
INPUT Ports
rosc_clk
bank0_hp_rx_io_clk[1:0]
bank1_hp_rx_io_clk[1:0]
bank0_hv_rx_io_clk[1:0]
bank1_hv_rx_io_clk[1:0]
INPUT Ports
rosc_clk
0b10000000 (128)
bank0_hp_rx_io_clk[0]
0b00000000 (0)
bank0_hp_rx_io_clk[1]
0b00001000 (8)
bank1_hp_rx_io_clk[0]
0b00100000 (32)
bank1_hp_rx_io_clk[1]
0b00110000 (48)
bank0_hv_rx_io_clk[0]
0b01000000 (64)
bank0_hv_rx_io_clk[1]
0b01000001 (65)
bank1_hv_rx_io_clk[0]
0b01000010 (66)
bank1_hv_rx_io_clk[1]
0b01000011 (67)
MUX
cfg_pllref_hv_rx_io_sel - 1bit(s)
cfg_pllref_hv_bank_rx_io_sel - 2bit(s)
cfg_pllref_hp_rx_io_sel - 2bit(s)
cfg_pllref_hp_bank_rx_io_sel - 1bit(s)
cfg_pllref_use_hv - 1bit(s)
cfg_pllref_use_rosc - 1bit(s)
OUTPUT Ports
out
OUTPUT Ports
out