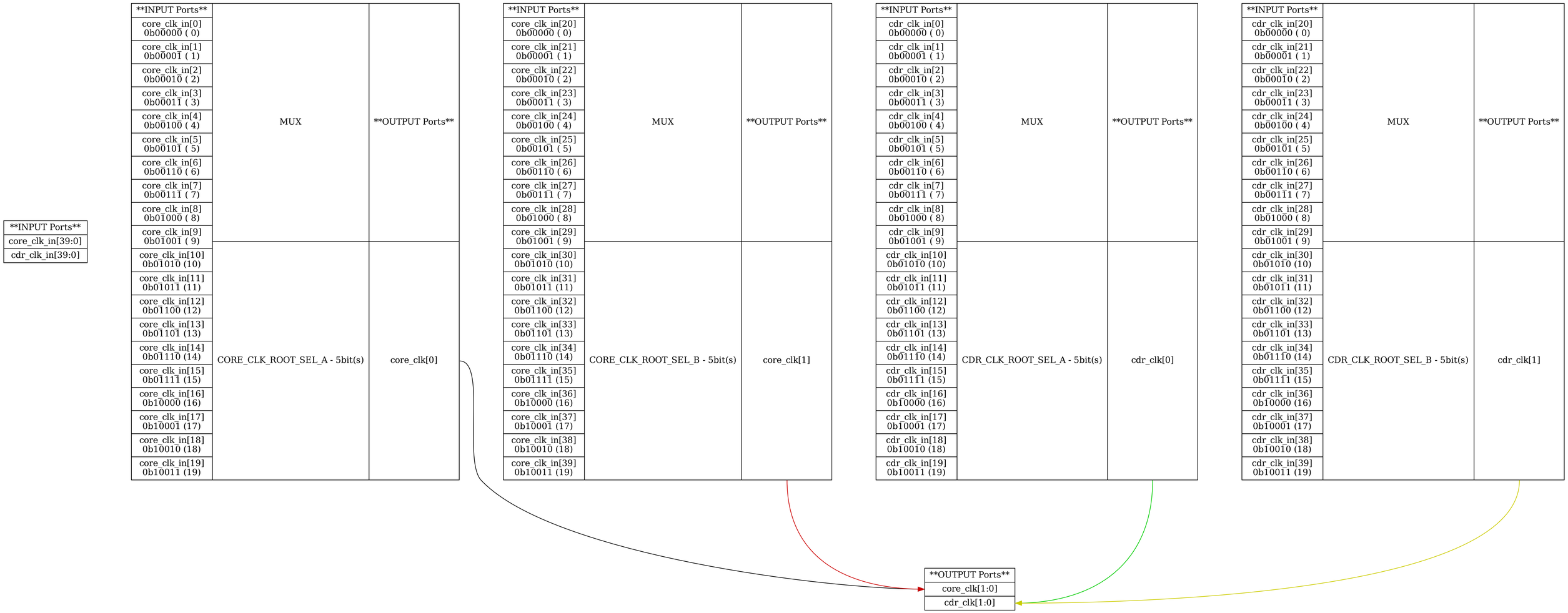
INPUT Ports
core_clk_in[39:0]
cdr_clk_in[39:0]
INPUT Ports
core_clk_in[0] 0b00000 (0)
core_clk_in[1] 0b00001 (1)
core_clk_in[2] 0b00010 (2)
core_clk_in[3] 0b00011 (3)
core_clk_in[4] 0b00100 (4)
core_clk_in[5] 0b00101 (5)
core_clk_in[6] 0b00110 (6)
core_clk_in[7] 0b00111 (7)
core_clk_in[8] 0b01000 (8)
core_clk_in[9] 0b01001 (9)
core_clk_in[10] 0b01010 (10)
core_clk_in[11] 0b01011 (11)
core_clk_in[12] 0b01100 (12)
core_clk_in[13] 0b01101 (13)
core_clk_in[14] 0b01110 (14)
core_clk_in[15] 0b01111 (15)
core_clk_in[16] 0b10000 (16)
core_clk_in[17] 0b10001 (17)
core_clk_in[18] 0b10010 (18)
core_clk_in[19] 0b10011 (19)
MUX
CORE_CLK_ROOT_SEL_A - 5bit(s)
OUTPUT Ports
core_clk[0]
INPUT Ports
core_clk_in[20] 0b00000 (0)
core_clk_in[21] 0b00001 (1)
core_clk_in[22] 0b00010 (2)
core_clk_in[23] 0b00011 (3)
core_clk_in[24] 0b00100 (4)
core_clk_in[25] 0b00101 (5)
core_clk_in[26] 0b00110 (6)
core_clk_in[27] 0b00111 (7)
core_clk_in[28] 0b01000 (8)
core_clk_in[29] 0b01001 (9)
core_clk_in[30] 0b01010 (10)
core_clk_in[31] 0b01011 (11)
core_clk_in[32] 0b01100 (12)
core_clk_in[33] 0b01101 (13)
core_clk_in[34] 0b01110 (14)
core_clk_in[35] 0b01111 (15)
core_clk_in[36] 0b10000 (16)
core_clk_in[37] 0b10001 (17)
core_clk_in[38] 0b10010 (18)
core_clk_in[39] 0b10011 (19)
MUX
CORE_CLK_ROOT_SEL_B - 5bit(s)
OUTPUT Ports
core_clk[1]
INPUT Ports
cdr_clk_in[0] 0b00000 (0)
cdr_clk_in[1] 0b00001 (1)
cdr_clk_in[2] 0b00010 (2)
cdr_clk_in[3] 0b00011 (3)
cdr_clk_in[4] 0b00100 (4)
cdr_clk_in[5] 0b00101 (5)
cdr_clk_in[6] 0b00110 (6)
cdr_clk_in[7] 0b00111 (7)
cdr_clk_in[8] 0b01000 (8)
cdr_clk_in[9] 0b01001 (9)
cdr_clk_in[10] 0b01010 (10)
cdr_clk_in[11] 0b01011 (11)
cdr_clk_in[12] 0b01100 (12)
cdr_clk_in[13] 0b01101 (13)
cdr_clk_in[14] 0b01110 (14)
cdr_clk_in[15] 0b01111 (15)
cdr_clk_in[16] 0b10000 (16)
cdr_clk_in[17] 0b10001 (17)
cdr_clk_in[18] 0b10010 (18)
cdr_clk_in[19] 0b10011 (19)
MUX
CDR_CLK_ROOT_SEL_A - 5bit(s)
OUTPUT Ports
cdr_clk[0]
INPUT Ports
cdr_clk_in[20] 0b00000 (0)
cdr_clk_in[21] 0b00001 (1)
cdr_clk_in[22] 0b00010 (2)
cdr_clk_in[23] 0b00011 (3)
cdr_clk_in[24] 0b00100 (4)
cdr_clk_in[25] 0b00101 (5)
cdr_clk_in[26] 0b00110 (6)
cdr_clk_in[27] 0b00111 (7)
cdr_clk_in[28] 0b01000 (8)
cdr_clk_in[29] 0b01001 (9)
cdr_clk_in[30] 0b01010 (10)
cdr_clk_in[31] 0b01011 (11)
cdr_clk_in[32] 0b01100 (12)
cdr_clk_in[33] 0b01101 (13)
cdr_clk_in[34] 0b01110 (14)
cdr_clk_in[35] 0b01111 (15)
cdr_clk_in[36] 0b10000 (16)
cdr_clk_in[37] 0b10001 (17)
cdr_clk_in[38] 0b10010 (18)
cdr_clk_in[39] 0b10011 (19)
MUX
CDR_CLK_ROOT_SEL_B - 5bit(s)
OUTPUT Ports
cdr_clk[1]
OUTPUT Ports
core_clk[1:0]
cdr_clk[1:0]