```
[VIRT_MROM] =         {       .base: 0x1000,         .size: 0x11000 },
    uint32_t reset_vec[8] = {
        0x00000297,                     /* 1:  auipc  t0, %pcrel_hi(dtb) */
        0x02028593,                     /*     addi   a1, t0, %pcrel_lo(1b) */
        0xf1402573,                     /*     csrr   a0, mhartid  */
#if defined(TARGET_RISCV32)
        0x0182a283,                     /*     lw     t0, 24(t0) */
#elif defined(TARGET_RISCV64)
        0x0182b283,                     /*     ld     t0, 24(t0) */
#endif
        0x00028067,                     /*     jr     t0 */
        0x00000000,
        start_addr,                     /* start: .dword */
        0x00000000,
                                        /* dtb: */
    };
    target_ulong start_addr = memmap[VIRT_DRAM].base;
    [VIRT_DRAM] =         { .base: 0x80000000,         .size: 0x0 },
```