```
static void riscv virt board init(MachineState *machine)
 {
      const struct MemmapEntry *memmap = virt memmap;
      RISCVVirtState *s = RISCV VIRT MACHINE(machine);
      MemoryRegion *system memory = get system memory();
      MemoryRegion *main mem = g_new(MemoryRegion, n_structs: 1);
      MemoryRegion *mask rom = g_new(MemoryRegion, n_structs: 1);
      char *plic hart config;
      size t plic hart config len;
      target ulong start addr = memmap[VIRT DRAM].base;
sifive clint create(memmap[VIRT_CLINT].base,
   memmap[VIRT_CLINT].size, smp_cpus,
   sip_base: SIFIVE_SIP_BASE, timecmp_base: SIFIVE_TIMECMP_BASE, time_base: SIFIVE_TIME_BASE);
serial_mm_init(system_memory, memmap[VIRT_UART0].base,
    it_shift: 0, irq: qdev get gpio in(DEVICE(obj: s->plic), n: UARTO_IRQ), baudbase: 399193,
    chr: serial_hd( i: 0), end: DEVICE_LITTLE_ENDIAN);
virt flash create(s);
```