ECE 6213 – Design of VLSI Circuits

Fall 2022 – The George Washington University – Dr. Jerry Wu

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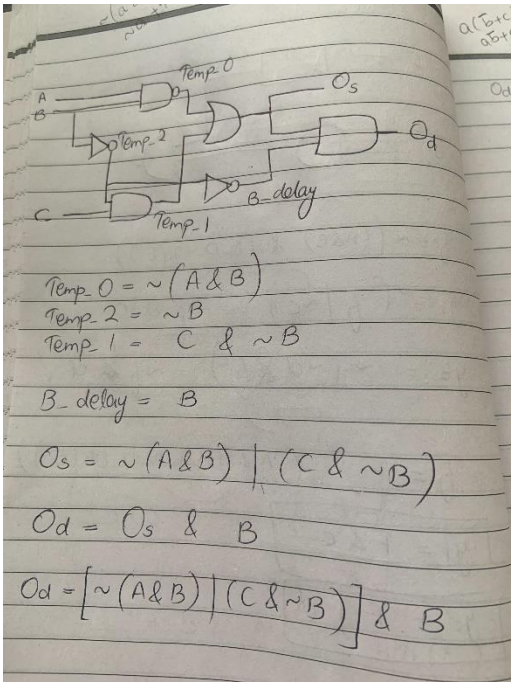
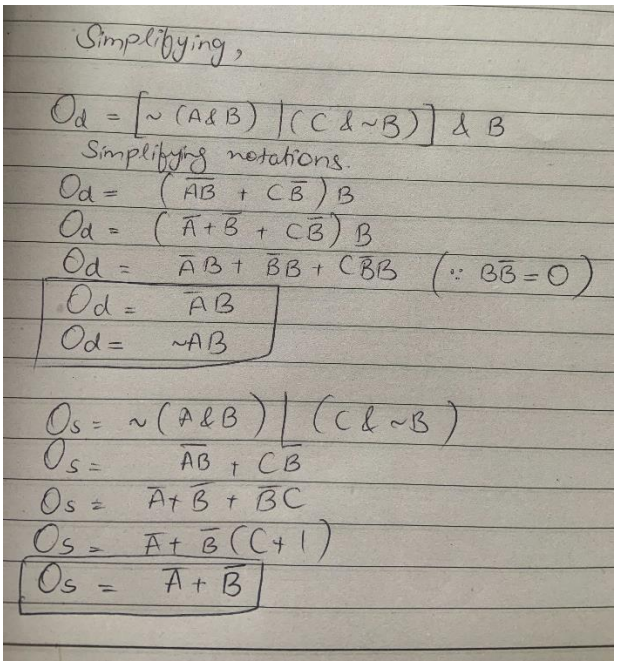
Problem 1 – 35 points

- **Obtain the equation and simplify it accordingly**

  The equation is: $O_{dynamic} = [\sim(A\&B)|(C\&\sim B)]\ \&\ B$. My work is attached below:



The simplified expressions are: $O_{static} = \sim A \mid \sim B = \sim(AB)$, and $O_{dynamic} = \sim AB$. My working is below:



- **Discuss the possible issue with the original circuit**

Let's calculate the timing delays for the two outputs:

$Temp_0 = 2\ nS$

$Temp_2 = 0.8\ nS$

$Temp_1 = 0.8 + 2 = 2.8\ nS$

$O_{static} = 1.5 + \ 2.8\ nS$ (longer delay out of its two inputs) $= 4.3\ nS$

$B_{delay} = 0.8 + 0.8 = 1.6\ nS$

$O_{dynamic} = 2 + 4.3 = 6.3\ nS$

The issue thus in the circuit is that even though we wanted the B_{delay} to be the critical path for $O_{dynamic}$, the gate delay for O_{static} is greater and thus instead the total delay is longer than intended.

Problem 2 – 55 points

- **Create a truth table for "excess-5" code to BCD**

Excess-5 input				**BCD output**			
w	**x**	**y**	**z**	**a**	**b**	**c**	**d**
0	1	0	1	0	0	0	0
0	1	1	0	0	0	0	1
0	1	1	1	0	0	1	0
1	0	0	0	0	0	1	1
1	0	0	1	0	1	0	0
1	0	1	0	0	1	0	1
1	0	1	1	0	1	1	0
1	1	0	0	0	1	1	1
1	1	0	1	1	0	0	0
1	1	1	0	1	0	0	1

Rest of the cases are don't care X.

- **Derive and optimize each output (a, b, c, d) as a function of the inputs (by K-maps based on your truth table)**

K-Maps:

Output a		y, z			
		00	**01**	**11**	**10**
w, x	**00**	X	X	X	X
	01	X			
	11		1	X	1
	10				

a(w, x, y, z) = wxz + wxy

Verilog: assign a = (w & x & z) | (w & x & y);

Output b		y, z			
		00	**01**	**11**	**10**
w, x	**00**	X	X	X	X
	01	X			
	11	1		X	
	10		1	1	1

b(w, x, y, z) = x'y + x'z + xy'z'

Verilog: assign b = (~x & z) | (~x & y) | (x & ~y & ~z);

Output c		y, z			
		00	**01**	**11**	**10**
w, x	**00**	X	X	X	X
	01	X		1	
	11	1		X	
	10	1		1	

c(w, x, y, z) = y'z' + yz

Verilog: assign c = (y & z) | (~y & ~z);

Output d		y, z			
		00	**01**	**11**	**10**
w, x	**00**	X	X	X	X
	01	X			1
	11	1		X	1
	10	1			1

d(w, x, y, z) = z’

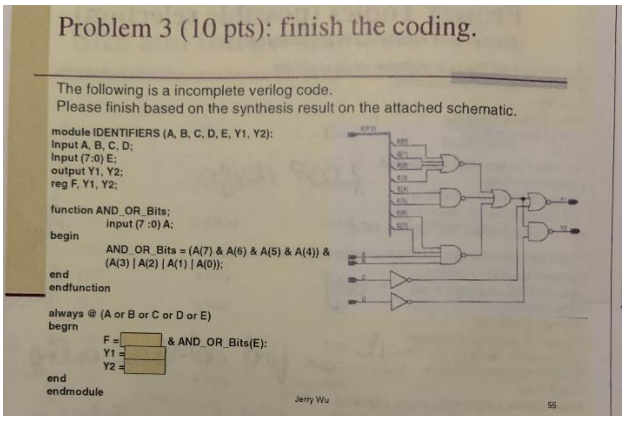
Verilog: assign d = ~z;

- **Model a converter circuit at gate level in structural style**

```
module p2_gates(w, x, y, z, a, b, c, d);

input w, x, y, z;
output a, b, c, d;

wire t1, t2, t3

    // model output a

    and g1(t1, w, x);   // t1 = wx
    and g2(t2, t1, y);  // t2 = wxy
    and g3(t3, t1, z);  // t3 = wxz
    or g4(a, t2, t3);   // a = wxy + wxz

    // model output b
    not g5(t4, x);          // t4 = x'
    and g6(t5, t4, y);      // t5 = x'y
    and g7(t6, t4, z);      // t6 = x'z

    not g8(t7, y);          // t7 = y'
    not g9(t8, z);          // t8 = z'

    and g10(t9, x, t7);     // t9 = xy'
    and g11(t10, t9, t8);   // t10 = xy'z'

    or g12(t11, t5, t6);    // t11 = x'y + x'z
    or g13(b, t11, t10);    // b = x'y + x'z + xy'z'

    // model output c
    and g14(t12, t7, t8);   // t12 = y'z'
    and g15(t13, y, z);     // t13 = yz
    or g16(c, t12, t13);    // c = y'z' + yz

    // model output d
    not g17(d, z);          // d = z'

endmodule
```

Problem 3 – 10 points

- **Following is incomplete Verilog code, please finish based on the synthesis result on the attached schematic.**



F = A & B & AND_OR_Bits(E)

Y1 = F & C

Y2 = F | D