UART\_Clock\_Generator

Diagram

Description automatically generated

The following is a breakdown of my implementation of the different modules for the UART\_Clock\_generator, as well as corresponding verification tests.

**Module 1: Divide\_by\_13**

For verification, I simply recreated the waveforms from the book.

The source file is: divideby13.v, and the testbench is divideby13\_tb.v

Diagram

Description automatically generated with medium confidence

Graphical user interface

Description automatically generated

**Module 2:** 8 to 1 multiplexer

The source file is: 8to1mux.v, and the testbench is 8to1mux \_tb.v

For testing, I initialize each of the 8 inputs randomly, cycle through the select pins, and assert the correct output. I also implemented error monitoring, watchdog signals, as well as self-reporting in my testbench. The testbench executes with 0 errors.

Text

Description automatically generated