OS INSPIRED COMPLETE KERNEL FUSION

A Thesis

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Osayamen Jonathan Aimuyo

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ABSTRACT

Distributed Machine Learning (DML) is increasingly recognized as a communication-bound workload, with most existing work aiming to alleviate this bottleneck through communication–computation overlap. However, current approaches—largely reliant on CPU-managed operator scheduling and synchronous communication collectives—leave significant performance on the table.

This thesis identifies, analyzes and addresses the inefficiencies arising from the interplay between CPU-driven collective communication and highly parallel GPU computation. We demonstrate that the standard bulk-synchronous communication model underutilizes GPU interconnect bandwidth and is especially vulnerable to straggler-induced performance degradation. Focusing on dynamic workloads such as Mixture-of-Experts (MoE), we highlight two critical bottlenecks. First, we observe *payload inefficiency* at the application layer, where existing collective primitives force unnecessary padding of GPU network buffers. Second, we expose how CPU-driven execution limits the exploitation of *task locality* and introduces artificial synchronization barriers across distributed GPU tasks.

To overcome these limitations, we propose a model of *complete GPU residency*, where inter-GPU communication is integrated directly into GPU kernels. We realize this vision in *FlashDMoE*: a persistent, in-kernel, actor-style operating system with packet switching that enables complete operator fusion for Distributed MoE (DMoE) into a *single kernel*, the first of its kind. *FlashDMoE* features a modular, message-driven architecture that supports lockless execution

across tens of thousands of GPU threads and across distributed GPUs as well. We demonstrate how *FlashDMoE* addresses the all-to-all communication bottleneck in expert parallelism and enables high-throughput, GPU-initiated communication. Evaluated against state-of-the-art distributed MoE frameworks, *FlashDMoE* achieves up to **15**× speedup, establishing a new, scalable design methodology for distributed GPU systems.

BIOGRAPHICAL SKETCH

Osayamen Jonathan Aimuyo is a computer science researcher specializing in distributed and parallel computing systems and algorithms. His work focuses on low-level optimizations for computational and communication bottlenecks in large-scale machine learning training and inference on accelerators. Jonathan earned a BS in computer engineering, *summa cum laude*, with Tau Beta Pi and Phi Kappa Phi Honors from the University of Texas at Dallas (class of 2023), where he was a Presidential Achievement Scholar and a semifinalist for the national Jack Kent Cooke Transfer Scholarship (2019). He is currently a second-year CS MS student at Cornell University, advised by Dr. Rachee Singh. In industry, he has contributed to large-scale distributed systems through internships at Microsoft ('22 - '24), Chime Financial ('22), and JPMorgan Chase ('20 - '21). After graduating from Cornell, he will intern at NVIDIA with the CUDA Math Libraries team, before beginning his PhD in Computer Science at Stanford University in Fall 2025, where his research would be supported by the **NSF GRFP** fellowship.

To those who stubbornly refuse to give up despite circumstances suggesting otherwise.

ACKNOWLEDGEMENTS

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To the **Christ Chapel Choir ('24/25)**, thank you for being my second family away from home. I joined you not knowing how to read sheet music, yet you welcomed me warmly and gave me room to grow rapidly. That kindness means more to me than I can express. One of my fondest memories was singing Han-

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CHAPTER 1

INTRODUCTION

State-of-the-art large language models (LLMs), including DeepSeek-v3 [10], LLama4 [3], DBRX [42] and Snowflake Arctic [43], have adopted the Mixture-of-Experts (MoE) [44] architecture for its computational efficiency [41] and reliable performance across language modeling tasks [10, 3, 21].

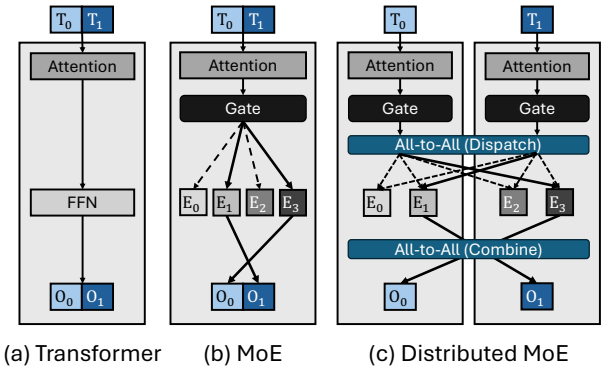


Figure 1.1: Transformer blocks (a) without MoE, (b) with MoE, and (c) with distributed MoE and expert parallelism. `T`, `E`, and `O` represent input tokens, experts, and output activations, respectively.

Depicted in Figure 1.1(a), the conventional Transformer block consists of a self-attention module followed by a feed-forward network (FFN) [49]. In contrast, MoE architectures replace this single FFN with identically sized FFNs, otherwise known as experts, (Figure 1.1(b)). A trainable neural network, known as a gate function, sparsely activates these experts by dynamically routing input tokens to selected experts at runtime. This increase in model parameters (more FFNs) improves model quality without a *corresponding increase in computational cost*.

1.1 Computational Cost Equivalence

The preceding claim seems counterintuitive because *shouldn't the increase in the number of experts yield a proportional increase in the model's computational operations?* The answer is no, due to how tokens are *distributed* across experts in comparison to the singular FFN. For example, consider a token matrix T as defined below where S is the sequence length and H the embedding dimension.

$$T \in \mathbb{R}^{S \times H}$$

The typical FFN operator, defined below,

$$\text{FFN}(x) = W_2 \cdot \phi(xW_1 + b_1) + b_2 \tag{1.1}$$

comprises two linear transformations on learnable weight matrices $W_1 \in \mathbb{R}^{H \times P}$, $W_2 \in \mathbb{R}^{P \times H}$ each followed by additions with bias terms $b_1 \in \mathbb{R}^{1 \times P}$, $b_2 \in \mathbb{R}^{1 \times H}$ and separated by a nonlinear activation ϕ (e.g., GELU [16] or ReLU [30]). Here dimension P is an intermediate projection for the FFN, typically $P = 4 \cdot H$ [27]. If we define $\mathcal{F}_{FFN}$ as the **F**loating **P**oint **OP**erations (FLOPs) needed to compute a forward pass of the FFN, then using Equation 1.1 we have the resulting expression.

$$\mathcal{F}_{FFN} = \mathcal{F}_{L_0} + \mathcal{F}_{L_1} \tag{1.2}$$

where $\mathcal{F}_{L_i}$ is the FLOPs cost for computing linear transformation i. These linear transformations are **GE**neral **M**atrix **M**ultiplications (GEMMs). We know that multiplying two matrices of sizes (M, K) and (K, N) demands $2MNK$ FLOPs, therefore we can expand Equation 1.2 as

$$\mathcal{F}_{FFN} = 2SHP + 2SHP = 4SHP \tag{1.3}$$

An MoE model differs from the dense transformer by *restricting* the number of tokens [25, 11] routed to an FFN (interchangeably called expert). Specifically,

for a model with N_e experts, each expert has a fixed capacity for tokens S_e defined as follows

$$S_e = \frac{S}{N_e} \tag{1.4}$$

With the above, we can compute $\mathcal{F}_{MoE}$. Intuitively, this quantity would be the aggregate of $\mathcal{F}_{FFN_j}$ where $j \in \{0, \cdots, N_e - 1\}$.

$$\mathcal{F}_{MoE} = \sum_{j=0}^{N_e-1} \mathcal{F}_{FFN_j} \tag{1.5}$$

Observe that $\mathcal{F}_{FFN_j}$ is derivable from Equation 1.2 by replacing S with S_e. Applying this observation and evaluating 1.5 gives the below result

$$\mathcal{F}_{MoE} = N_e \cdot 4S_eHP \tag{1.6}$$

Substituting with 1.4, yields the below which proves that the computational cost is equivalent between the MoE and dense transformer models!

$$\mathcal{F}_{MoE} = 4SHP = \mathcal{F}_{FFN} \tag{1.7}$$

This relationship presents empirically as uniform latency when N_e increases but only till a certain threshold. Exceeding this limit causes the latency to increase proportionally; existing work gives no explanation for this phenomenon, but we hypothesize GPU L1/L2 cache thrashing to be the culprit.

1.2 Communication Overheads in Distributed MoE

As MoE model sizes grow, GPU memory constraints prevent hosting all experts on a single device. The standard practice is to distribute experts across multiple GPUs using expert parallelism (EP), which requires the gate function to route tokens via AllToAll communication [10, 43, 42, 46]. Overall, each MoE

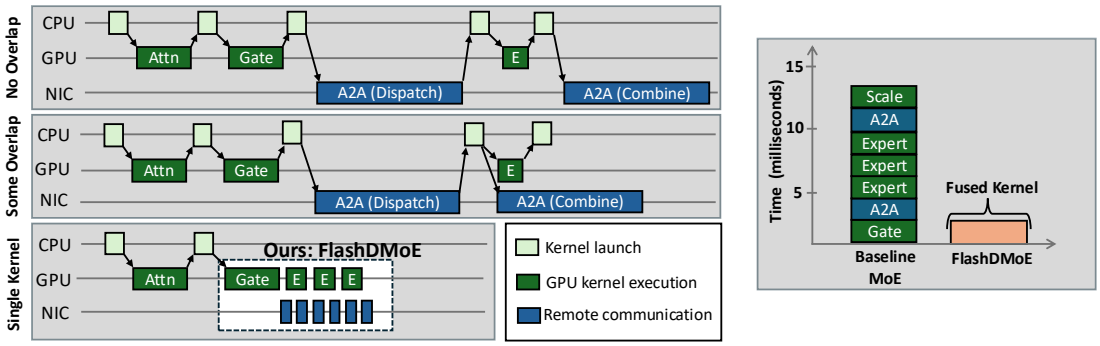


Figure 1.2: Comparing *FlashDMoE* with state-of-the-art techniques that either do not overlap communication and computation (left, top) or do some overlap (left, middle). *FlashDMoE* is a persistent kernel that fuses all computation and communication of the MoE operator (left, bottom). *FlashDMoE* implements device-initiated computation (gate, expert FFN, scale) and communication tasks (right).

layer executes two ALLTOALL operations during inference, introducing significant communication overhead. ALLTOALL communication is challenging to optimize on GPU networks and is highly sensitive to straggler delays—a phenomenon where a single *straggler* GPU delays all others from making progress. In practice, these communication operations can account for up to 40% of the total runtime during inference or training [26, 22].

1.3 Kernel Launch Overheads in Distributed MoE

Works	**Launched GPU Ops**
FlashDMoE	1
COMET [55]	33
Megatron-LM CUTLASS [36, 32]	85
Megatron-LM TE [36, 32]	261
Megatron-LM + DeepEP [10]	432
DeepSpeedMoE [41]	550

Table 1.1: **Kernel Fusion Comparison.** Our method is the first to fully fuse the DMoE layer into a single GPU kernel. We report GPU operations from detailed profiling with Nsight Systems.

To mitigate these communication bottlenecks, recent work pipelines computation with communication tasks (Figure 1.2, middle left). However, the effectiveness of these solutions is limited by the overhead of launching many kernels from the CPU. Specifically, MoE layers interleave multiple computation kernels (such as gate and expert computations) and communication operations, forcing the CPU to launch many GPU kernels per forward pass (see Table 1.1). Frequent kernel launches negatively affect performance by: (1) creating non-deterministic kernel start times across GPUs, exacerbating straggler issues; (2) introducing unnecessary synchronization points, causing GPUs to wait on peers or the CPU before proceeding; and (3) incurring repeated global memory round trips at kernel boundaries. Although CUDA graphs [53] can partially mitigate the first issue in static workloads, they are incompatible with MoE's dynamic expert routing patterns. Addressing the remaining issues requires novel solutions, which we provide in this work through complete kernel fusion and asynchronous device-initiated communication.

1.4 This work's Contributions: DMoE in a single kernel

To overcome these fundamental inefficiencies in state-of-the-art MoE models, we develop *FlashDMoE*, a novel MoE architecture that integrates all computation and communication tasks into a single persistent GPU kernel, namely a kernel that remains active for the entirety of the MoE operator (Figure 1.2 bottom left). Instead of multiple kernel launches coordinated by the CPU, *FlashDMoE* requires launching only one kernel, significantly reducing the involvement of the CPU in the MoE operator. Within the fused kernel, *FlashDMoE* implements a concurrent-programming model to achieve fine-grained parallelization of com-

putation and communication tasks of the MoE operator. This design enables *FlashDMoE* to efficiently utilize GPU resources by reducing idle time.

1.4.1 Warp Specialization and Tile Parallelism.

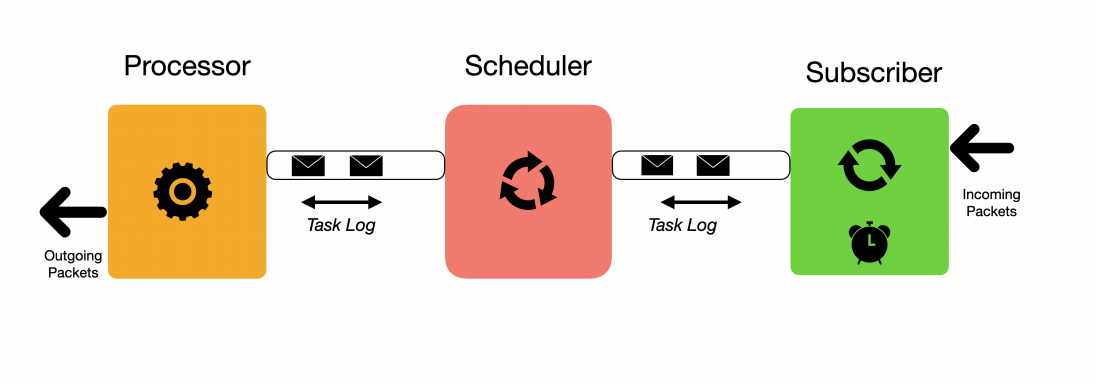


Figure 1.3: *FlashDMoE* Actors. The Subscriber observes received remote *packets* (blob of tiles), decodes them into *tasks* and notifies the scheduler of the enqueued tasks. We assign three CUDA warps to this role. The Scheduler maintains a *ready queue* of Processors from which it schedules tasks. The Processors performs the operation encoded in its task descriptor and eagerly communicates its output, if necessary.

FlashDMoE implements *tile-level parallelism*, meaning it partitions input token matrices into smaller, independent units called *tiles*, which are processed concurrently by GPU thread warps. These warps specialize as *processors* since they process input to compute the gate function and expert FFNs. A handful of warps perform specialized administrative tasks of (1) scheduling computational tasks by mapping them to warps (*scheduler*), and (2) communicating with other GPUs (*subscriber*). This design allows *FlashDMoE* to dynamically assign tasks to GPU warps based on warp availability and the current workload, ensuring that no warp remains idle while useful work can be done. *FlashDMoE* selects tile dimensions to maximize GPU arithmetic intensity and minimize register pressure.

1.4.2 Asynchronous and payload-efficient communication.

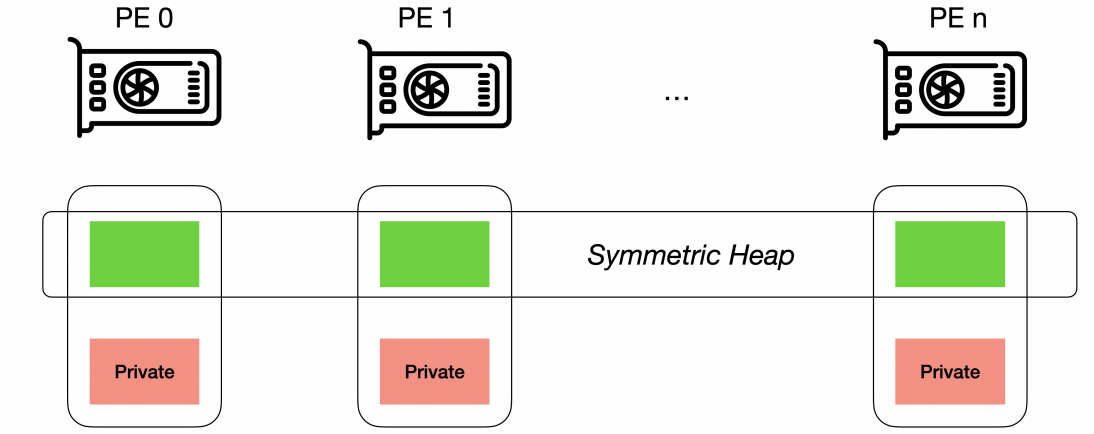


Figure 1.4: Depiction of a Partitioned Global Adress Space (PGAS) [54] across a *team* of **P**rocessing **E**lements (PEs). The symmetric heap is an unifromly sized memroy region resident on each PE and accessible by every other PE via one-sided **D**irect **M**emory **A**ccess (DMA) or **R**emote DMA (RDMA) operations.

By redesigning the MoE operator from the ground up, *FlashDMoE* resolves fundamental inefficiencies inherent in the conventional MoE execution pipeline. One inefficiency is due to workload imbalance across GPUs due to skewed popularity of experts. Existing implementations [41] indiscriminately perform AllToAll communications, transferring null values to GPUs that host unpopular experts, resulting in wasted communication bandwidth and unnecessary computations on null matrices. *FlashDMoE* introduces *payload-efficient* communication by sending tokens only to GPUs with actively selected experts, thereby conserving both communication and computational resources.

1.4.3 Technical Challenges

Realizing the single-kernel design of *FlashDMoE* required solving several technical challenges. *FlashDMoE*'s design is a radical departure from traditional synchronous AllToAll collectives, where GPUs remain idle until the slowest GPU completes its communication. Instead, *FlashDMoE* establishes a global address space via NVSHMEM [37] across all GPUs to achieve asynchronous communication between GPUs while allowing them to continue performing useful computation tasks. To implement device-initiated computation primitives, *FlashDMoE* develops custom high-performance GEMM operations for the MoE operator in CUTLASS [48].

1.4.4 Research Papers

This thesis comprises a first-author publication [4] at ACM SIGMETRICS'24 and another first-author submission in review at NeurIPS '25.

CHAPTER 2

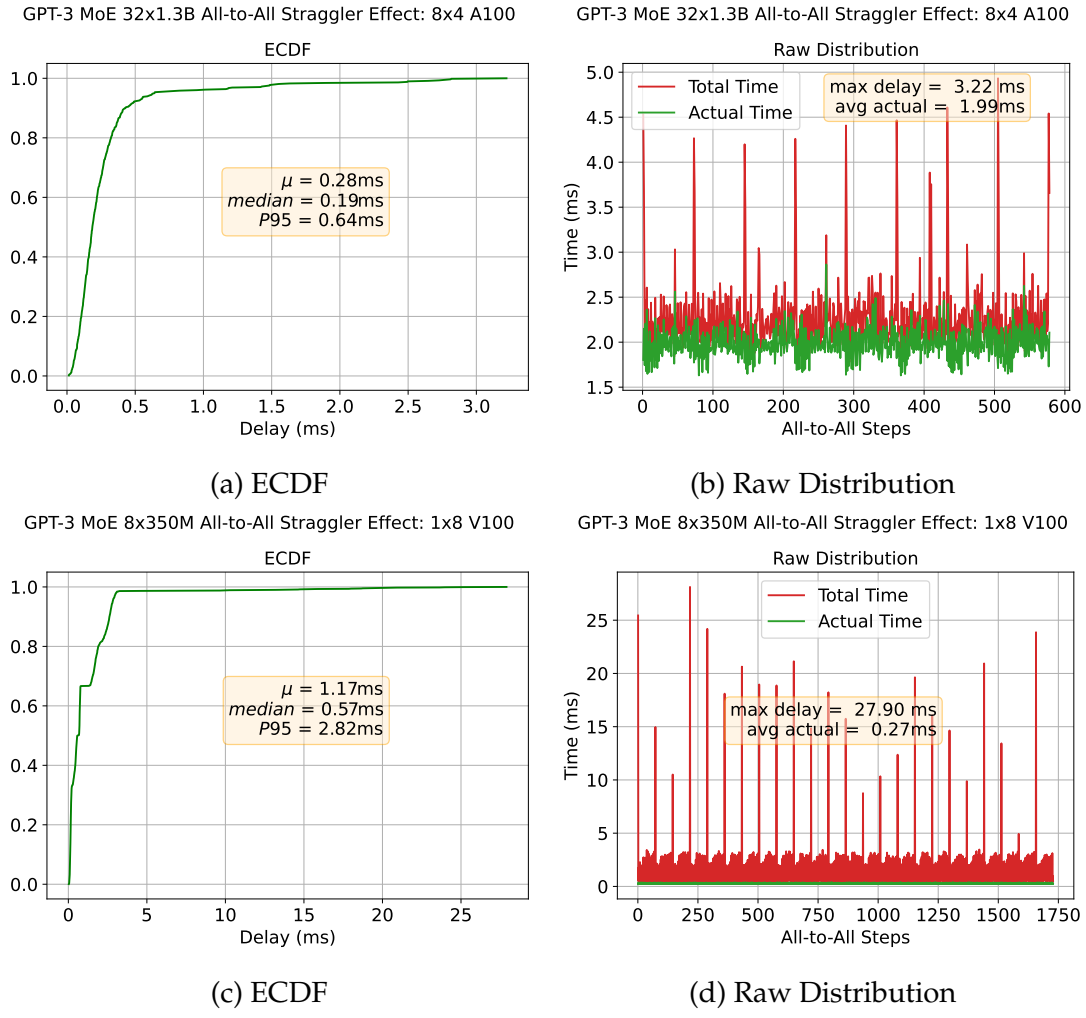
RELATED WORK

Computation-Communication Overlap. To reduce the communication overheads of synchronization in distributed DNN training, many research efforts have been focused on increasing the overlap of computation and communication. For generic Transformer-based models without MoE layers, many works [20, 52, 7, 39, 24, 47, 29, 50, 40] have provided insights and techniques to partition and schedule computation and communication operations, a imed at finer-grained overlapping. To address the challenges posed by AllToAll communication and expert parallelism in MoE training, Tutel [19] and FasterMoE [14] overlap AllToAll with expert computation. Lancet [23] additionally enables both non-MoE computation in forward pass and weight gradient computation in backward pass to be overlapped with AllToAll. Despite overlapping, the performance of these approaches is limited in practice due to blocking synchronous collective communication with barriers. In contrast, *FlashDMoE* fundamentally eliminates the inefficiencies with asynchronous, device-initiated data transfers overlapped with tiled computation all *within a single kernel*, further differentiating itself from SOTA works [56, 55, 10] who also use this form of kernel-initiated communication but at a coarse-grained granularity and without complete kernel fusion.

CHAPTER 3

MOTIVATION

3.1 Straggler Effect



(a) ECDF

(b) Raw Distribution

(c) ECDF

(d) Raw Distribution

Figure 3.1: Straggler effect of synchronous AllToAll. $M \times N$ A100 or V100 denotes N GPUs within a node across M nodes. Every GPU communicates with every other GPU per AllToAll step. We capture the distribution of delay induced by stragglers across many steps. **Actual Time** t_a denotes the fastest kernel execution time across all GPUs, conversely **Total Time** t is the maximum recorded step time, while *Delay* is the maximum difference between t and t_a.

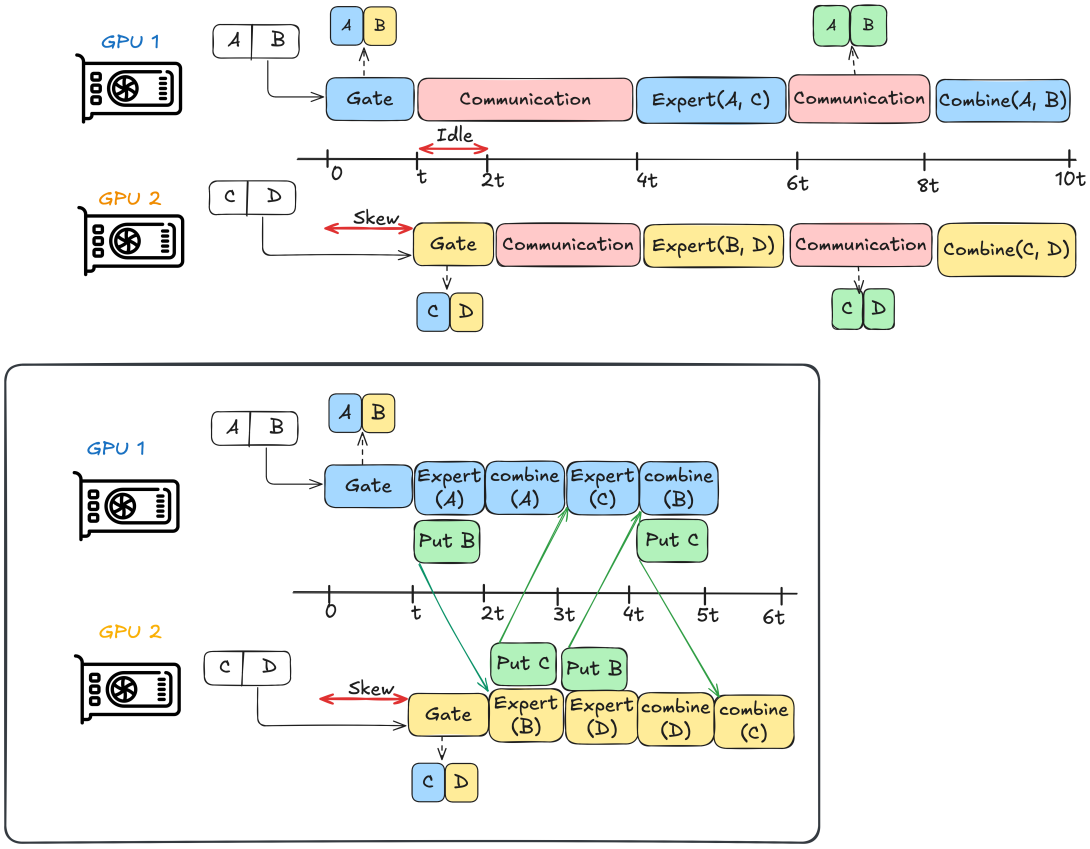


Figure 3.2: Overlapped Schedule (bottom) showing how idle time from the sequential schedule (top) is repurposed for computation. *FlashDMoE* implements the overlapped schedule.

ALLTOALL communication as currently used in MoE frameworks is a *synchronous* collective operation among all participating GPUs. In this setting, disparities in processing speeds or kernel scheduling among workers induce a straggler effect detrimental to the collective operation's performance. Specifically, as shown in Figure 3.1, for distributed training of a 1.3B MoE model across 32 A100 GPUs, we see P95 communication performance degradation of **1.32X** when compared to the mean actual kernel time from Figure 3.1b. This performance reduction is rather tame as the underlying hardware is a supercomputer that is well-tuned against "software jitter" [33]. On the other hand, the performance loss is more severe in a single node commodity Virtual Machine (VM)

of 8 V100 GPUs with higher bandwidth, where we observe p95 performance reduction of **11X**. In line with prior work [6, 8] from the HPC community, we argue that obviating the inherent barrier in this synchronous collective communication would allow GPUs to repurpose this observed idle time for useful computation.

3.2 Kernel Launch Overheads

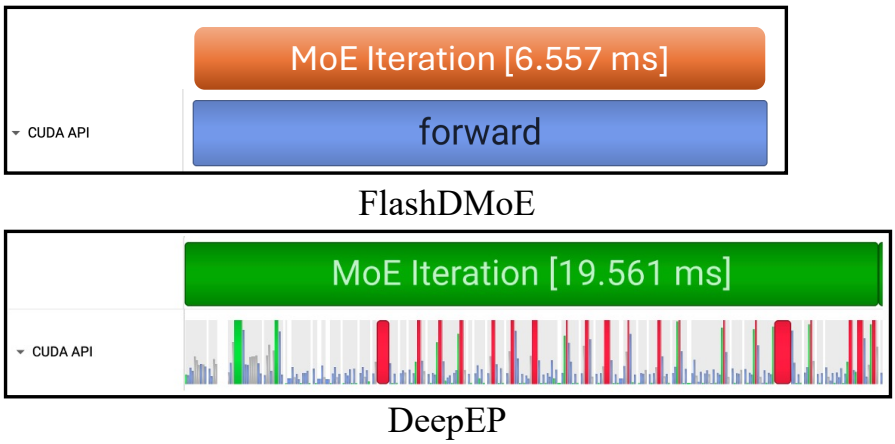


Figure 3.3: Kernel Launch overhead (CUDA API row) juxtaposed with runtime latency. Compared to DeepEP that launches 432 kernels, *FlashDMoE* launches a single one.

We compare the kernel launch overheads between *FlashDMoE* and existing baselines. Table 1.1 shows the number of kernel launches during a single forward pass: *FlashDMoE* launches exactly one persistent kernel, while the baselines require up to 550 short-lived kernels. Figure 3.3 visually compares *FlashDMoE* and DeepEP [10] using CUDA API traces captured by NSight Systems. DeepEP exhibits numerous small CUDA API calls, while *FlashDMoE* maintains high GPU utilization by avoiding launch overhead and synchronization gaps—achieving 93.17% GPU utilization (§6) compared to 20.61% for DeepEP.

CHAPTER 4

METHOD

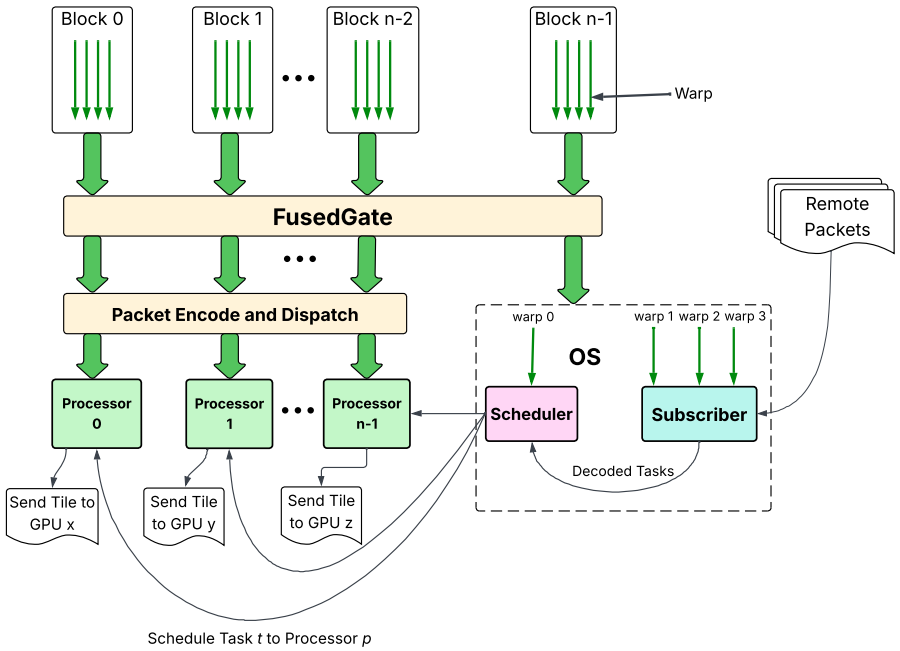


Figure 4.1: FlashDMoE *Fused Kernel*. Green arrows demonstrate block or warp specialization.

The performance of modern distributed MoE systems suffers from two primary bottlenecks: (1) frequent AllToAll collective communication operations on the critical execution path due to expert parallelism, and (2) significant overhead from repeatedly launching multiple computation and communication kernels on the host CPU. To overcome these limitations, we introduce *FlashDMoE*, a fully fused MoE operator implemented as a single persistent GPU kernel. Unlike previous approaches [55, 10, 41, 36, 18, 22, 15, 34, 45, 51, 9], *FlashDMoE* is the first solution to implement a *completely fused Distributed MoE kernel*, eliminating kernel launch overhead entirely by requiring only a single kernel launch (see Table 1.1).

Algorithm 1: FlashDMoE *Distributed MoE Fused Kernel*

Input: $A, O \in \mathbb{R}^{S \times H},\ E \in \mathbb{R}^{L \times H \times P},\ N$

```
begin
    T, G_φ ← FusedGate(A)
    if blockId +1 < N then
        Dispatch(T, A)
        processor::start()
    else
        if warpID == 0 then
            scheduler::start()
        else
            subscriber::start(E, O)
        end if
    end if
end
```

4.1 Actor Model

The design of *FlashDMoE* is based on the actor model of concurrent computation [2, 17, 12]. We implement this model by specializing GPU thread blocks and warps into three distinct actor roles: (1) **Processor** (§4), (2) **Subscriber** (§2), and (3) **Scheduler**(§3). The Processor performs compute (GEMMs and element-wise operations) and tile communication. We use CUTLASS [48] as the underlying infrastructure for high-performance BLAS routines and NVSHMEM for kernel-initiated communication [37]. The Subscriber and Scheduler perform administrative functions. Specifically, the Scheduler assigns computational tasks to available thread blocks. One key innovation is making the Scheduler both *multithreaded*, enabling high scheduling throughput, and *work-conserving*, ensuring consistently high GPU SM utilization. On the other hand, the Subscriber subscribes to data communicated over the network. Of the N thread blocks on a GPU, we specialize $N-1$ to adopt the **Processor** role. We specialize the last block for administrative functions. Within this block, we specialize three warps for the

Subscriber role and one warp for the **Scheduler** role. This split of thread blocks across actors is intentional: our goal is to use few resources for administrative tasks while reserving bulk of the resources for performing MoE computation tasks. Figure 4.1 summarizes the *FlashDMoE* architecture and its constituent actors, while Algorithm 1 gives a very close translation of the system in code.

4.2 Inter-Actor Interactions

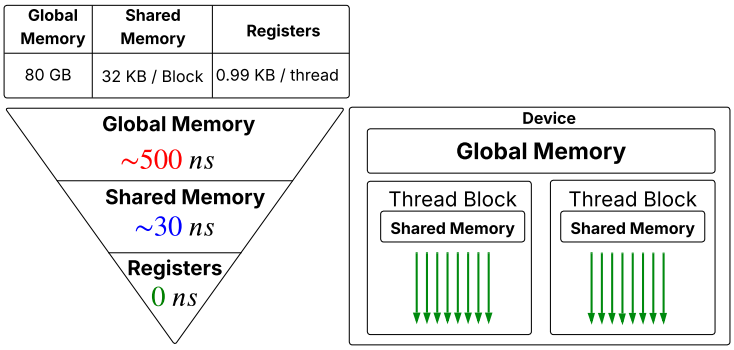


Figure 4.2: *GPU Memory Hierarchy*. The inverted pyramid (left) shows the load/store access latency [28, 1, 38]. Table above outlines the capacity for different memory tiers (for A100 GPUs). The shared memory and register capacity are static configurations for *FlashDMoE*. The right figure shows accessibility scopes: on-chip **registers** are scoped to a thread; on-chip **shared memory** is visible to all threads in a block; and off-chip **global memory** is accessible by all threads on device.

FlashDMoE decomposes MoE computation and communication at the granularity of a tile, a statically sized partition of a tensor, to achieve parallel execution and efficient overlap of tasks. Each tile corresponds to a discrete unit of work encapsulated by a *task descriptor*. The **Subscriber** actor decodes these task descriptors from the remote data packets it receives. Concurrently, the **Scheduler** actor receives notifications about available tasks and batches them for execution

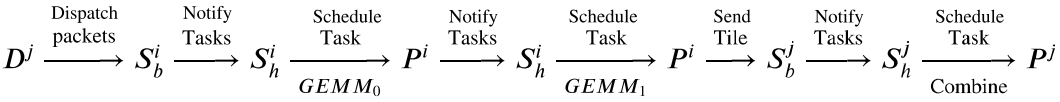


Figure 4.3: *DMoE Functional Dependencies Expressed as a Chain of Actor Interactions*. We denote S_b, S_h, and P as the Subscriber, Scheduler and Processor actors, respectively. For any actor $a \in \{S_b, S_b, P\}$, a^i identifies an actor on GPU i. We define D_i^j as the operator, where GPU j dispatches packets of tiles to GPU i, This diagram expresses task dependencies at the granularity of a tile, namely $GEMM_0$, $GEMM_1$, combine and communication produce an output tile.

by the **Processor** actors. **Processor** actors perform computations defined by the tasks, like the feed-forward network (FFN) and expert-combine operations. Figure 4.3 shows the chain of actor interactions in *FlashDMoE* that comprise DMoE.

4.3 Tiling

Selecting appropriate tile dimensions in *FlashDMoE* is crucial to ensure efficient GPU utilization. A small-sized tile underutilizes the GPU's tensor cores, while excessively large tiles create register pressure, causing performance-degrading register spills to local memory. After careful parameter sweeps, we choose tile dimensions of (128, 64). Our key insights are: increasing tile width raises the register usage per thread, potentially triggering costly spills; increasing tile height without adjusting thread count increases workload per thread, harming performance. Raising the thread count per block beyond our fixed value of 128 threads reduces the number of concurrent blocks, negatively affecting SM occupancy. Larger thread-block sizes also increase overhead from intra-block synchronization (*__syncthreads()* barriers), further degrading performance. Thus, our chosen tile dimensions deftly balance these constraints.

Algorithm 2: *Subscriber Actor*: executed by three warps

```
1  begin
2      interrupt ← GetSharedInterrupt()
3      flags ← GetSymmetricFlags()
4      tQ ← GetTQ()
5      // Predefined upper bound on the number of tasks.
6      // Modulated to the actual task count computed
7      // from dispatch signals received from peer GPUs
8      taskBound ← GetTaskBound()
9      while AtomicLoad(interrupt) == False do
10         // dispatch flags
11         do in parallel
12             Visit dispatch flags
13             Atomically retrieve signal
14             if Signal is set and flag is not visited then
15                 Mark visited
16                 SelfCorrectTaskBound(taskBound, Signal)
17                 Enforce memory consistency before consuming packet
18                 Decode packet into a set of GEMM_0 task descriptors
19                 Write task descriptors to tQ
20                 Notify Scheduler of decoded tasks
21             end if
22         end
23         Advance flags by number of dispatch flags length
24         Atomically retrieve signal
25         // combine signals
26         do in parallel
27             Visit combine flags: one per tile
28             if Signal is set and flag is not visited then
29                 Mark visited
30                 Enforce memory consistency before consuming packet
31                 Decode packet into a set of combine task descriptors
32                 Write task descriptors to tQ
33                 Notify Scheduler of decoded tasks
34             end if
35         end
36     end while
37 end
```

Algorithm 3: *Scheduler Actor*: executed by one warp

```
   Input: N: Number of processors
 1 begin
 2     scheduled ← 0
 3     tTB ← 0
 4     tqS ← {}
 5     pTDB ← GetProcessorDoorbell()
 6     sTDB ← GetSubscriberDoorbell()
 7     taskBound ← GetTaskBound()
 8     tTB ← AtomicLoad(taskBound)
 9     // circular buffer ready queue
10     rQ ← {}
11     // Populate ready queue with Processor ids
12     PopulateRQ(rQ)
13     while scheduled < tTB do
14         lt ← 0
15         do in parallel
16             Sweep doorbells and populate task counts into tqS
17             Aggregate locally observed task counts into lt
18         end
19         qS, taskTally ← 0
20         // qS is the inclusive output
21         WarpInclusiveSum(lt, qS, tasktally)
22         while tasktally > 0 do
23             Repopulate rQ with ready processor ids
24             do in parallel
25                 Starting at rQ[qS] signal processors about tasks from tqS
26             end
27         end while
28         if threadId == 0 then
29             tTB ← AtomicLoad(taskBound)
30         end if
31         tTB ← WarpBroadcast(tTB)
32     end while
33     InterruptSubscribers()
34     InterruptProcessors()
35 end
```

Algorithm 4: *Processor Actor*: executed by a block

```
1  begin
2      tQ ← GetTQ()
3      signal ← 0
4      // shared memory variables
5      task ← {}
6      interrupt ← False
7      complete ← False
8      while interrupt == False do
9          if warpId == 0 then
10             if threadId == 0 then
11                 awaitTaskFromScheduler(interrupt, signal)
12                 FencedNotifyRQ(ready)
13             end if
14             syncwarp()
15             warpReadTQ(tQ, signal, task)
16         end if
17         syncthreads()
18         if interrupt == False then
19             switch task.Type do
20                 case GEMM_0 do
21                     // fused GEMM, epilogue and async tile
                           staging
22                     fGET(GEMM_0, task)
23                     if threadId == 0 then
24                         complete ← NotifyTileCompletion()
25                     end if
26                     syncthreads()
27                     if complete == True then
28                         NotifySchedulerNextGEMM(tQ)
29                     end if
30                 end case
31                 case GEMM_1 do
32                     // fused GEMM, epilogue and async tile
                           transfer
33                     fGET(GEMM_1, task)
34                 end case
35                 case Combine do
36                     combine(task)
37                 end case
38             end switch
39         end if
40     end while
41 end
```

CHAPTER 5

PROGRAMMING ABSTRACTIONS

5.1 Task

We describe the FFN in §1.1, so here we explicate the *combine* operation. The expert-combine operation, used in architectures like GShard [25] and DeepSeek [10], merges outputs from multiple experts by computing a weighted combination based on their affinity scores:

$$C_i = \sum_{j=1}^{k} g_{i,e} \tag{5.1}$$

$$\mathbf{h}_i = \sum_{j=1}^{k} \frac{g_{i,e}}{C_i} \cdot \mathbf{h}_i^k \tag{5.2}$$

Above, $i \in 0, S-1$ represents an input token index, $e = E_{i,k}$ identifies the k-th expert selected for token i, and $g_{i,e}$ is the affinity score indicating how relevant expert e is for token i.

5.2 Unified Abstraction

We unify the FFN and combine operations under a common abstraction called a *task*. Tasks provide a uniform interface for communicating tile-level work among Subscribers, Schedulers, and Processors. Formally, a task descriptor $t \in \mathcal{T}$ is defined as a tuple:

$$t = (\mathcal{M}, \star, \phi)$$

where $\mathcal{M}$ is a set of metadata (such as device ID, tile index), $\star$ is a binary tensor operation (specifically, matrix multiplication $\cdot$ or Hadamard product $\odot$), and ϕ

is an element-wise activation function (e.g., ReLU or identity). We define a task t operating on input tensors A, B, D, producing output tensor C, as follows:

$$\mathcal{F}_t(A, B, C, D) := C \leftarrow \phi\,(A \star_t B + D) \tag{5.3}$$

The operator $\star_t$ (instantiated from $\star$) may behave differently depending on the task metadata $\mathcal{M}$, and the result of $A \star_t B$ is accumulated into D. We provide an example of task metadata in Figure 5.1.

```
#define GEMMs 2
struct __align__(16) Task {
    const byte* aData;
    array<const byte*, GEMMs> bData;
    array<byte*, GEMMs> cData;
    array<const byte*, GEMMs> dData;
    byte* rcData;
    uint64_t* flags;
    uint M;
    uint syncIdx;
    uint tileIdx;
    uint batchIdx;
    uint peerIdx;
    uint expertIdx;
    uint isPeerRemote;
    TaskType taskType;
    uint16_t tileSize;
    // Pad till 128-byte cache line
    uint padding[6] = {};
}
```

Figure 5.1: *Task Struct*. TaskType $\in \{GEMM_0,\ GEMM_1,\ Combine\}$

In practice, we implement each task defined by Equation 5.3 as a *single fused* `__device__` decorated function which the **Processor** (Algorithm 4) invokes at runtime. Fusion for t entails applying ϕ and the succeeding addition operation to registers storing the results of the binary operator $\star_t$. To illustrate its flexibility, we show how the FFN and expert-combine operations can be expressed

using this task framework. Note that we omit the matrix multiplication symbol $(\cdot)$ for simplicity. Also, ϕ_1 can be any activation function, while ϕ_2 is the identity function. The FFN is expressed as:

$$t_1 = (\mathcal{M}, \cdot, \phi_1), \quad t_2 = (\mathcal{M}, \cdot, \phi_2),$$

$$\mathcal{F}_{t_1}(A, B_1, C_1, D_1) \coloneqq C_1 \leftarrow \phi_1 \left(AB_1 + D_1\right),$$

$$\mathcal{F}_{t_2}(C_1, B_2, C_2, D_2) \coloneqq C_2 \leftarrow \phi_2 \left(C_1 B_2 + D_2\right).$$

Whereas, the expert-combine operation is formalized as:

$$t_3 = (\mathcal{M}, \odot, \phi_2),$$

$$\mathcal{F}_{t_3}(A, S, C, C) \coloneqq C \leftarrow \phi_2 \left(A \odot S + C\right).$$

5.3 Symmetric Tensor Layout for Inter-GPU Communication

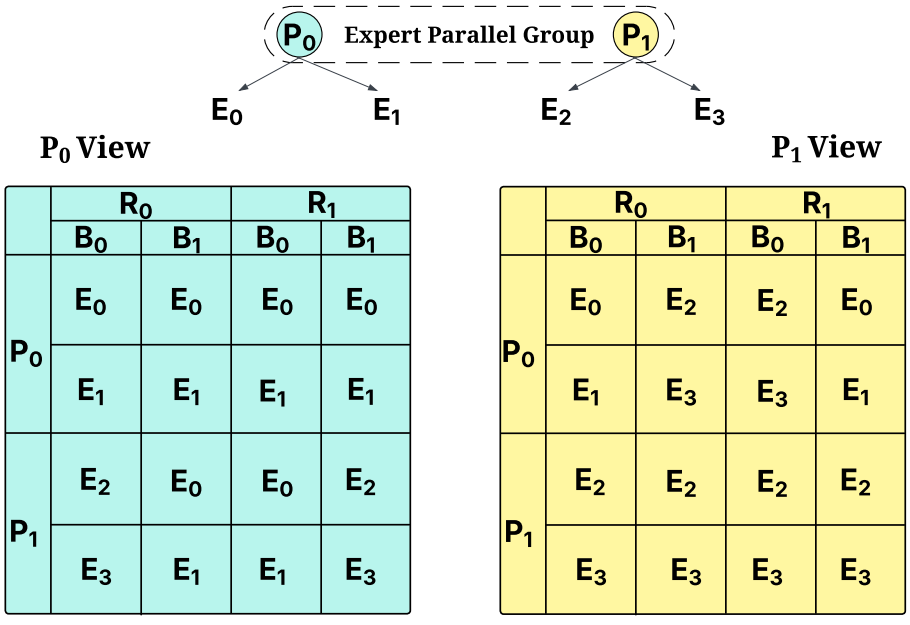


Figure 5.2: *Symmetric Tensor Layout across 2 Expert-parallel Processes.*

Within a single GPU device, the actors in *FlashDMoE* communicate through the GPU's memory subsystem (see Figure 4.2). Specifically, the Scheduler and Subscriber actors exchange data via fast shared memory, while other actor pairs communicate through global memory. For communication across multiple devices, *FlashDMoE* uses *device-initiated communication*, leveraging the one-sided PGAS (Partitioned Global Address Space) programming model [54]. However, achieving scalable and correct one-sided memory accesses in PGAS without costly synchronization is a known challenge [10, 56]. We address this challenge with a provably correct and scalable solution: a symmetric tensor layout L, supporting fully non-blocking memory accesses. We define L as:

$$L \in \mathbb{R}^{P \times R \times B \times E \times C \times H}$$

where: P is the expert parallel world size, R identifies communication rounds (two rounds, one for token dispatch and one for combine), B is number of staging buffers, E is the number of local experts, C is the upscaled expert capacity (§5.4) and H is the embedding dimension. Our core insight to enable non-blocking communication is *temporal buffering*. Specifically, we overprovision memory for the underlying token matrix by at least $2 \cdot r$ times, where r is the number of communication rounds in the dependency graph, and the factor of 2 accounts for separate buffers for incoming and outgoing data within each communication round. For MoE models, we have $2 \cdot r = 4$. This modest increase in memory usage eliminates the need for synchronization during one-sided data transfers. Figure 5.3 illustrates how cells within this symmetric tensor layout are indexed and used for Direct Memory Access (DMA) and Remote DMA (RDMA) operations. As Theorem 5.3.1 reinforces, this indexing scheme over L is the underlying mechanism that allows for fully non-blocking

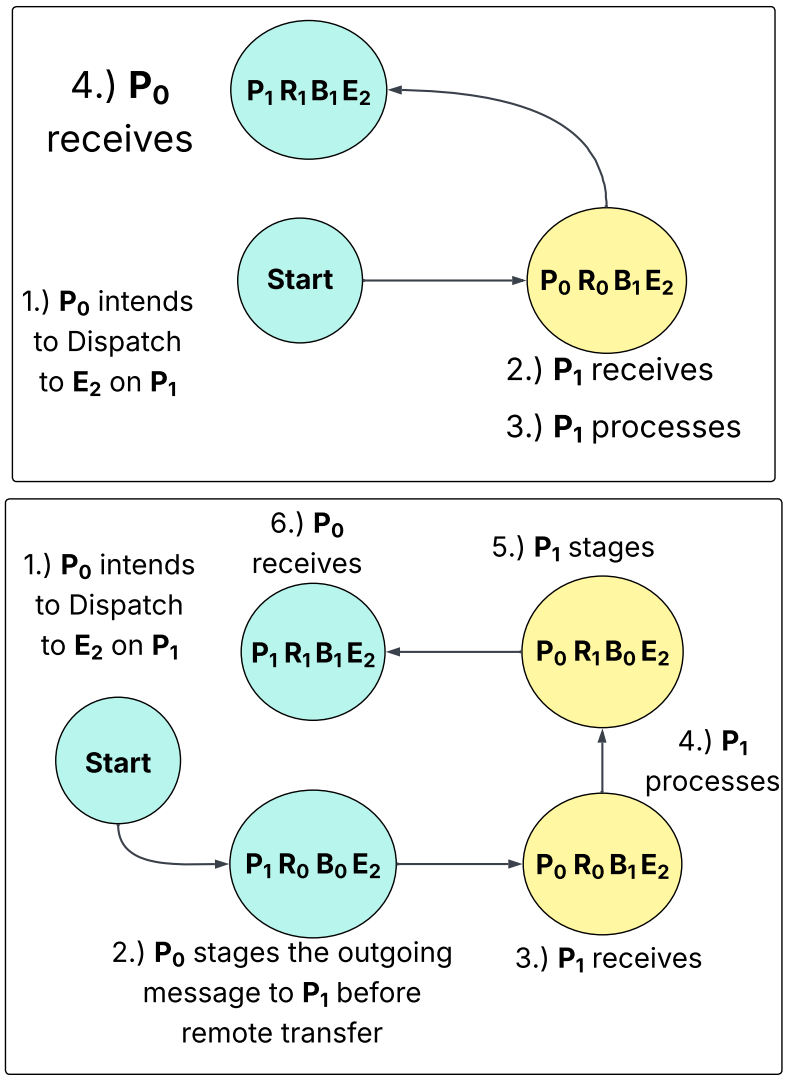


Figure 5.3: *State machine for DMA (top) and RDMA (bottom) communication.*

accesses eliding synchronization because all accesses are write *conflict-free*.

Definition 5.3.1. *Define a write as $w(p_s, p_t, i)$, where p_s is the source process and i is an ordered tuple indicating the index coordinates for L residing on the target process p_t. A write-write conflict occurs when there exist at least two distinct, un-synchronized, concurrent writes $w_1(p_{s_1}, p_{t_1}, i_1)$ and $w_2(p_{s_2}, p_{t_2}, i_2)$, such that $p_{t_1} = p_{t_2}$ and index coordinates $i_1 = i_2$ but $p_{s_1} \neq p_{s_2}$*

Definition 5.3.2. *For any source process p_s, a valid index coordinate $i = (p*, r, b, e, c)$ satisfies the following:*

1. *For inter-device writes, it must hold that* $p* = p_s$ *and* $b = 1$*. Note this also applies to self-looping writes* $w(p_t, p_t, i)$*.*
2. *For any write* $w(p_s, p_t, i)$*, if* $b = 0$*, then* $p_s = p_t$*. This rule describes intra-device staging writes.*

Theorem 5.3.1. *L is write-write conflict-free.*

Proof. As is the case for typical physical implementations, assume that each index coordinate i maps to a distinct memory segment in L. Next, we show by contradiction that no write-write conflicts can exist when accessing L using *valid* i. For simplicity, we only include the index coordinates when describing a write. Assume that there exist at least two writes $w_1(p_{s_1}, p_{t_1}, i_1)$, $w_2(p_{s_2}, p_{t_2}, i_2)$ with $p_{t_1} = p_{t_2}$ and valid destination coordinates i_1, i_2, where $i_1 = i_2$ lexicographically and both are unpacked below.

$$i_1 = (p_1, r_1, b_1, e_1, c_1),\ i_1 = (p_2, r_2, b_2, e_2, c_2)$$

Note that for the message staging state, even though $i_1 = i_2$ the resultant memory segments reside in different physical buffers resident in p_{s_1} and p_{s_2} respectively. Therefore, for this state, there are no conflicts as intra-process writes always have distinct c_j coordinates, where $j \in \{0, C-1\}$. For inter-process transfers, we have two cases.

Case 1: $p_{s_1} = p_{s_2}$

Here, w_1 and w_2 are identical operations. This contradicts the definition of a conflict, which requires that $p_{s_1} \neq p_{s_2}$. In practice, such repeat writes never even occur.

Case 2: $p_{s_1} \neq p_{s_2}$

To ensure validity for i_1 and i_2, it is the case that $p_1 = p_{s_1}$ and $p_2 = p_{s_2}$. However, this implies that $i_1 \neq i_2$ yielding a contradiction as desired. □

To construct L, we start from the original token buffer $T \in \mathbb{R}^{S \times H}$, where S is the sequence length and H is the hidden dimension. We first reorganize the sequence dimension S into three sub-dimensions representing the expert capacity (C), local expert slots (E), and the expert parallel world size (W), st:

$$C \cdot E \cdot W = C \cdot E' = S', \quad \text{where} \quad S' \geq S \text{ and } E' \geq E_W$$

In the typical case of uniform expert distribution (illustrated in Figure 5.2), we have $S' = S$ and $E' = E_W$, where E_W is the total number of experts in the model. Thus, the size of the token buffer is $Size(T) = S' \cdot H$. In Figure 5.2, each cell labeled E_i (with $i \in \{0, \ldots, 3\}$) is a matrix of size (C, H). Extending prior work [25, 55], we introduce additional temporal dimensions R (communication rounds) and B (staging buffers). Each communication round has two fixed staging slots: one for outgoing tokens and another for incoming tokens. Each slot, indexed by dimension P, forms a tensor of shape (S', H). Therefore, the tensor size $Size(L)$ is generally at least four times the original token buffer size, becoming exactly four times larger in the case of uniform expert distribution. Empirically (§6.7), we find:

$$Size(L) \approx 4 \cdot Size(T)$$

5.4 In-place Padding for Payload Efficiency

Due to the dynamic and uneven distribution of tokens in MoE dispatch [5], GPUs commonly receive fewer tokens than their predefined expert capacity.

Current MoE frameworks [41] typically pad these buffers with null tokens before computation, unnecessarily increasing communication payloads and degrading performance. In contrast, we propose *in-place padding*, performing padding directly within the local symmetric tensor buffers and thus eliminating excess network communication. As we show in Figure 5.2 as a reference, each cell E_i is sized according to the expert capacity C. We further align this capacity to ensure divisibility by the tile block size $bM = 128$, guaranteeing safe and aligned memory reads by Processor threads consuming remote tokens. This in-place padding strategy slightly increases the memory footprint of L, as described below:

$$Size(L) \approx \begin{cases} 4 \cdot Size(T), & \frac{S}{E} \geq bM \\ 4 \cdot \frac{bM \cdot E}{S} \cdot Size(T), & \text{otherwise} \end{cases}$$

CHAPTER 6

EVALUATION

Table 6.1: Implementation metrics of *FlashDMoE* using fully inlined NVSHMEM.

Metric	Value
Total lines of code (CUDA/C++)	6820
Kernel stack frame size	0 B
Spill stores (per thread)	0
Spill loads (per thread)	0
Shared memory usage (per block)	46 KB
Registers per thread	255
Max active blocks per SM	2
Compilation time	53 seconds
Binary size	29 MB

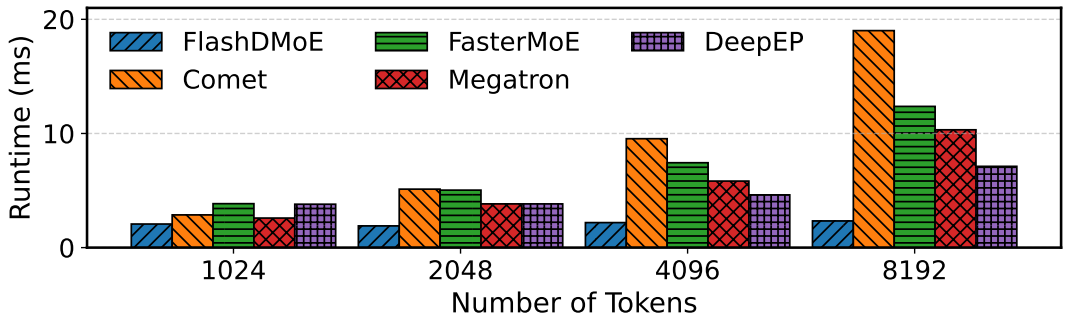
We implement (Table 6.1) and evaluate *FlashDMoE* by addressing two main questions: (1) Under what conditions does *FlashDMoE* outperform state-of-the-art MoE systems, and why (§6.2 - 6.5)? and (2) How much GPU memory does *FlashDMoE* require for core data structures (§6.7)?

6.1 Setup

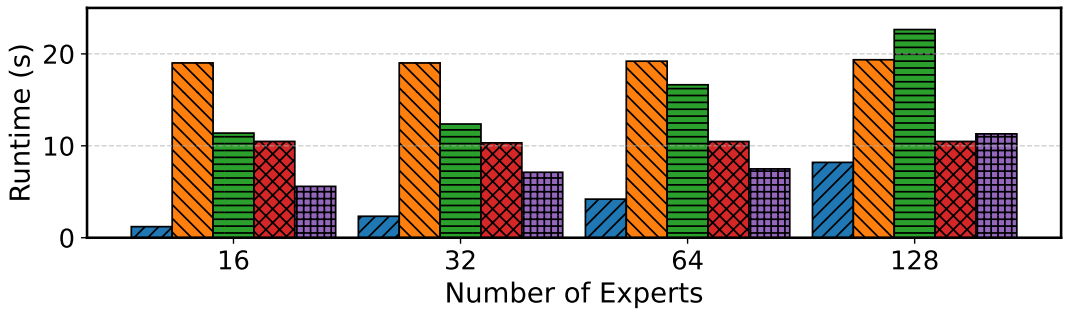
We run experiments on a RunPod server with 8 × NVIDIA H100 80G GPUs, 125 GB of RAM, and 20 vCPUs. We used PyTorch 2.6.0, CUDA 12.8, and Ubuntu 22.04. All experiments use MoE transformer models configured with 16 attention heads, an embedding dimension of 1024, and an FFN hidden size of 4096. We use top-2 routing with a capacity factor of 1.0. Note all baselines were evaluated using FP16 precision, while *FlashDMoE* was evaluated on FP32 precision, see §7 for more details. We compare *FlashDMoE* against several state-of-the-art MoE systems: (1) **Comet** [55], (2) **FasterMoE** [14], (3) **Megatron-LM** [31], and

(4) **DeepEP** [10]. Comet and DeepEP rely on NVSHMEM for communication, while FasterMoE and Megatron-LM use NCCL. We also evaluate *FlashDMoE* on a multi-node environment and discuss our findings in §6.6.

6.2 Scalability with Tokens and Experts



(a) Scaling with the number of tokens (E = 32).



(b) Scaling with the number of experts (T = 8K)

Figure 6.1: Scalability with respect to the number of tokens and experts. All experiments use 8 GPUs.

We first analyze the scalability of *FlashDMoE* in two dimensions: the number of input tokens and the number of experts. Figure 6.1 shows execution time for a single MoE layer on 8 GPUs. *FlashDMoE* outperforms baselines between **1.4X** to **9.5X** when scaling across sequence lengths and between **1.2X** to **15X** across

number of experts. We provide raw performance numbers in §6.8.

When scaling number of tokens (Fig. 6.1a), *FlashDMoE* maintains near-constant execution time (2.07 – 2.33 ms). In contrast, baselines incur significant runtime increases. For example, Comet's runtime grows from 2.9 ms to 19 ms, FasterMoE from 3.85 ms to 12.37 ms, Megatron-LM from 2.59 ms to 10.32 ms, and DeepEP from 3.80 ms to 7.12 ms. *FlashDMoE* avoids these overheads by overlapping computation and communication, achieving stable performance despite higher token counts. When scaling the number of experts (Figure 6.1b), *FlashDMoE*'s runtime increases proportionally from 1.12 ms to 8.20 ms, reflecting higher overhead from routing and processing additional experts. Comet and Megatron-LM exhibit relatively flat runtimes (around 19 ms and 10.4 ms, respectively) but at significantly higher latencies. FasterMoE (7.9–22.65 ms) and DeepEP (6.03–11.3 ms) show increasing runtimes due to overheads from inefficient communication or computation handling.

6.3 GPU Scalability

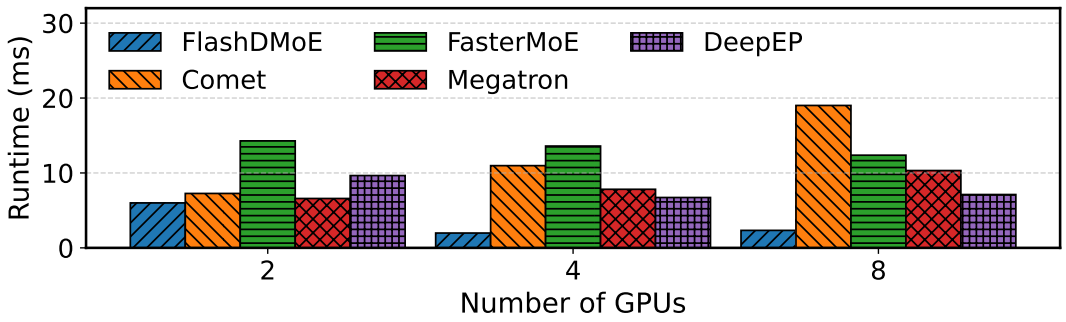
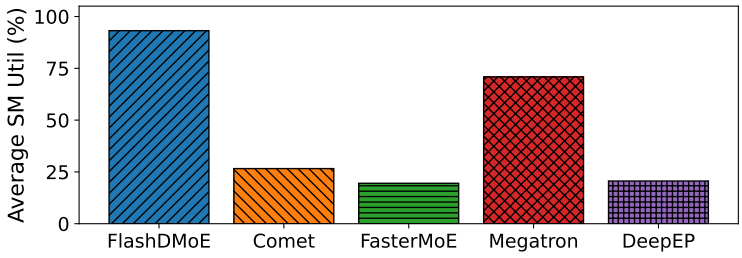


Figure 6.2: Scalability with respect to the number of GPUs (E = 32, T = 8K).

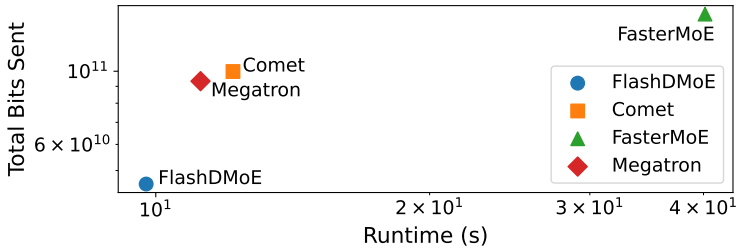
Figure 6.2 keeps tokens per GPU constant while scaling GPU count. *FlashD-*

MoE shows strong scalability, achieving a speedup from 5.99 ms (2 GPUs) to 1.98 ms (4 GPUs) and maintaining performance at 8 GPUs (2.33 ms). This highlights efficient inter-GPU communication and workload distribution. Comet and Megatron-LM degrade notably (Comet: 7.26–19.01 ms; Megatron-LM: 6.59–10.32 ms), indicating communication bottlenecks at scale. FasterMoE shows modest improvements (14.28–12.37 ms), and DeepEP displays a similar pattern to *FlashDMoE* (9.65–7.12 ms) but with consistently higher runtimes.

6.4 SM Utilization



(a) Comparison of SM utilization, defined as the ratio of cycles in which SMs have at least one warp in flight to the total number of cycles [35]. Values represent the average SM utilization over 100 iterations. All experiments use T = 8K and E = 64 on two GPUs.



(b) Payload efficiency. The y-axis shows the total number of bits transferred over NVLink with the same configuration. The x-axis shows the total layer execution time over 100 iterations. Both axes are log-scaled.

Figure 6.3: Factors leading to performance improvement of *FlashDMoE*.

Figure 6.3a shows GPU utilization, measured by the average SM utilization (fraction of GPU cycles with active warps [35]). *FlashDMoE* achieves over 90% SM utilization, showing effective fine-grained task scheduling and reduced idle GPU time.

6.5 Payload Efficiency

We next evaluate payload efficiency (Figure 6.3b) by measuring the volume of data transferred over NVLink. Traditional MoE frameworks communicate zero-padded tokens, inflating network payloads. In contrast, *FlashDMoE*'s in-place padding approach transmits only active tokens, reducing communication volume substantially and resulting in better runtime performance.

6.6 Multi-Node Evaluation

6.6.1 Setup

In this experiment, we seek to evaluate *FlashDMoE* in the multi-node setting. We use 4 nodes, where each node comprises 4 A100 GPUs fully interconnected via NVLink. Across nodes, each GPU uses a single NIC providing 25 GB/s of bandwidth. We set the number of experts to be 16 and assign each GPU to host only one, so the number of local experts is 1. Note that we define MIV formally as follows:

$$MIV = \frac{Tokens}{Experts} * local\_experts * precision * hidden\_size * 2 * n_{rg}$$

where n_{rg} is the number of remote peers and the multiplicative factor of 2 accounts for communication rounds (dispatch and combine). $n_{rg} = 12$ for this experiment.

6.6.2 Results

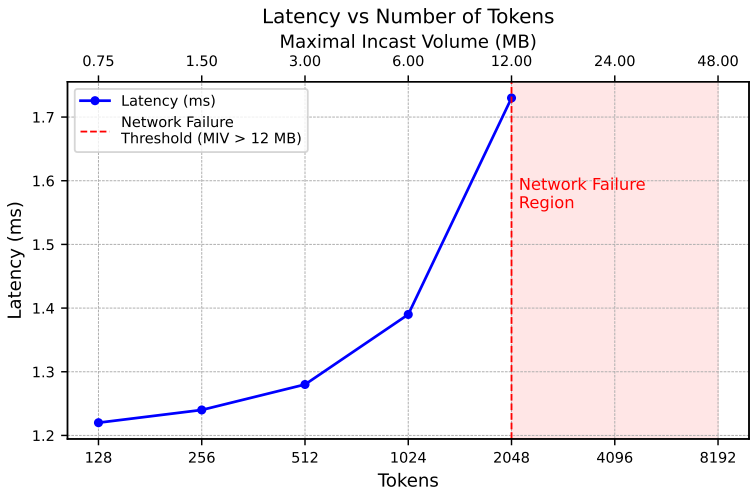


Figure 6.4: Multi-node Latency evaluation. Embbeding dimension is 1024 and FFN intermediate size is 4096. We define Maximal Incast Volume (MIV) as the worst case upper bound for data volume that a NIC receives in a single incast occurence.

We observe a sublinear increase in latency as we scale the number of tokens. However, we observe at $Tokens > 2048$, that the application fails to terminate due to failure to receive expectant messages. We hypothesize this failure to be due to buffer overflow at the networking hardware layer as is common for applications that generate many and large messages [33] like our system. We note that this failure is addressable by tuning hardware configurations [13] but we consider this exploration as an exercise orthogonal to this work.

6.7 Memory Overhead

We measure the GPU memory required for the symmetric tensor L and runtime bookkeeping state of *FlashDMoE*. Memory overhead depends primarily on the tile size, expert capacity (EC), and the number of experts (E). Table 6.2 summarizes memory overhead under various configurations, confirming that *FlashDMoE* maintains a modest and predictable memory footprint.

Table 6.2: Memory overhead (tile size $bM = 128$, $Size(T) = \text{Tokens} * 4KB$).

Tokens	Experts	EC	max(bM, EC)	Bookkeeping (MB)	$Size(L)$ (MB)	Total (MB)
4K	16	256	256	64.57	64.00	128.57
4K	32	128	128	64.55	64.00	128.55
4K	64	64	128	128.90	128.01	256.91
4K	128	32	128	257.96	256.02	513.98
8K	16	512	512	128.95	128.01	256.95
8K	32	256	256	128.90	128.01	256.91
8K	64	128	128	128.90	128.01	256.91
8K	128	64	128	258.15	256.02	514.17
16K	16	1024	1024	257.89	256.02	513.90
16K	32	512	512	257.79	256.02	513.81
16K	64	256	256	257.80	256.02	513.81
16K	128	128	128	258.53	256.02	514.54

6.8 Numerical Data

Table 6.3: Latency (ms) comparison across different numbers of tokens (Figure 6.1a).

Tokens	FlashDMoE	Comet	FasterMoE	Megatron	DeepEP
1024	2.07	2.87	3.85	2.59	3.80
2048	1.90	5.12	5.04	3.83	3.83
4096	2.19	9.54	7.44	5.83	4.62
8192	2.33	19.01	12.37	10.32	7.12

Table 6.4: Latency (ms) comparison across different numbers of experts (Figure 6.1b).

Experts	FlashDMoE	Comet	FasterMoE	Megatron	DeepEP
16	1.20	19.01	11.38	10.47	5.59
32	2.33	19.01	12.37	10.32	7.12
64	4.20	19.21	16.64	10.47	7.49
128	8.20	19.36	22.65	10.47	11.30

Table 6.5: Latency (ms) comparison across different numbers of GPUs (Figure 6.2).

GPUs	FlashDMoE	Comet	FasterMoE	Megatron	DeepEP
2	6.00	7.26	14.28	6.59	9.65
4	1.98	10.98	13.59	7.82	6.72
8	2.33	19.01	12.37	10.32	7.12

CHAPTER 7

LIMITATIONS AND FUTURE WORK

Despite the performance gains and architectural innovations of *FlashDMoE*, there are several limitations worth acknowledging—both practical and conceptual—that open the door to future research.

- **Programming complexity.** Developing fully fused, persistent kernels is a non-trivial engineering task. While *FlashDMoE* proves the feasibility and benefit of such kernels, their construction demands deep expertise in GPU architectures, synchronization and distributed protocols, and memory hierarchies. This high barrier to entry limits adoption. Future work may consider compiler-level abstractions or DSLs to democratize this technique.
- **FP16 support and shared memory bank conflicts.** Although modern GPUs natively support half-precision computation, adapting FLASHDMOE to FP16 is non-trivial for the Processor's computational operators. Specifically, our manually tuned swizzle shared memory layouts are not the most efficient template parameters for CUTLASS' Collective Mainloop operator which we use to implement our in-device GEMMs. This suboptimal configuration degrades memory throughput as shown in §A. Overcoming this for Ampere GPUs and below would require careful investigation of optimal layouts, but for Hopper GPUs and above, we anticipate using the builder interface that CUTLASS provides in our future improvements.
- **Lack of backward pass and training support.** While this work focuses on inference, enabling training requires fusing backward computation and

gradient communication into the kernel. Supporting this entails non-trivial changes to both memory bookkeeping and task descriptor definitions. Nevertheless, it remains an exciting direction for extending this system to fully support end-to-end training.

CHAPTER 8

CONCLUSION

This thesis introduces *FlashDMoE*, the first system to fuse the entire Mixture-of-Experts (MoE) operator into a single, persistent GPU kernel. We show that prevailing MoE implementations suffer from two critical inefficiencies: (1) CPU-managed synchronous communication that leads to underutilized interconnects and (2) fragmented execution via multiple GPU kernels, introducing overhead and synchronization delays.

In contrast, *FlashDMoE* embraces a model of GPU autonomy by embedding computation, communication, and scheduling within a unified kernel. It leverages actor-style concurrency, warp specialization, and asynchronous (R)DMA to achieve fine-grained communication–computation overlap.

Our evaluation demonstrates up to **15× speedup** over state-of-the-art systems, up to **4**× improved GPU utilization, and greater payload efficiency, especially in dynamic workloads like MoE. *FlashDMoE* challenges the dominant execution paradigms in distributed deep learning and presents a compelling template for building future GPU-native systems.

While several limitations remain—including programming complexity and lack of FP16 support—this work lays the groundwork for a new era of *in-kernel distributed computation*. Future systems may build upon this foundation to enable kernel fusion for entire training pipelines, ushering in a design shift from CPU orchestration to **fully autonomous GPU execution**.

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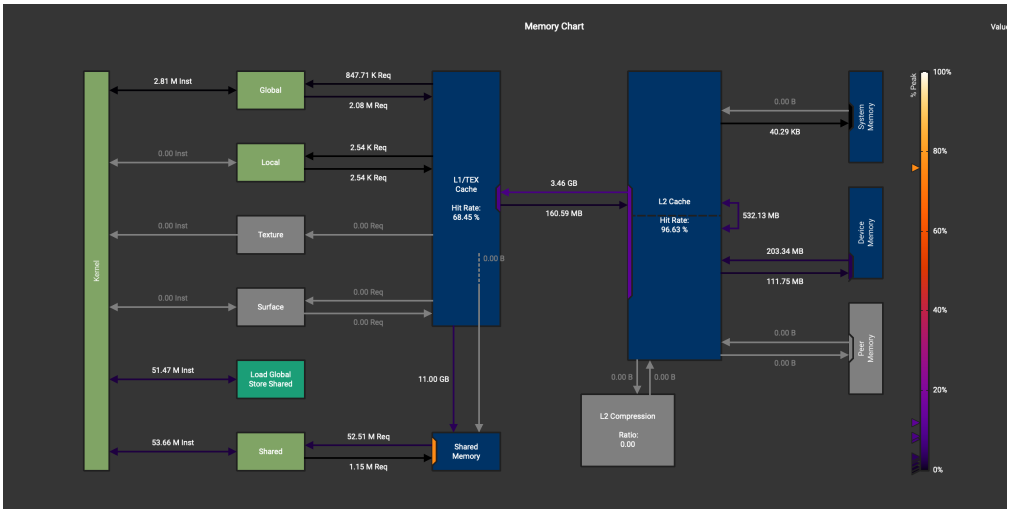
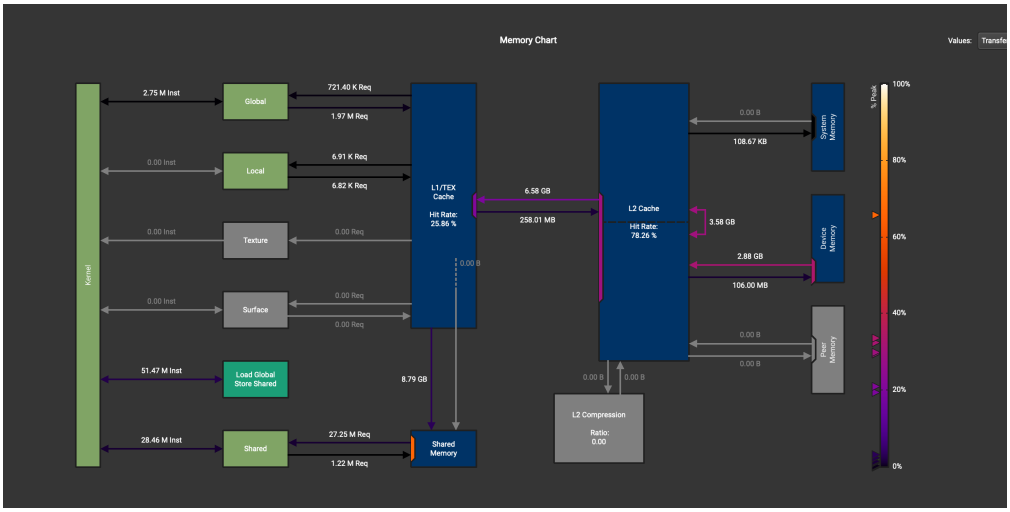
APPENDIX A

FP16 MEMORY THROUGHPUT



(a) Memory subsystem throughput for FP16



(b) Memory subsystem throughput for FP32

Figure A.1: Here, we report the total GPU memory throughput for both FP16 (top) and FP32 (bottom) variants of *FlashDMoE*. Notably, the FP16 implementation issues approximately 2× more shared memory instructions compared to its FP32 counterpart under identical workloads. We attribute this inefficiency to suboptimal shared memory layouts in *FlashDMoE* when operating on half-precision data. While this bottleneck is addressable through improved layout strategies, we leave its resolution to future work due to time constraints.