IC Design LAB Report

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1 Area/Time/Power Report:

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1
2 ****************************************
3 Report : timing
4          -path full
5          -delay max
6          -max_paths 1
7 Design : alu
8 Version: R-2020.09-SP5
9 Date   : Tue Mar  8 23:26:53 2022
10 ****************************************
11
12 Operating Conditions: WCCOM   Library: fsa0m_a_generic_core_ss1p62v125c
13 Wire Load Model Mode: enclosed
14
15   Startpoint: reg_data_a_reg[0]
16               (rising edge-triggered flip-flop clocked by clk_p_i)
17   Endpoint: ALU_d2_r_reg[14]
18             (rising edge-triggered flip-flop clocked by clk_p_i)
19   Path Group: clk_p_i
20   Path Type: max
21
22   Des/Clust/Port     Wire Load Model       Library
23   ------------------------------------------------
24   alu                G200K                 fsa0m_a_generic_core_tt1p8v25c
25   alu_DW_mult_uns_0  enG5K                 fsa0m_a_generic_core_tt1p8v25c
26
27   Point                                                   Incr       Path
28   ---------------------------------------------------------------------------
29   clock clk_p_i (rise edge)                               0.00       0.00
30   clock network delay (ideal)                             0.50       0.50
31   reg_data_a_reg[0]/CK (QDFFRBN)                          0.00       0.50 r
32   reg_data_a_reg[0]/Q (QDFFRBN)                           0.53       1.03 r
33   mult_41/a[0] (alu_DW_mult_uns_0)                        0.00       1.03 r
34   mult_41/U165/O (INV1S)                                  0.21       1.23 f
35   mult_41/U140/O (INV1S)                                  0.11       1.35 r
36   mult_41/U141/O (INV1S)                                  0.30       1.65 f
37   mult_41/U179/O (NR2)                                    0.24       1.89 r
38   mult_41/U53/S (FA1S)                                    0.42       2.30 f
39   mult_41/U52/S (FA1S)                                    0.39       2.70 f
40   mult_41/U12/CO (FA1S)                                   0.42       3.12 f
41   mult_41/U11/CO (FA1S)                                   0.40       3.52 f
42   mult_41/U10/CO (FA1S)                                   0.40       3.92 f
43   mult_41/U9/CO (FA1S)                                    0.40       4.31 f
44   mult_41/U8/CO (FA1S)                                    0.40       4.71 f
45   mult_41/U7/CO (FA1S)                                    0.40       5.11 f
46   mult_41/U6/CO (FA1S)                                    0.40       5.51 f
47   mult_41/U5/CO (FA1S)                                    0.40       5.91 f
48   mult_41/U4/CO (FA1S)                                    0.40       6.31 f
49   mult_41/U3/CO (FA1S)                                    0.40       6.70 f
50   mult_41/U2/S (FA1S)                                     0.53       7.24 r
51   mult_41/product[14] (alu_DW_mult_uns_0)                 0.00       7.24 r
52   U203/O (AOI22S)                                         0.12       7.36 f
53   U202/O (ND3)                                            0.18       7.53 r
54   ALU_d2_r_reg[14]/D (QDFFRBT)                            0.00       7.53 r
55   data arrival time                                                  7.53
56
57   clock clk_p_i (rise edge)                              10.00      10.00
58   clock network delay (ideal)                             0.50      10.50
59   clock uncertainty                                      -0.10      10.40
60   ALU_d2_r_reg[14]/CK (QDFFRBT)                           0.00      10.40 r
61   library setup time                                     -0.10      10.30
62   data required time                                                10.30
63   ---------------------------------------------------------------------------
64   data required time                                                10.30
65   data arrival time                                                 -7.53
66   ---------------------------------------------------------------------------
67   slack (MET)                                                        2.77
68
69
70 1
```

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****************************************
Report : area
Design : alu
Version: R-2020.09-SP5
Date   : Tue Mar  8 23:24:03 2022
****************************************

Library(s) Used:

    fsa0m_a_generic_core_tt1p8v25c (File: /home/raid7_2/userb08/b8502141/HW3/fsa0m_a_generic_core_tt1p8v25c.db)

Number of ports:                          130
Number of nets:                           579
Number of cells:                          401
Number of combinational cells:            363
Number of sequential cells:                35
Number of macros/black boxes:               0
Number of buf/inv:                         98
Number of references:                      26

Combinational area:               7533.892821
Buf/Inv area:                      656.207993
Noncombinational area:            2227.982376
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (Wire load has zero net area)

Total cell area:                  9761.875197
Total area:                 undefined
1
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```
Loading db file '/home/raid7_2/userb08/b8502141/HW3/fsa0m_a_generic_core_tt1p8v25c.db'
Information: Propagating switching activity (low effort zero delay simulation). (PWR-6)
Warning: Design has unannotated primary inputs. (PWR-414)
Warning: Design has unannotated sequential cell outputs. (PWR-415)

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Report : power
        -analysis_effort low
Design : alu
Version: R-2020.09-SP5
Date   : Tue Mar  8 23:25:22 2022
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Library(s) Used:

    fsa0m_a_generic_core_tt1p8v25c (File: /home/raid7_2/userb08/b8502141/HW3/fsa0m_a_generic_core_tt1p8v25c.db)


Operating Conditions: WCCOM   Library: fsa0m_a_generic_core_ss1p62v125c
Wire Load Model Mode: enclosed

Design        Wire Load Model            Library
------------------------------------------------
alu                    G200K             fsa0m_a_generic_core_tt1p8v25c
alu_DW01_sub_0         enG5K             fsa0m_a_generic_core_tt1p8v25c
alu_DW01_add_0         enG5K             fsa0m_a_generic_core_tt1p8v25c
alu_DW_mult_uns_0      enG5K             fsa0m_a_generic_core_tt1p8v25c


Global Operating Voltage = 1.62
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  = 287.5571 uW   (47%)
  Net Switching Power  = 322.3782 uW   (53%)
                         ---------
Total Dynamic Power    = 609.9352 uW  (100%)

Cell Leakage Power     =  33.7987 nW


                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000              0.0000            0.0000  (   0.00%)
memory             0.0000           0.0000              0.0000            0.0000  (   0.00%)
black_box          0.0000           0.0000              0.0000            0.0000  (   0.00%)
clock_network      0.0000           0.0000              0.0000            0.0000  (   0.00%)
register           0.2131           0.2340          9.1773e+03            0.4471  (  73.30%)
sequential         0.0000           0.0000              0.0000            0.0000  (   0.00%)
combinational  7.4493e-02        8.8369e-02          2.4621e+04            0.1629  (  26.70%)
--------------------------------------------------------------------------------------------------
Total              0.2876 mW        0.3224 mW       3.3799e+04 pW         0.6100 mW
1
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2 Discussion:

Timing: The slack in my design is positive. It's quite cool.
Power: It seems to be a very power-saved chip, and its power is consumed mostly by the registers.
Area: It does not consume a lot of area, obviously. Most on the combinational area.