IC Design Lab

HW 3 Synthesis

- Due on 03/10/2022, 23:59 , 10% penalty for each day of delay
- If you have any questions, please contact r10943003@ntu.edu.tw, and specify [ICDLab] before your title

I. Objectives

In this homework, you will practice synthesizing a design by using design compiler.

II. Design Files

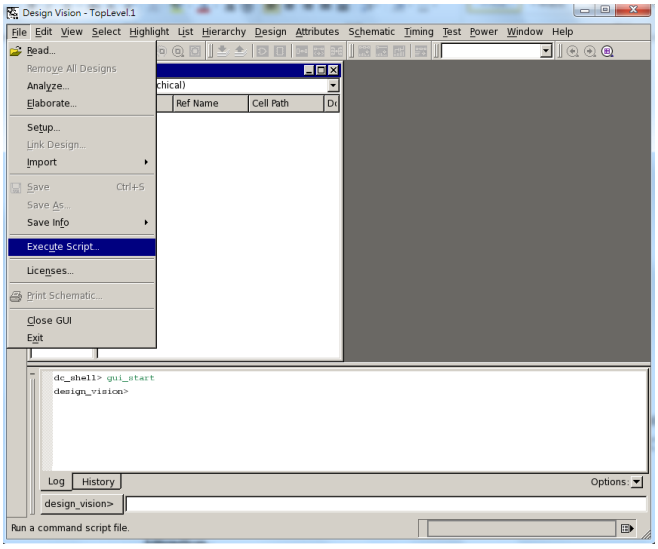
Copy files from course website and check if you have these files：

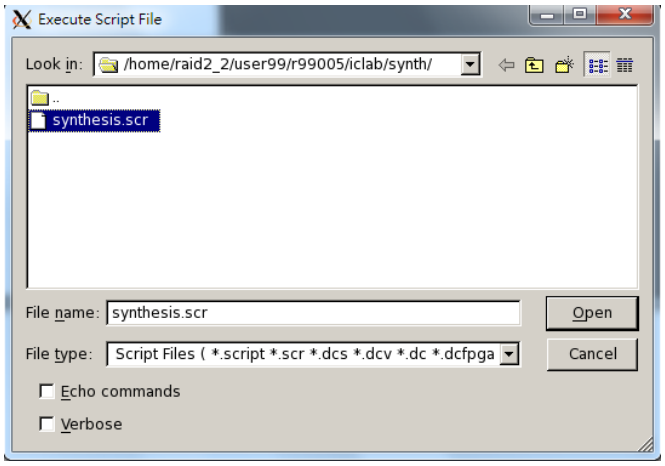
1. Some .db files
2. fsa0m_a_generic_core_21.lib.src
3. HW3_alu_tb.v
4. HW1_alu.v
5. synthesis.scr(or .tcl)
6. .synopsys_dc.setup

III. Specifications

In this homework, you should synthesize your design in HW1 using the commands taught in the course. The file name of your HW1 design should be “HW1_alu.v”. Port names and port order should be the same in HW1. Top module name should be “alu”. You can refer to the procedures in Lab 3.

The way of executing a script file in DC is shown below:





Latches are not allowed in your design. **The slack should be non-negative**. If your design cannot be synthesized, please check if there is some non-synthesizable syntax in your code and fix them.

Your score will be evaluated by whether your gate-level design passes gate-level simulation or not. You can use HW3_alu_tb.v to do gate-level simulation yourself.

IV. Attention

1. Plagiarism is not allowed.
2. Design file: HW3_alu_syn.v, HW3_alu.sdf and HW3_alu.sdc

V. Grading

1. Design Files :
   HW3_alu_syn.v , HW3_alu.sdf and HW3_alu.sdc (70%)
2. Report
   2.1 Area, timing and power report (15%)
   2.2 Discussion (15%): Discuss about the 3 reports mentioned above.

VI. Notification

1. You should compress your design files into a single ZIP file, and then upload your ZIP file to ceiba before 2022/03/10 23:59

Files should be compressed as follows:

ICDLAB_HW3_StudentID.zip

- ICDLAB_HW3_StudentID
  - HW3_alu_syn.v
  - HW3_alu.sdf
  - HW3_alu.sdc
  - StudentID_HW3.pdf

Examples:

ICDLAB_HW3_r10943003.zip

- ICDLAB_HW3_r10943003
  - HW3_alu_syn.v
  - HW3_alu.sdf
  - HW3_alu.sdc
  - r10943003_HW3.pdf