IC Design Lab

HW4 Place & Route

- Due on 03/17/2022, 23:59 AM in class, 10% penalty for each day of delay
- If you have any questions, please contact r10943003@ntu.edu.tw , and specify [ICDLab] before your title

I. Objective

In this homework, you will practice using Innovus to do automatic place and route.

II. Design Files

1. Your gate-level verilog code from the previous homework (For example, HW3_alu_syn.v)or CHIP_syn.v from Lab4
2. The technology files provided in the Lab4.

III. Specification

In this homework, you should use Innovus to do P&R using CHIP_syn.v offered by Lab4 or your design in HW3.

Note that if you want to use your hw3 code , you should re-synthesize your HW1_alu.v by UMC library. You should download Synthesis(UMC18).rar and use Design Compiler to do HW3 again (very simple)

The file name of your HW3 design should be “CHIP_syn.v”. Port names and port order should be the same in HW3. Top module name should be “CHIP”. You can refer to the procedures in Lab 4.

Note that the CHIP.ioc and CHIP.sdc are not provided to you. You should write them by yourself.

IV. Grading

1. Electronic submission: (70%)
   HW4.gds, HW4.sdf, HW4_post_layout.v.
2. Report:
   2.1 Your final layout figure **before** adding dummy metals and the message of no violation in the core area. (15%)
   2.2 Discussion: (15%)
   You can change different core utilization, power ring and stripe, SDC constraints, IO positions, etc. Discuss how these parameters affects your layout.

V. Notification

Files should be compressed as follows:

ICDLAB_HW4_StudentID.zip

- ICDLAB_HW4_StudentID
  - HW4.gds
  - HW4.sdf
  - HW4_post_layout.v
  - StudentID_HW4.pdf

Examples:

ICDLAB_HW4_r10943003.zip

- ICDLAB_HW4_r10943003
  - HW4.gds
  - HW4.sdf
  - HW4_post_layout.v
  - r10943003_HW4.pdf

<補充>

如果有下面跟 PAD 有關的 violation(X)，可以先忽略沒關係!
只要 Core area 裡面的電路是沒有 violation 即可。

當然若 violation 消不掉，以盡量消為主，並把你們怎麼解決 violation 的方式寫在報告中。