IC Design Lab

HW5 Post-Layout Verification

- Due on 03/24/2022, 23:59, 10% penalty for each day of delay
- If you have any questions, please contact r10943003@ntu.edu.tw , and specify [ICDLab] before your title

I. Objective

In this homework, you will practice all the post-layout verification procedure by Calibre and the post-layout simulation by NC-verilog.

II. Prepared Files

The layout file	CHIP.gds
The netlist file after P&R	CHIP.v
The timing file for post-layout gate-level simulation	CHIP.SDF

These files are from the APR tool (SOCE).

III. Specification

In the post-layout verification part, you should verify your layout form HW5 by Calibre DRC, LVS. After all verifications have done, you should run post-layout gate-level simulation by NC-verilog.

IV. Grading

1. Electronic submission: (80%)

P&R layout file	CHIP.gds	10%
DRC report file	DRC.rep	20%
LVS report file	lvs.rep	20%
Post-layout Gate-level simulation files and **function correctness**	CHIP.v	30%
	CHIP.SDF	

Note that : DRC.rep is renamed file form QA_pass.sum which is generated by Lab5_DRC.

2. Discussion: (20%)

You can make some discussion about the post-layout verification, including Calibre DRC, LVS, and the post-layout simulation by NC-verilog. You can discuss about the problems you met when you are doing the post-layout verification and the methods that you solve them.

V. Notification

Files should be compressed as follows:

ICDLAB_HW5_StudentID.zip

- ICDLAB_HW5_StudentID
  - CHIP.gds
  - DRC.rep
  - lvs.rep
  - CHIP.v
  - CHIP.SDF
  - StudentID_HW5.pdf

Examples:

ICDLAB_HW5_r10943003.zip

- ICDLAB_HW5_r10943003
  - CHIP.gds
  - DRC.rep
  - lvs.rep
  - CHIP.v
  - CHIP.SDF
  - r10943003_HW5.pdf