

```
# Loading work.lab01_vlg_vec_tst
# Loading work.lab01
# Loading cycloneiv_ver.cycloneiv_io_obuf
# Loading cycloneiv_ver.cycloneiv_io_ibuf
# Loading cycloneiv_ver.cycloneiv_lcell_comb
# Loading work.lab01_vlg_sample_tst
# Loading work.lab01_vlg_check_tst
# Simulation passed !
# ** Note: $finish      : lab01.vt(150)
#   Time: 1 us  Iteration: 0  Instance: /lab01_vlg_vec_tst/th_out
*****
Running quartus vcd_to_vwf
>> quartus_sim --tcl_eval convert_vector -format vwf
      ation/qsim/lab01.msim.vcd}
PID = 16084
Vector file lab01.msim.vwf is saved in text format.
it into Compressed Vector Waveform File format in o
le size
Vector conversion from lab01.msim.vcd to lab01.msim.
```

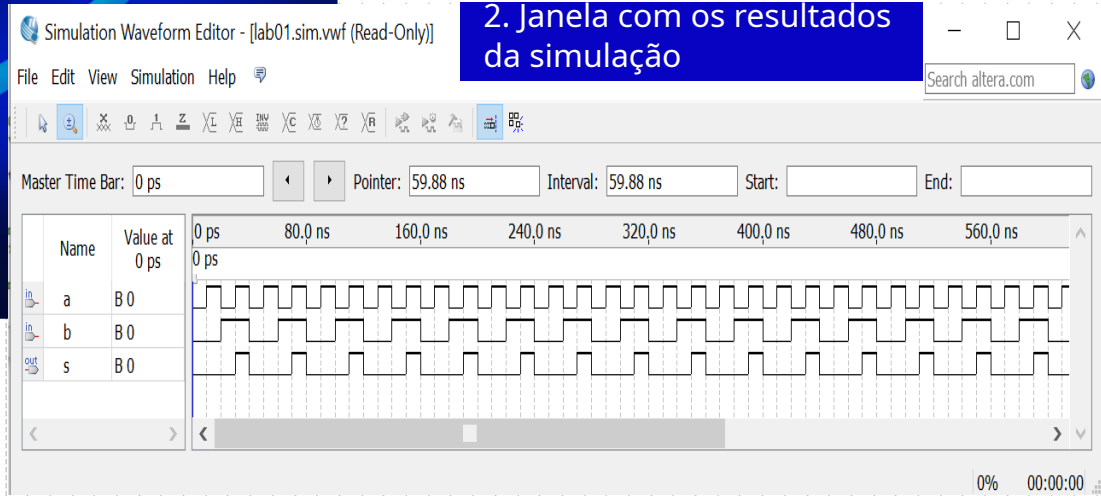
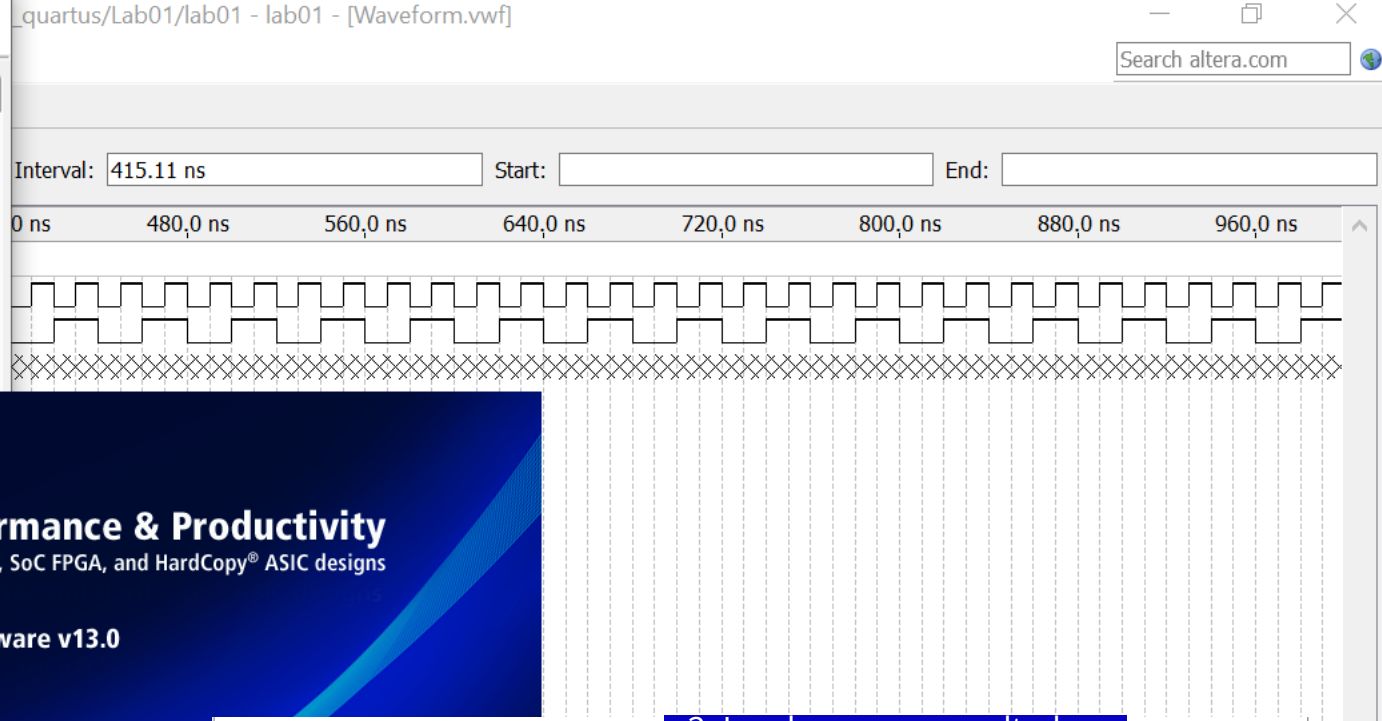
Converting ModelSim output .vcd to .vwf

1. Verificar a inexistência de erros

**# 1 in Performance & Productivity**  
for CPLD, FPGA, SoC FPGA, and HardCopy® ASIC designs

**Design Software v13.0**

**ALTERA**  
MEASURABLE ADVANTAGE™



2. Janela com os resultados da simulação