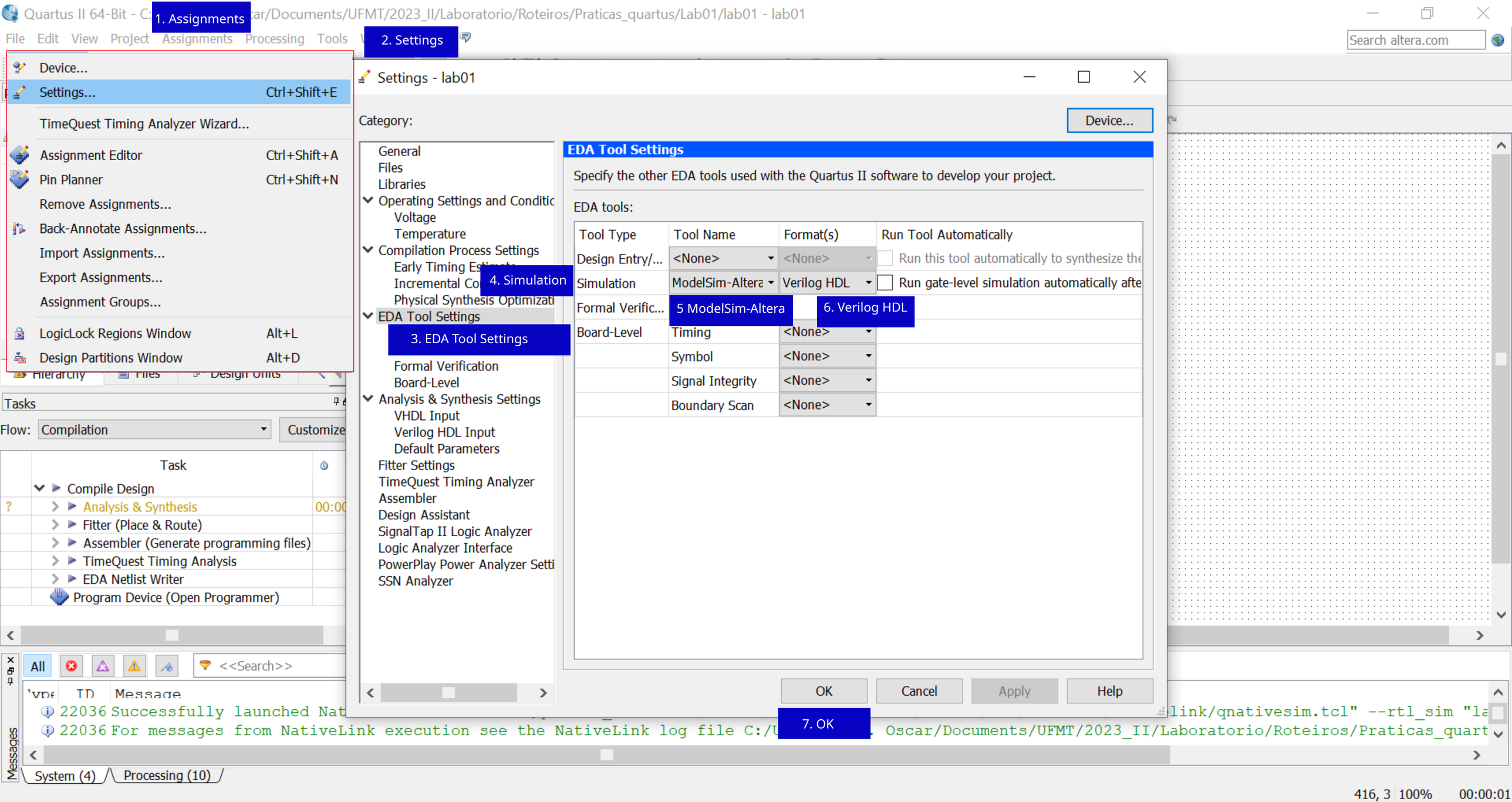
1. Assignments
2. Settings
Quartus II 64-Bit - C:/Users/Oscar/Documents/UFMT/2023_II/Laboratorio/Roteiros/Praticas_quartus/Lab01/lab01 - lab01
File Edit View Project Assignments Processing Tools
Search altera.com
Device...
Settings... Ctrl+Shift+E
TimeQuest Timing Analyzer Wizard...
Assignment Editor Ctrl+Shift+A
Pin Planner Ctrl+Shift+N
Remove Assignments...
Back-Annotate Assignments...
Import Assignments...
Export Assignments...
Assignment Groups...
LogicLock Regions Window Alt+L
Design Partitions Window Alt+D
Settings - lab01
Category:
Device...
General
Files
Libraries
Operating Settings and Conditic
Voltage
Temperature
Compilation Process Settings
Early Timing Estimate
Incremental Co
Physical Synthesis Optimizati
EDA Tool Settings
Formal Verification
Board-Level
Analysis & Synthesis Settings
VHDL Input
Verilog HDL Input
Default Parameters
Fitter Settings
TimeQuest Timing Analyzer
Assembler
Design Assistant
SignalTap II Logic Analyzer
Logic Analyzer Interface
PowerPlay Power Analyzer Setti
SSN Analyzer
4. Simulation
3. EDA Tool Settings
EDA Tool Settings
Specify the other EDA tools used with the Quartus II software to develop your project.
EDA tools:
Tool Type
Tool Name
Format(s)
Run Tool Automatically
Design Entry/...
<None>
Run this tool automatically to synthesize the
Simulation
ModelSim-Altera
Verilog HDL
Run gate-level simulation automatically afte
Formal Verific...
Board-Level
Timing
Symbol
Signal Integrity
Boundary Scan
5 ModelSim-Altera
6. Verilog HDL
OK
Cancel
Apply
Help
7. OK
Tasks
Flow: Compilation
Customize
Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programming files)
TimeQuest Timing Analysis
EDA Netlist Writer
Program Device (Open Programmer)
All
<<Search>>
Message
22036 Successfully launched Nat
22036 For messages from NativeLink execution see the NativeLink log file C:/U
link/qnativesim.tcl" --rtl_sim "la
Oscar/Documents/UFMT/2023_II/Laboratorio/Roteiros/Praticas_quart
Messages
System (4)
Processing (10)
416, 3 100% 00:00:01