

Quartus II 64-Bit

File Edit View Project Assignments Processing Tools Window Help

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Project Navigator

Compilation Hierarchy

Hierarchy Files Design Units

Tasks

Flow: Compilation Customize...

Task	Time
Compile Design	
Analysis & Synthesis	
Fitter (Place & Route)	
Assembler (Generate programming files)	
TimeQuest Timing Analysis	
EDA Netlist Writer	
Program Device (Open Programmer)	

Messages

System Processing

New Project Wizard

Summary [page 5 of 5]

When you click Finish, the project will be created with the following settings:

Project directory:

C:/Users/Prof. Oscar/Documents/UFMT/2023_II/Laboratorio/Roteiros/Praticas_quartus/Lab02

Local de trabalho no computador

Project name:

lab02

Nome do projeto

Top-level design entity:

lab02

Number of files added:

0

Number of user libraries added:

0

Device assignments:

Family name:

Cyclone IV GX

Plataforma computacional (não interessa para SD)

Device:

EP4CGX15BF14A7

EDA tools:

Design entry/synthesis:

<None> (<None>)

Simulation:

ModelSim-Altera (Verilog HDL)

Ferramentas de simulação

Timing analysis:

()

Operating conditions:

Core voltage:

n/a

Junction temperature range:

n/a

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