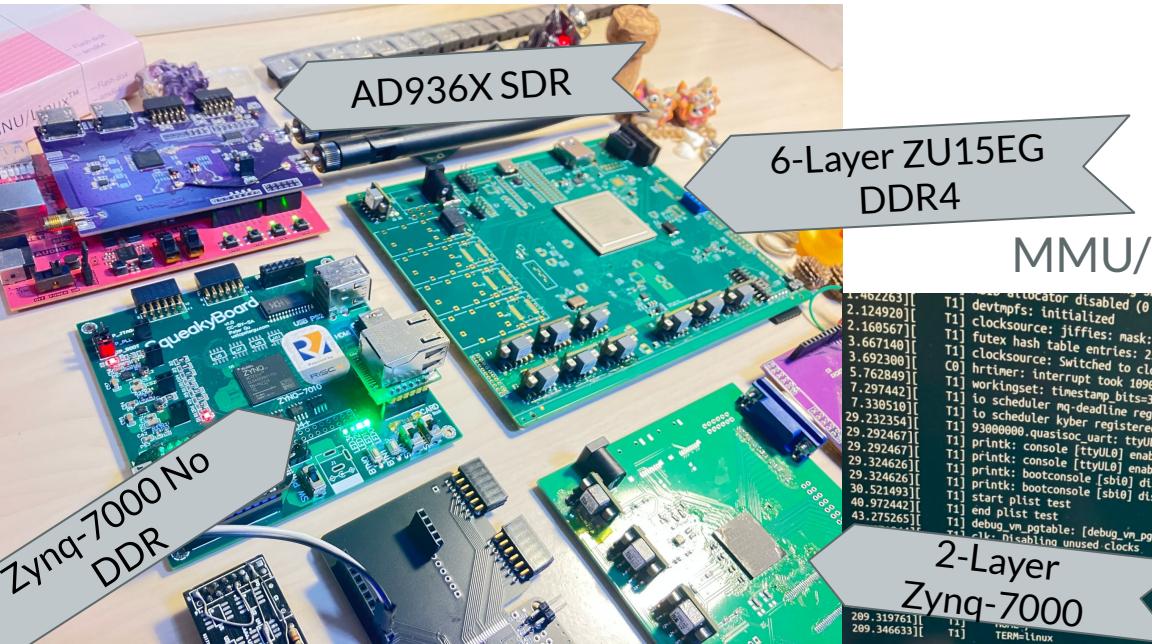


All Open Source Toolchain for ZYNQ 7000 SoCs

Yimin Gu, Hans Baier, Angelo Jacobo, Edmund Humenberger
Symbiotic EDA
OSCAR 2025

About Me

- PhD candidate @ U-Tokyo
- Amateur FPGA programming, RISC-V, PCB design, ZYNQ, Maker Faire, etc



```
1.462263[[  
2.124920[[  
2.168567[[  
3.667140[[  
3.692300[[  
5.762849[[  
7.297442[[  
7.330518[[  
29.232354[[  
29.292467[[  
29.292467[[  
29.324626[[  
29.324626[[  
30.521493[[  
48.972442[[  
43.275265[[  
T1] allocator disabled (0 bits)  
T1] devtmpfs: initialized  
T1] clocksource: jiffies: mask: 0xffffffff max_cycles: 0xffffffff,  
T1] futex hash table entries: 256 (order: 0, 7168 bytes, linein)  
C0] clocksource: Switched to clocksource riscv_clocksource  
hrtimer: interrupt took 10998890 ns  
T1] workingset: timestamp_bits=30 max_order=14 bucket_order=8  
T1] to scheduler mq-deadline registered  
T1] to scheduler kyber registered  
T1] 93000000. quasimodo_start: ttyUL0 at MMIO 0x93000000 (irq = 0, base_ba  
T1] printk: console [ttyUL0] enabled  
T1] printk: console [ttyUL0] enabled  
T1] printk: bootconsole [sbi0] disabled  
T1] printk: bootconsole [sbi0] disabled  
T1] start plist test  
T1] end plist test  
T1] debug_vn_pgtable: [debug_vn_pgtable  
T1] -t b- Disabling unused clocks  
]: Validating architecture  
en) memory: 5844K
```

Hackers & Painters



I'm neither



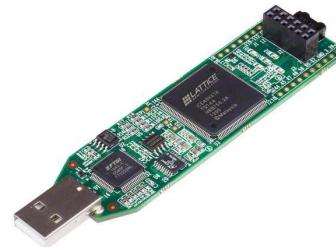
Table of Contents

- Open-source FPGA toolchains
- Now Zynq (demo)
- What does this mean
- Future

Open-source FPGA Toolchains

From iCE40 to Kintex 7

- Icestorm for Lattice iCE40, in 2015
- PrjTrellis for Lattice ECP5
- Project Apicula 🐝 for Gowin
- F4PGA for Xilinx 7 Series
- OpenXC7 supports Kintex 7
- ice40hx8k, 8K LE
- lfe5u-85f, 85K LE
- gw2ar, 20K LE
- xc7a200t, 200K LE
- xc7k480t, 480K LE



Possibilities

- PicoRV32, UberDDR3, Quasi SoC (No-MMU), KianRiscV, SD Card, HDMI, MMCM, IOSERDES
- Spartan 7/Artix 7/Kintex 7, Zynq 7000 PL, GTP, Artix 7 PCIe
- SATA controller, 10G ETH, GTX, PCIe Root Complex softcore

Runs on ARM Machines
(Apple M1 included)

Runs in Docker



Hans Baier @hansfbaiер@fosstodon.org
@hansfbaiер



A year's worth of work and headache. Being stuck 95% of the time. Finally the first square wave coming out of the Kintex7 GTX transceiver, using openXC7 the full open source FPGA toolchain.



Angelo Jacobo • 1st
Digital IC Design Engineer | Top #1 in EC...
1mo • 6

UberDDR3 now runs on OrangeCrab ECP5 FPGA 🎉

The open-source journey continues! [...more](#)



Now Zynq!

Double trouble?

- “Unique” PS + PL structure

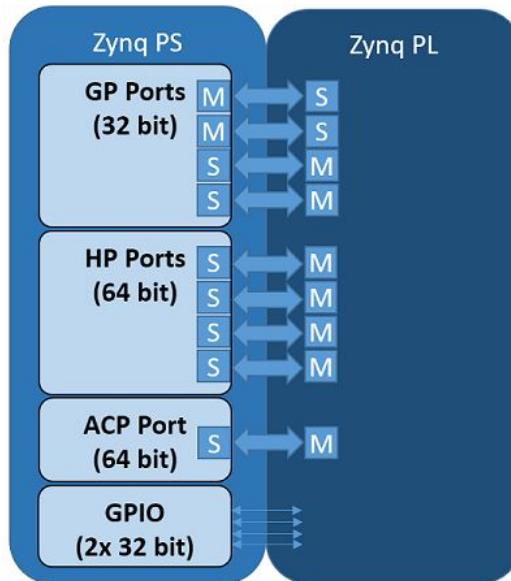
2x ARM A9, DDR3

ETH/USB/...

Flexible pins

Boot

Linux / RTOS



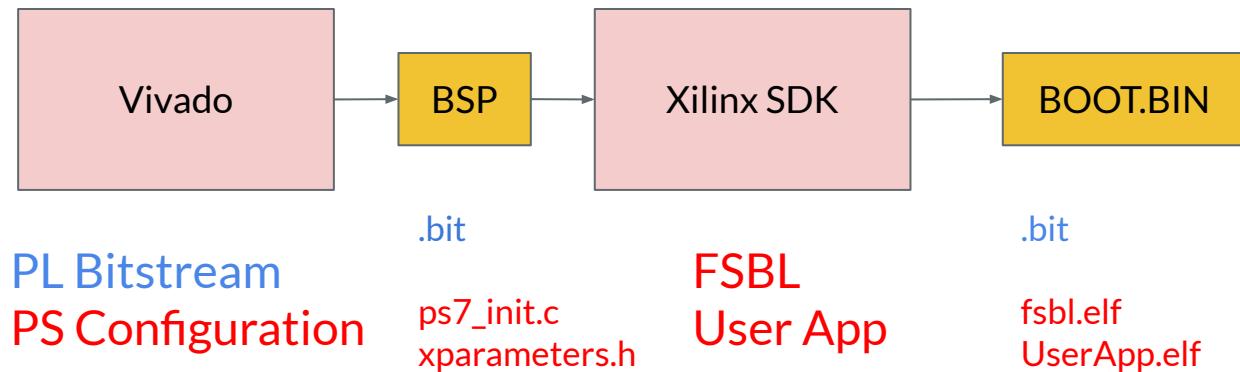
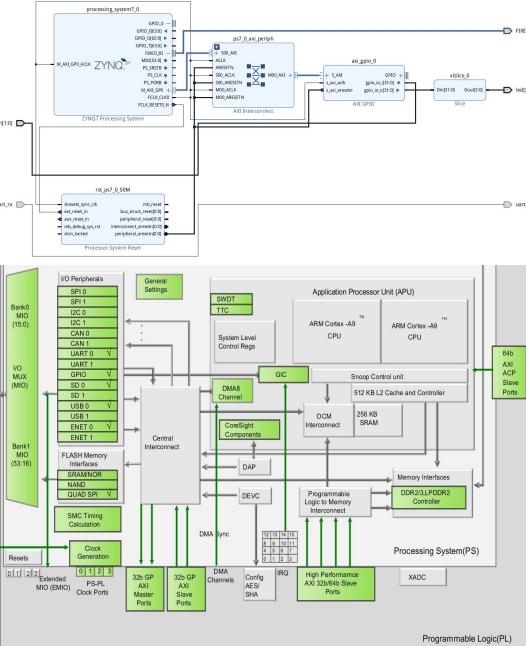
FPGA fabric,
HDMI/ETH/LED/...

Custom Logic
bitstream

https://pynq.readthedocs.io/en/latest/overlay_design_methodology/pspl_interface.html

Are you confident...

- Building a Zynq BOOT.BIN firmware by yourself?
- How long does it take?



Hundreds of mouse clicks!

Decoding the ARM registers

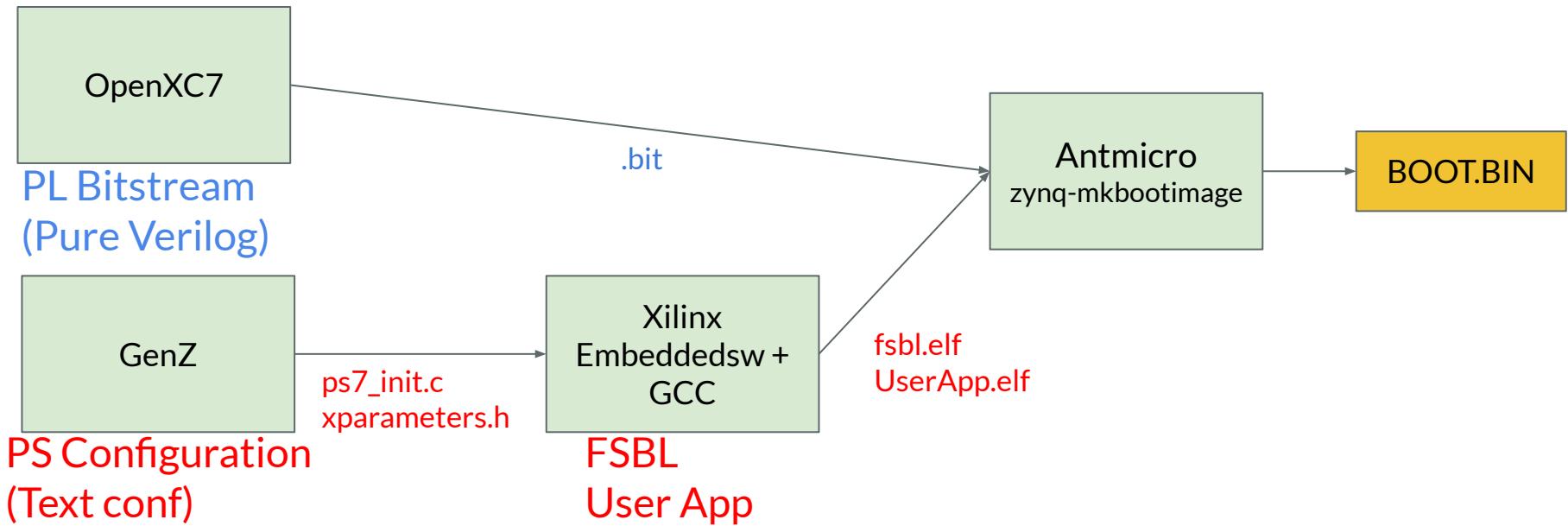
- 100+ reg writes
- Zynq 7000 SoC Technical Reference Manual (UG585)
 - PLLs
 - Clock Freqs
 - DDR (TODO)
 - MIO MUXs
 - Peripherals
- Debug (???)

ps7_init.c

```
// START: top
// .. START: SLCR SETTINGS
// .. UNLOCK_KEY = 0XDF0D
// .. ==> 0XF8000008[15:0] = 0x0000DF0DU
// .. ==> MASK : 0x0000FFFFU    VAL : 0x0000DF0DU
// ..
EMIT_WRITE(0XF8000008, 0x0000DF0DU),
// .. FINISH: SLCR SETTINGS
// .. START: PLL SLCR REGISTERS
// .. . START: ARM PLL INIT
// .. . PLL_RES = 0x2
// .. . ==> 0XF8000110[7:4] = 0x00000002U
// .. . ==> MASK : 0x000000F0U    VAL : 0x000000020U
// .. . PLL_CP = 0x2
// .. . ==> 0XF8000110[11:8] = 0x00000002U
// .. . ==> MASK : 0x000000F0U    VAL : 0x000000200U
// .. . LOCK_CNT = 0xfa
// .. . ==> 0XF8000110[21:12] = 0x000000FAU
// .. . ==> MASK : 0x003FF000U    VAL : 0x000FA000U
// ..
EMIT_MASKWRITE(0XF8000110, 0x003FFFF0U ,0x000FA220U),
// .. . . . START: UPDATE FB_DIV
// .. . . . PLL_FDIV = 0x28
// .. . . . ==> 0XF8000100[18:12] = 0x000000028U
// .. . . . ==> MASK : 0x0007F000U    VAL : 0x00028000U
// ..
EMIT_MASKWRITE(0XF8000100, 0x0007F000U ,0x00028000U),
// .. . . . FINISH: UPDATE FB_DIV
// .. . . . START: BY PASS PLL
// .. . . . PLL_BYPASS_FORCE = 1
// .. . . . ==> 0XF8000100[4:4] = 0x00000001U
// .. . . . ==> MASK : 0x00000010U    VAL : 0x000000010U
// ..
EMIT_MASKWRITE(0XF8000100, 0x000000010U ,0x000000010U),
// .. . . . FINISH: BY PASS PLL
// .. . . . START: ASSERT RESET
// .. . . . PLL_RESET = 1
// .. . . . ==> 0XF8000100[0:0] = 0x000000001U
// .. . . . ==> MASK : 0x000000001U    VAL : 0x000000001U
```

OpenXC7 + GenZ

- BOOT.BIN in 5 minutes
- Awesome through 2035



What does this mean?

Enjoy RP2040? How about Zynq!

	RP2040	Zynq 7010
“PS”	2x Cortex M0+ @ 133 MHz 264 kB SRAM UART, SPI, etc USB 1.1	 A small green printed circuit board with a central Broadcom SoC, labeled "raspberrypi pico Dev Board". It has a USB port and several pins for connecting external components.
“PL”	8x Programmable I/Os Modules	28K+ LE
I/O	30 GPIOs	80+ HR I/Os
Price	<€5	€10 - €200
Toolchain	Cross platform, FOSS  pico-sdk-2.1.0.tar.gz 2.3 MB Nov 25, 2024	x86 Win/Linux only, Proprietary  Vivado HLx 2019.1: All OS installer Single-File Download (TAR/GZIP - 21.39 GB) U.S. Government Export Approval

Enjoy RP2040? How about Zynq!

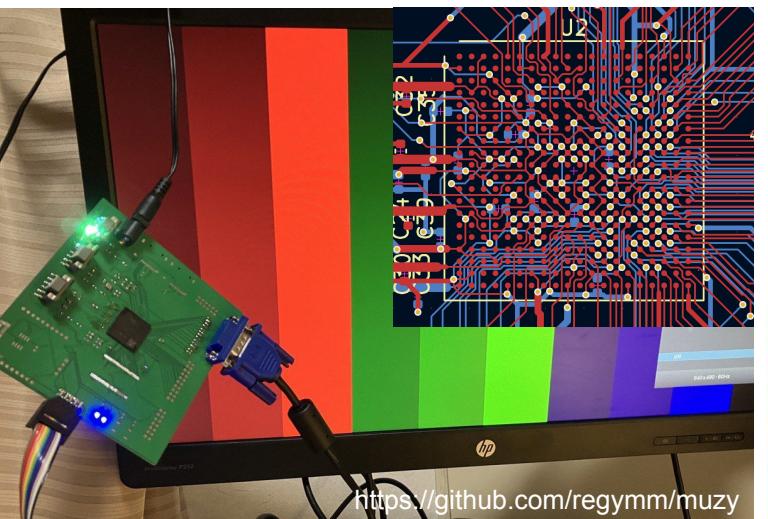
	RP2040	Zynq 7010		
“PS”	2x Cortex M0+ @ 133 MHz 264 kB SRAM UART, SPI, etc USB 1.1	 A small green printed circuit board with a central chip and various pins, labeled "Raspberry Pi Pico Dev Board".	2x Cortex A9 @ 667 MHz 256 kB OCM + DDR UART, SPI, SDCARD, etc USB 2.0, 1Gbps ETH	 A larger green printed circuit board with multiple chips, capacitors, and connectors, labeled "Zynq 7010 Dev Board".
“PL”	8x Programmable I/Os Modules	28K+ LE		
I/O	30 GPIOs	80+ HR I/Os		
Price	<€5	€10, €60 - €200		
Toolchain	Cross platform, FOSS  pico-sdk-2.1.0.tar.gz 2.3 MB Nov 25, 2024	Cross platform, FOSS <code>docker pull regymm/openxc7</code> <code>git clone https://.../GenZ</code>		

Zynq-as-MCU

- Boards are available
- Upcycled boards set price at €10



EBAZ4205, ~€10



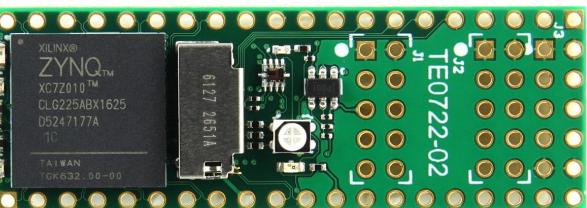
2-Layer
640x480 VGA
115 MHz SDRAM



shop.trenz-electronic.de

Photo Shows
Similar Product

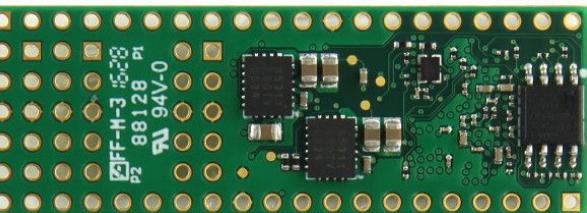
ZynqBerryZero, ~€100
Trenz electronic



shop.trenz-electronic.de

Photo Shows
Similar Product

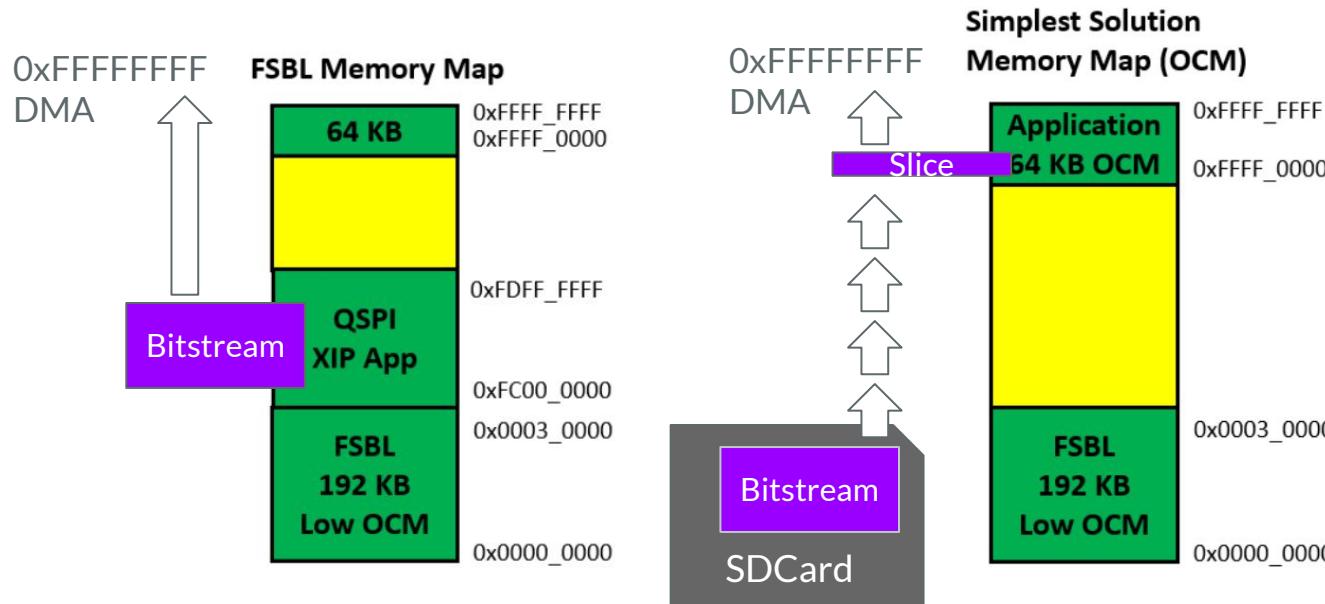
Muzy-2, BoM ~€10



DIPFORTy1, ~€60
Trenz electronic

Possibilities unlocked

- #1 No DDR SD Boot
 - Not supported officially, was not convenient



<https://xilinx-wiki.atlassian.net/wiki/spaces/A/pages/2418900993/Zynq+7000+Tips+and+Tricks>

Possibilities unlocked

- #2 Overclock 🔥

```
+cpu_mult_template='EMIT_MASKWRITE\(\0XF8000100, 0x0007F000U ,0x000XX000U\),  
+cpu_mult_find='\s'"\${cpu_mult_template/XX/\(..)}"  
+ddr_mult_template='EMIT_MASKWRITE\(\0XF8000104, 0x0007F000U ,0x000XX000U\),  
+ddr_mult_find='\s'"\${ddr_mult_template/XX/\(..)}"
```

- hz12opensource/libresdr

- GenZ

```
z7000_ps_param_900 = {  
    'freq' : { 'crystal' : 33.333333333,  
              'apu'      : 900.0  
            }  
}
```

Flexibility meets more flexibility

- #3 PL bitstream built on PS itself
- It's an ARM anyways
- OpenXC7 runs on 1 GB mem

```
Info: SA placement time 1.90s
Info: Max frequency for clock 'FCLK_CLK_buffered[0]': 145.50 MHz (PASS at 12.00 MHz)
Info: Slack histogram:
Info: legend: * represents 1 endpoint(s)
Info: + represents [1,1) endpoint(s)
Info: [ 76460, 76788) *****
Info: [ 76788, 77116) ***
Info: [ 77116, 77444) ***
Info: [ 77444, 77772) ***
Info: [ 77772, 78100) ***
Info: [ 78100, 78428) ***
Info: [ 78428, 78756) ***
Info: [ 78756, 79084) *
Info: [ 79084, 79412) ***
Info: [ 79412, 79740) ***
Info: [ 79740, 80068) ***
Info: [ 80068, 80396) ***
Info: [ 80396, 80724) ***
Info: [ 80724, 81052) |
Info: [ 81052, 81380) ***
Info: [ 81380, 81708) |
Info: [ 81708, 82036) |
Info: [ 82036, 82364) *
Info: [ 82364, 82692) |
Info: [ 82692, 83020) **
Info: Checksum: 0x05ea868f
Info: Running post-placement legalisation...
Info: Tying unused PS7 inputs to constants...
Info: Routing global clocks...
Info:   routing clock 'FCLK_CLK_buffered[0]'
Info: Running router...
Info: Setting up routing resources...

```



```
Tasks: 31, 7 thr; 2 running
Load average: 1.40 0.44 0.1
Uptime: 00:20:51

```

PID	USER	PRI	NI	VIRT	RES	SHR	S	CPU%	MEM%
2137	xilinx	20	0	1119M	439M	464	R	10.3	88.6
2120	xilinx	20	0	5832	1040	784	R	0.3	0.2
1706	root	20	0	25952	1148	1000	S	0.2	0.2
2106	xilinx	20	0	10140	92	0	S	0.1	0.0
814	root	19	-1	40492	168	4	S	0.0	0.0
1	root	20	0	27544	40	0	S	0.0	0.0
1341	root	20	0	13584	12	0	S	0.0	0.0
1445	systemd-t	20	0	17088	0	0	S	0.0	0.0

F1Help F2Setup F3Search F4Filter F5Tree F6SortBy F7Nic

Larger devices

- **Zynq 7030, 7035, 7045, 7100 now supported by OpenXC7 + GenZ**
- Would have transceivers and PCIe blocks, DDR3 on PL, ...



Future

Freedom is the future

- DDR3? PetaLinux? More IP cores?
- More IP cores w/ Open Source Toolchains?

Start here!

Name: basys3 FPGA Part: Auto (xc7a35tq) Backend: Auto (openxc7) Top Module: top

What mode do you want?
[Online Editor](#) [GitHub Project](#)

Constraint file

```
1 // This file is a general .xdc for the Basys3 rev B board
2 ## To use it in a project:
3 ## - uncomment the lines corresponding to used pins
4 ## - rename the used ports (in each line, after get_ports) according to
5 ## the pin assignments in the Basys3 Rev B Pinout table
6 # Clock signal
7 set_property PACKAGE_PIN HS [get_ports CLK100MHz]
8 set_property IOSTANDARD LVCMOS33 [get_ports CLK100MHz]
9 #create_clock -add -name sys_clk_pn -period 10.00 -waveform {0 5} [get_
10 _ports sys_clk_pn]
11 # Switches
12 set_property PACKAGE_PIN V17 [get_ports {sw[0]}]
13 set_property IOSTANDARD LVCMOS33 [get_ports {sw[0]}]
14 set_property PACKAGE_PIN V16 [get_ports {sw[1]}]
15 set_property IOSTANDARD LVCMOS33 [get_ports {sw[1]}]
16 set_property PACKAGE_PIN W16 [get_ports {sw[2]}]
17 set_property IOSTANDARD LVCMOS33 [get_ports {sw[2]}]
18 set_property PACKAGE_PIN W17 [get_ports {sw[3]}]
19 set_property IOSTANDARD LVCMOS33 [get_ports {sw[3]}]
20 set_property PACKAGE_PIN W18 [get_ports {sw[4]}]
21 set_property IOSTANDARD LVCMOS33 [get_ports {sw[4]}]
```

Verilog source file

```
1 // Basys3 test
2 // by petergu 2023.4.23
3 `timescale 1ns / 1ps
4
5 module top(
6     input CLK100MHz,
7     output [15:0]LED,
8     input [15:0]sw
9 );
10
11 reg [31:0]cnt = 0;
12 always @ (posedge CLK100MHz) begin
13     cnt <= cnt + 1;
14 end
15 assign LED[7:0] = cnt[31:24];
16 assign LED[15:8] = sw[15:8];
17
18 endmodule
```

Online, self-hostable
FPGA dev platform

Submit

No reply from server.

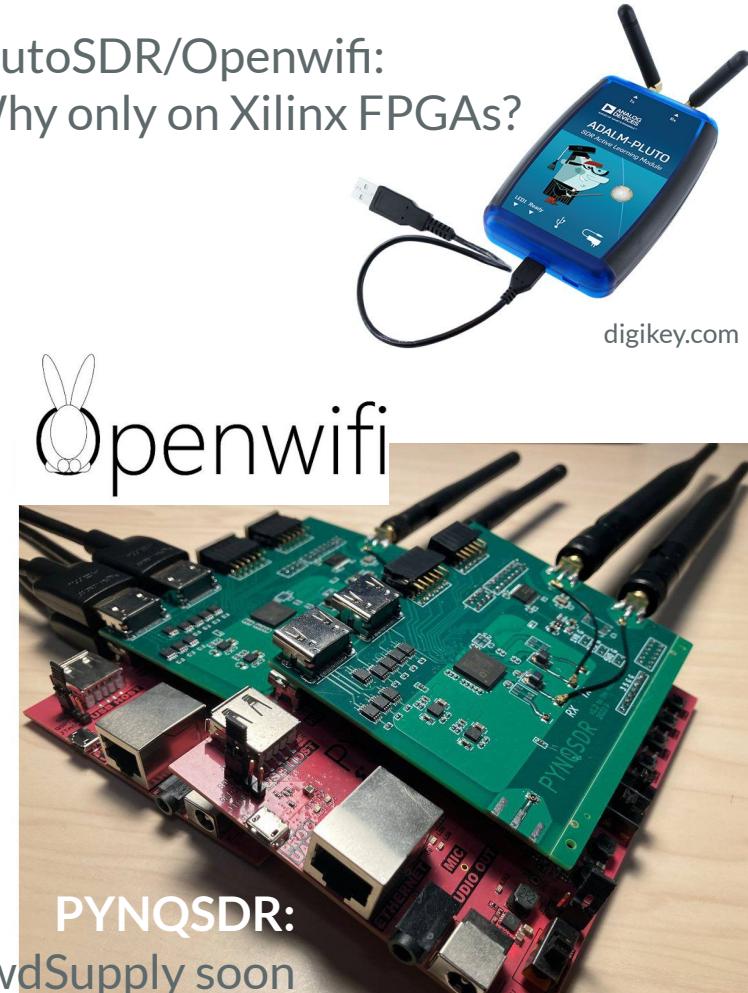
Fetch & Show Log Download Log Program Bitstream... Download Bitstream

Compilation log

```
WebUSB programmer log
wasmFPGALoader initializing...
wasmFPGALoader loaded.
```

<https://caas.symbioticeda.com/>

PlutoSDR/Openwifi: Why only on Xilinx FPGAs?



PYNQSDR:
release on CrowdSupply soon

Acknowledgement



OPEN
Compute Project®



OCP-TAP



LUG@USTC



VLAB@USTC

Thank you!

- github.com/regymm/GenZ
- github.com/openXC7