Edge ML Acceleration with RISCV-enhanced eFPGA-SoCs

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Introduction

- Growing demand to perform ML tasks on edge devices

Natural Language Interaction

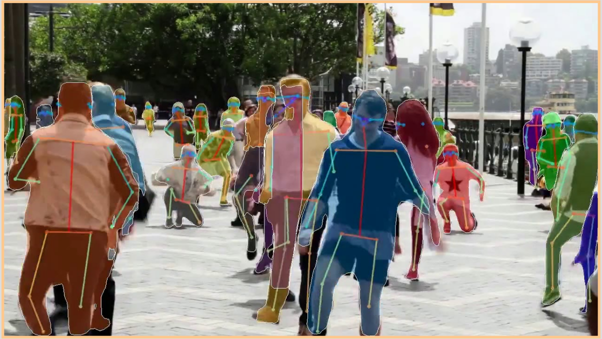
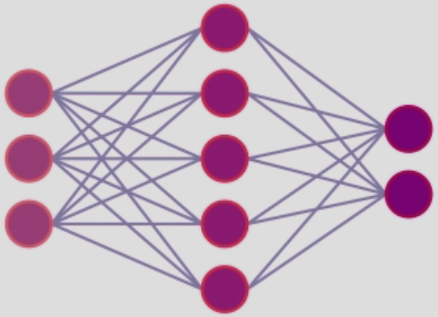


Image and Video Classification



On Device Training

- The appropriate HW deployment is:
  - *low power* - operates under severe power constraints
  - *low development effort* - easy to implement
  - *flexible* - adapt to changing ML models

These design criteria motivate innovation for specialized architectures

Motivation: Performance vs. Design Complexity

- **Cons of bespoke ML accelerator design from scratch**
  - High design effort
  - Significant software preparation
  - Low-flexibility/Fixed-function

Best Performance

High Design Complexity

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High Design Complexity

- **Role of Compilers + General Purpose Compute**
  - Streamline hardware interfacing
  - High-flexibility

Performance Suffers
Low Design Complexity

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- **Reuse in the Open-Source Domain**
  - Leverage existing solutions to reduce design complexity
  - Promotes interoperability across projects

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Is it possible to combine aspects of these general implementation approaches with specialized open-source hardware?

Background: Edge ML and Open-Source CPUs

- **TensorFlow (Lite)** open-source development of ML models
  - Easy to use - training, inference, model tuning
  - Pre-trained models - highly optimized
  - Easy portability to open-source hardware with RISC-V
- **RISC-V** open-source development of efficient general purpose computing platforms
  - Highly flexible HW and EDA tools
  - Easily programmable with software toolchain support
  - Enhanced performance with custom ISA extensions

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TensorFlow + RISC-V

Strong foundation for ML hardware

Related Work: TFLite + RISC-V + ISA Extensions

Architecture	TensorFlow Lite	ISA Extensions	Post-Silicon Reconfigurability	Open-Source Hardware	SoC Integration
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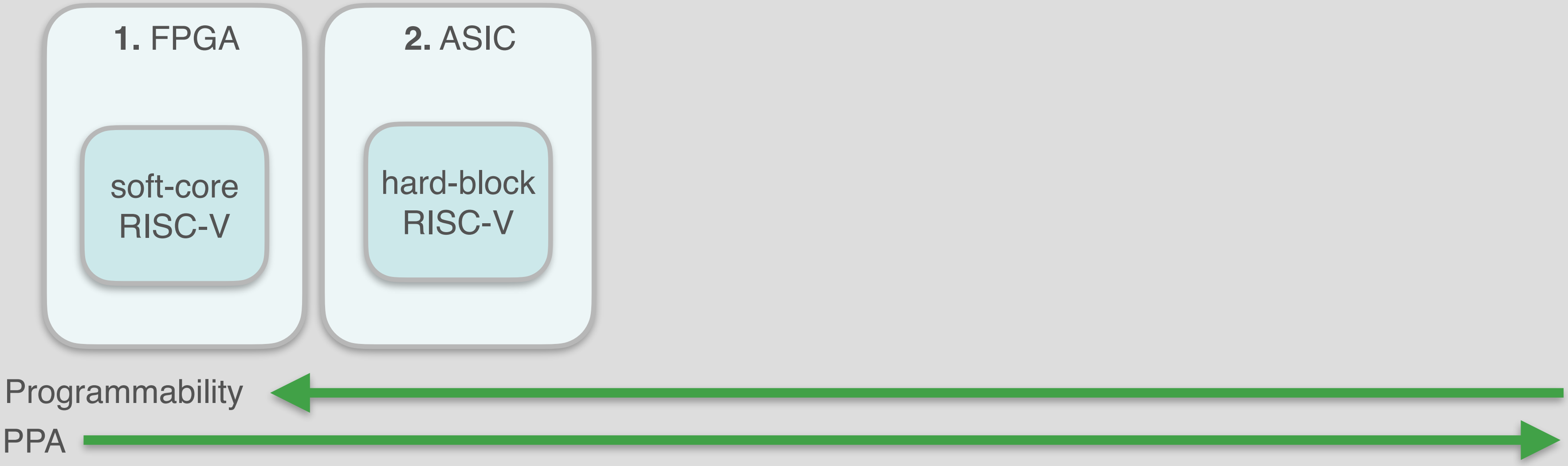
3					
4					
5					
This Work					



1. FPGA

soft-core RISC-V

2. ASIC

hard-block RISC-V

Programmability

PPA

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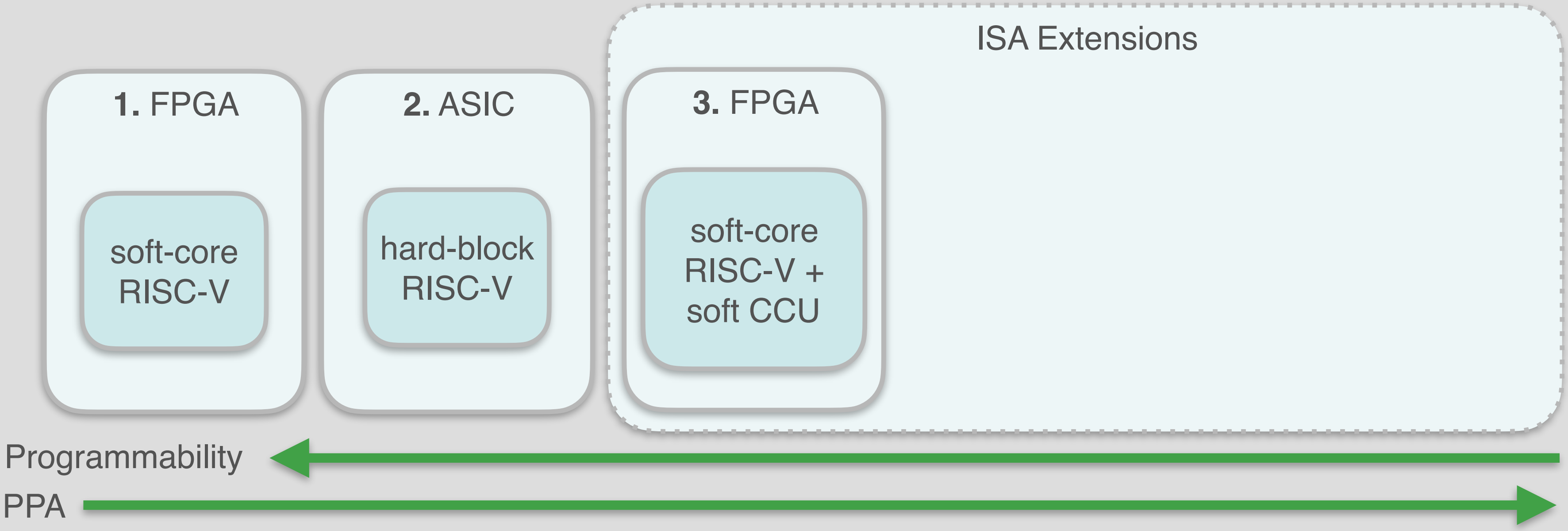

ISA Extensions

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3. FPGA

soft-core RISC-V + soft CCU

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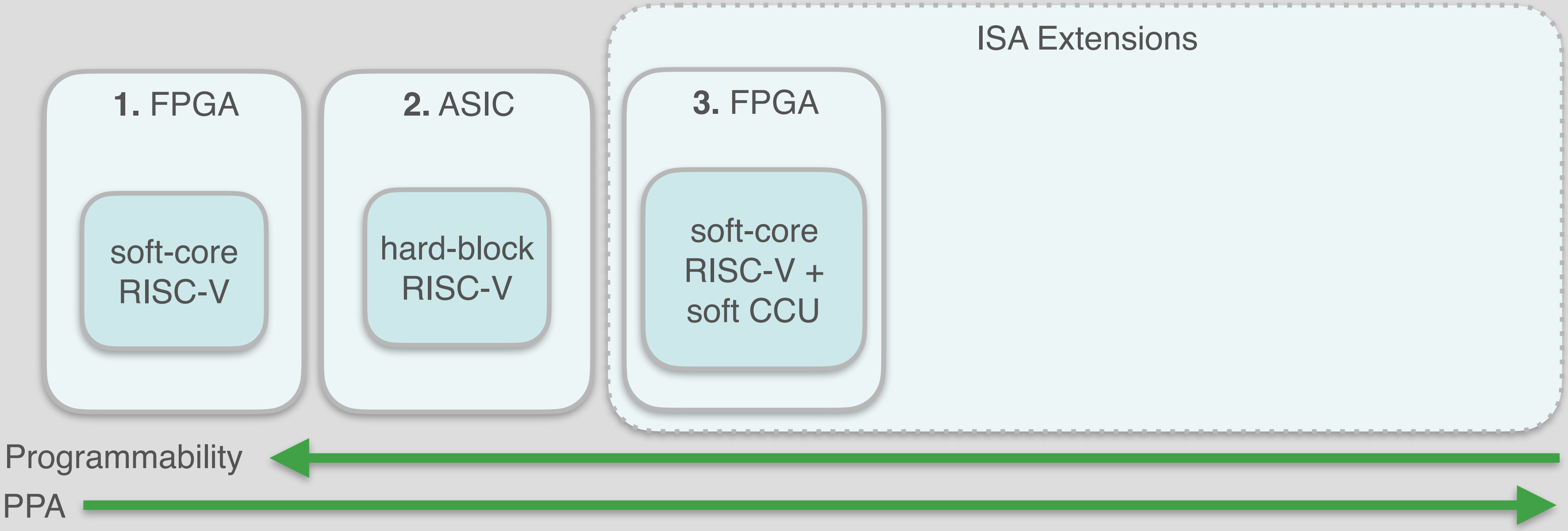

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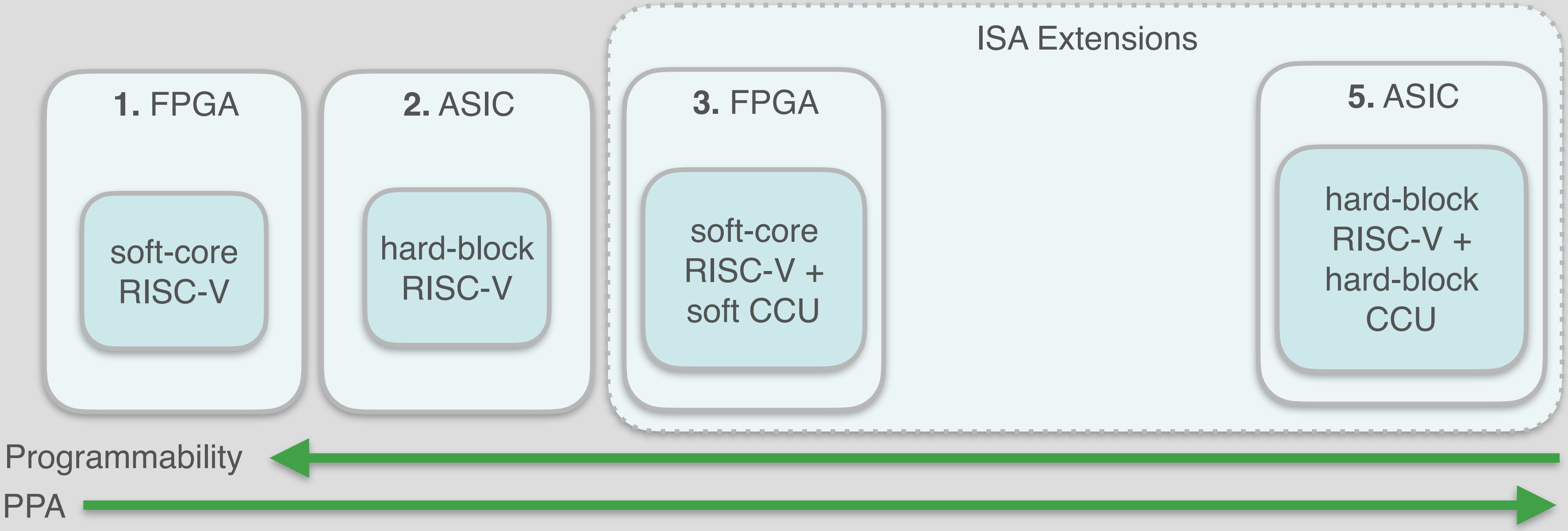

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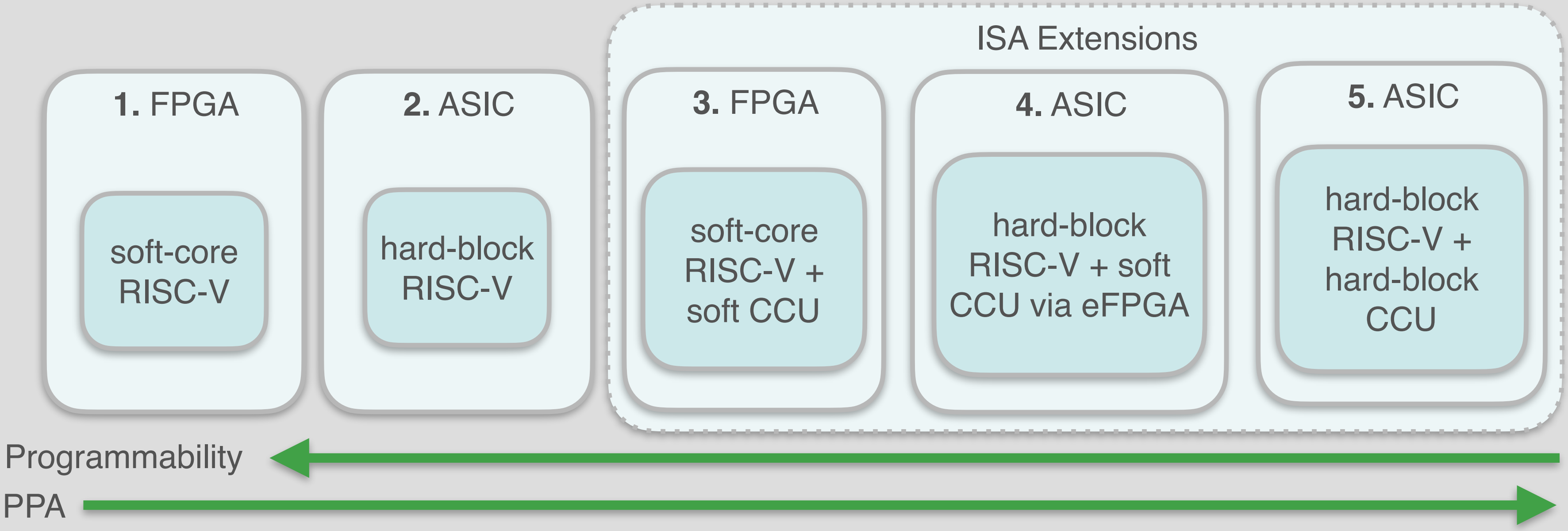

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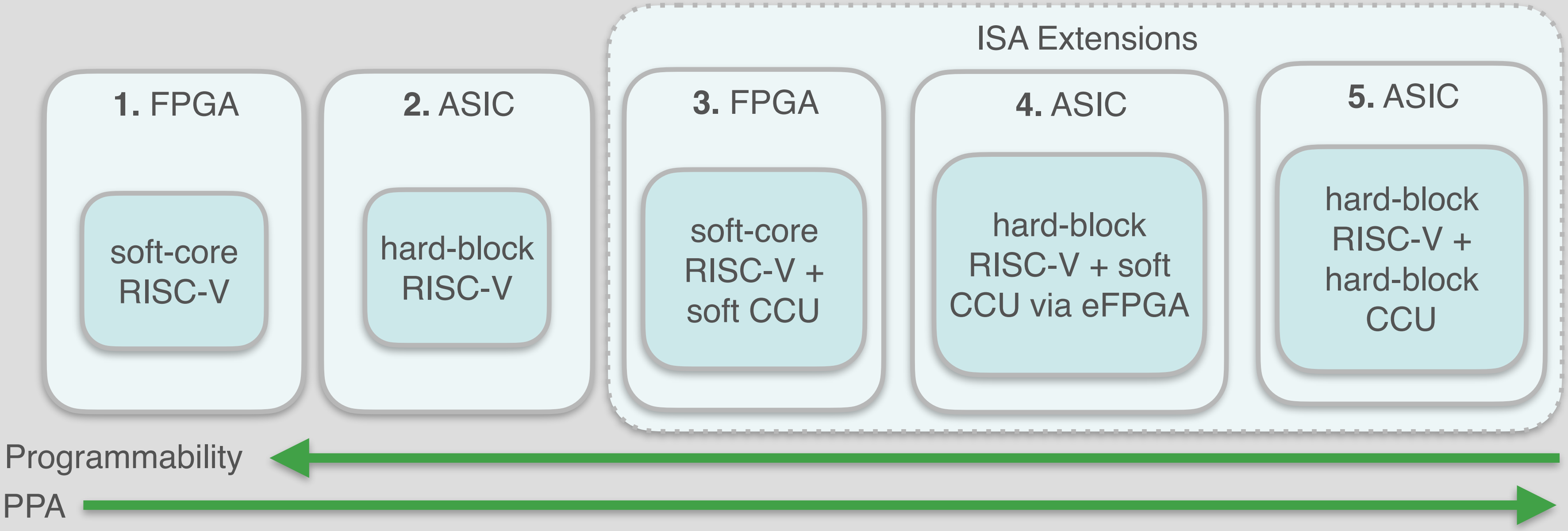

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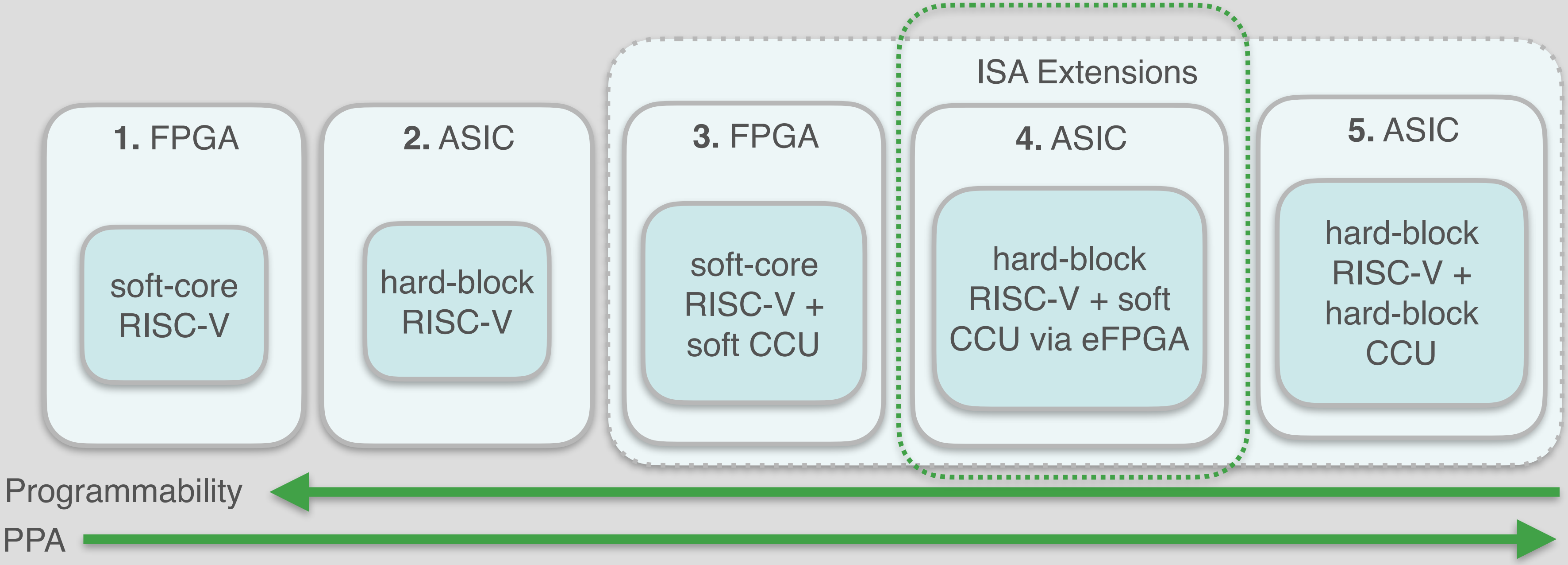

Proposal

- Assemble “hard-block” Ibex RISC-V and OpenFPGA eFPGA to support ML ISA extensions
- Integrate architecture as loosely-coupled programmable accelerator in SoC with ESP
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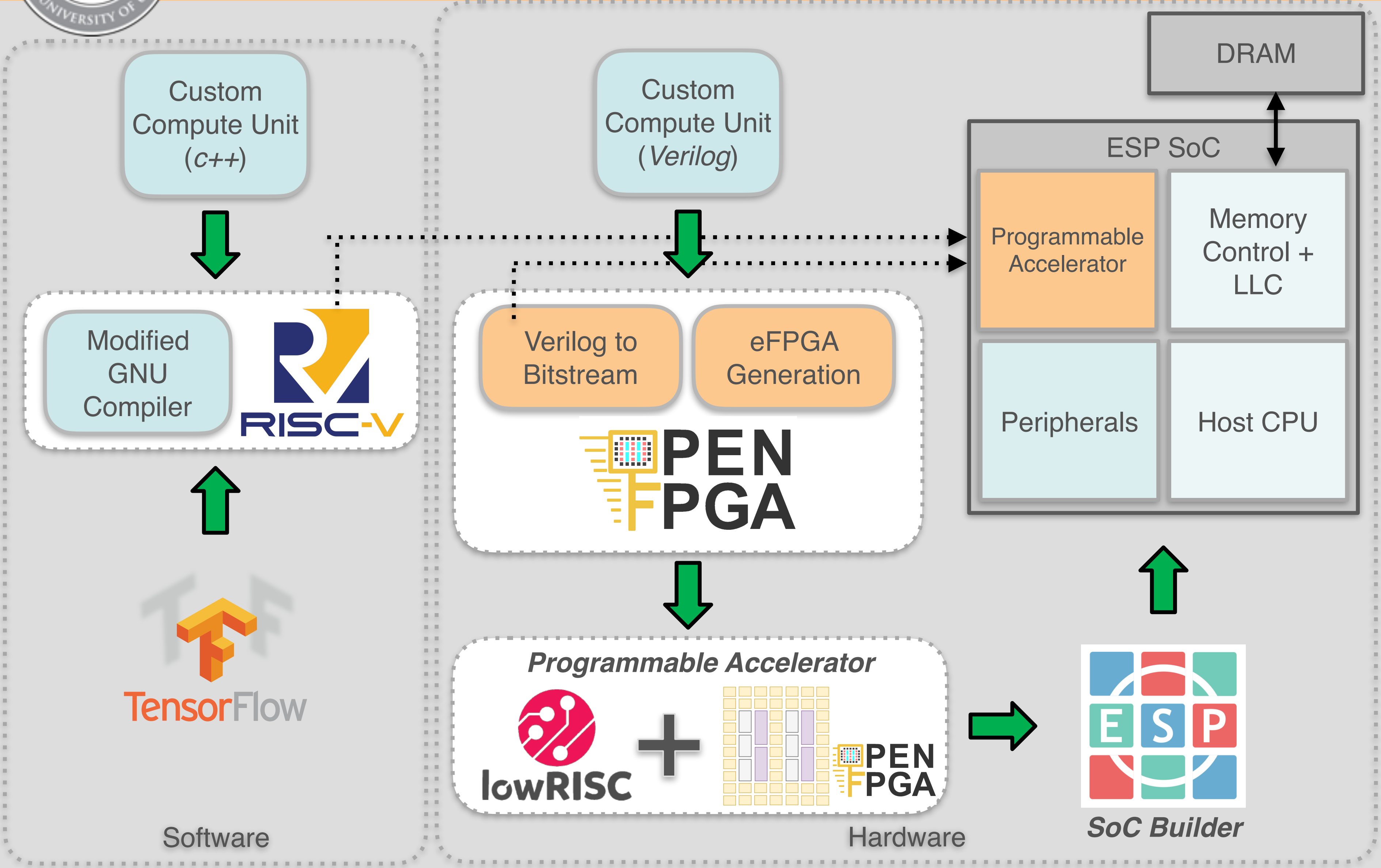
Contributions:

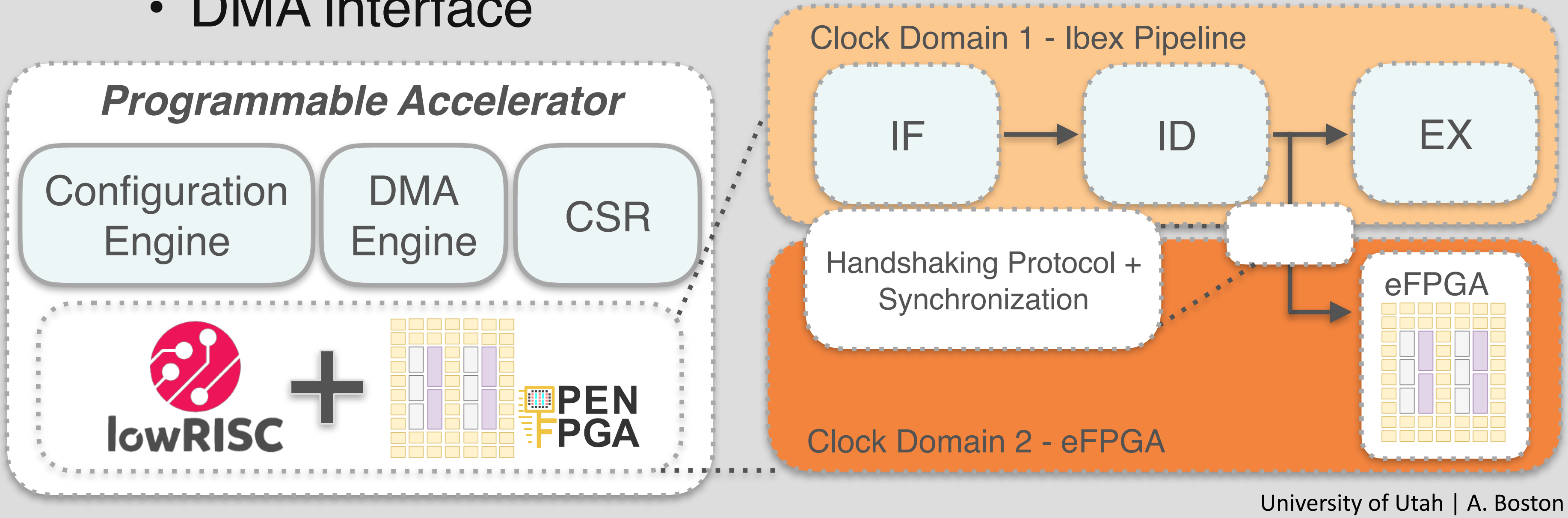
- Tightly-coupled RISC-V + eFPGA programmable accelerator
- Integration into ESP-based heterogeneous SoC
- Acceleration of TensorFlow Lite workloads

Open-Source Tool Flow



Programmable Accelerator Architecture

- Tightly-coupled Ibex RISC-V and OpenFPGA eFPGA
  - eFPGA inserted into RISC-V pipeline
  - RISC-V pipeline stalls when eFPGA invoked
  - Multi-Clock Domain management
  - eFPGA wrapper
    - Configuration engine
    - Control and status register
    - DMA interface



OpenFPGA - In a nutshell

Customers

Applications:
Yolov3
Resnet
etc.

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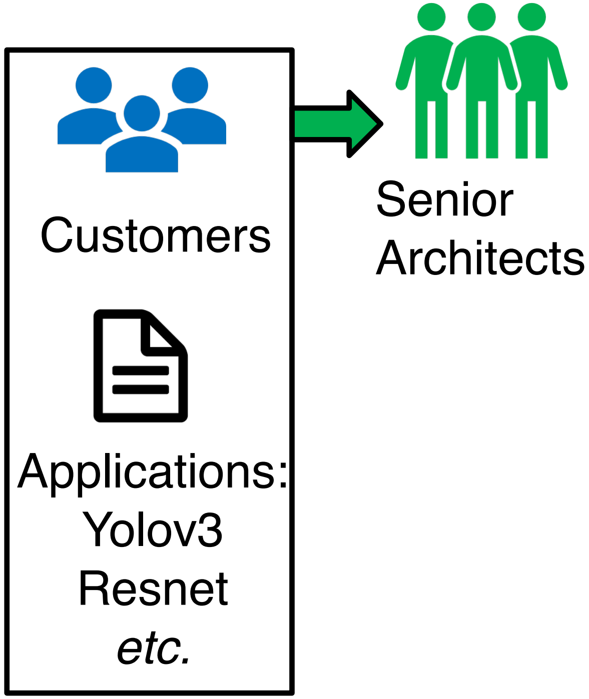

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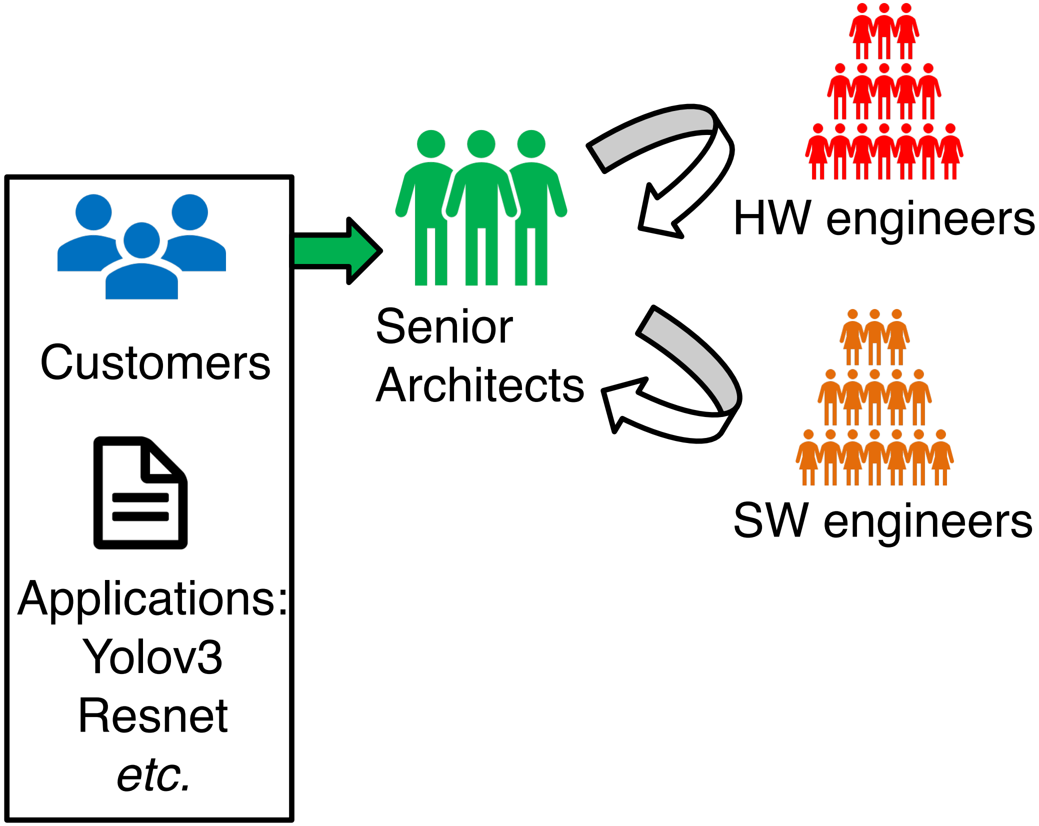

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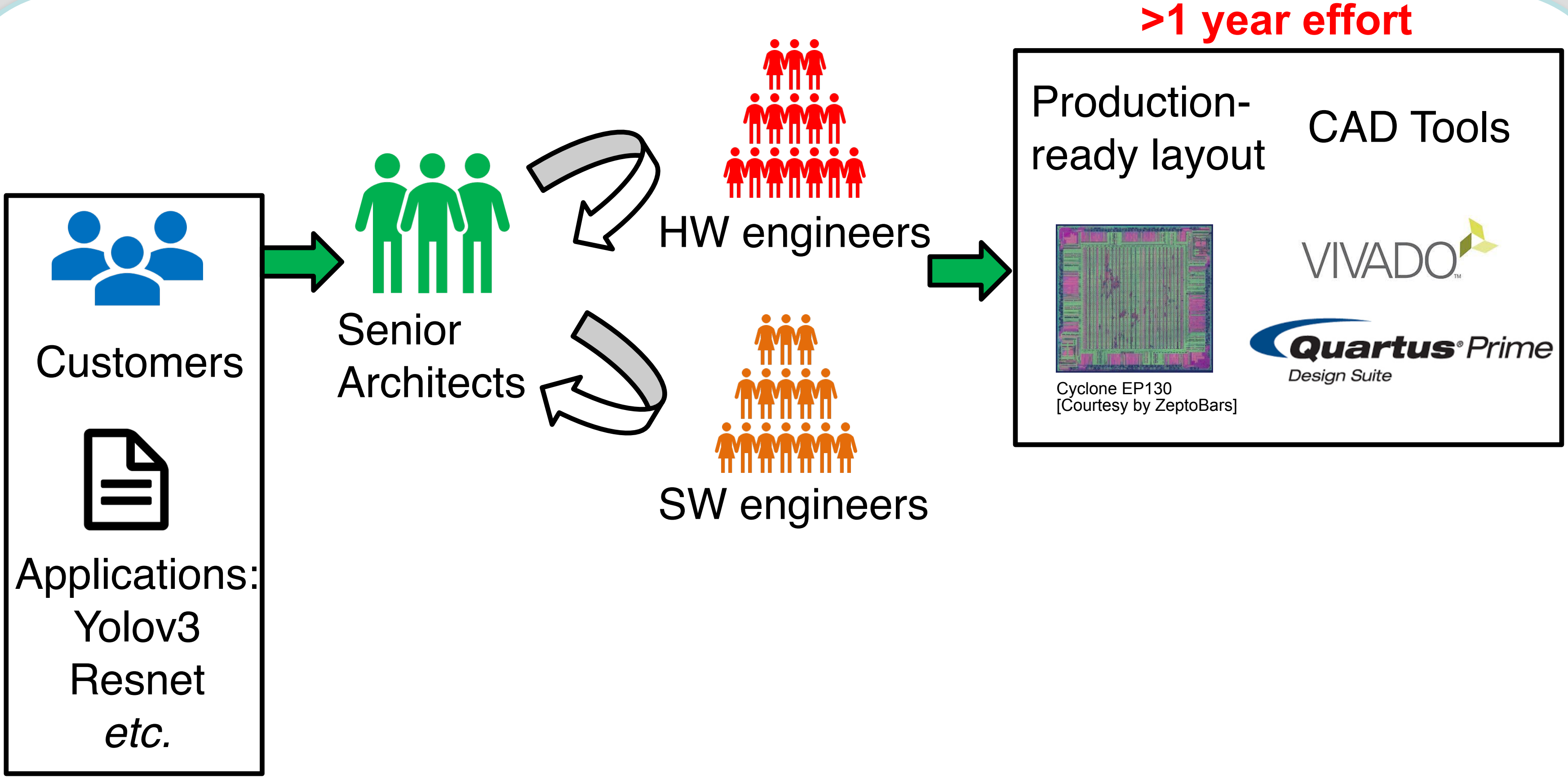

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>1 year effort

Production-ready layout

CAD Tools

Cyclone EP130
[Courtesy by ZeptoBars]

VIVADO

Quartus Prime
Design Suite

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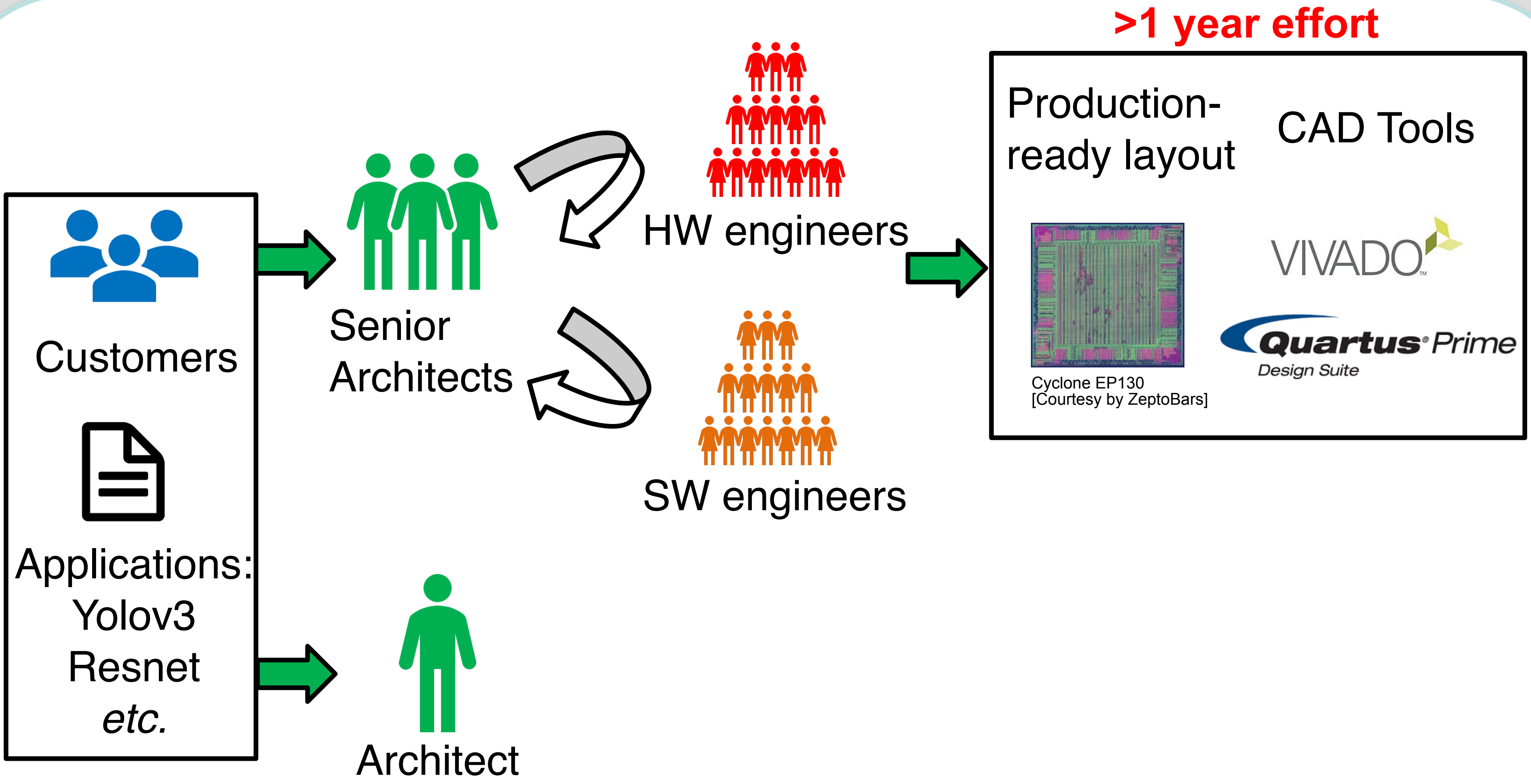

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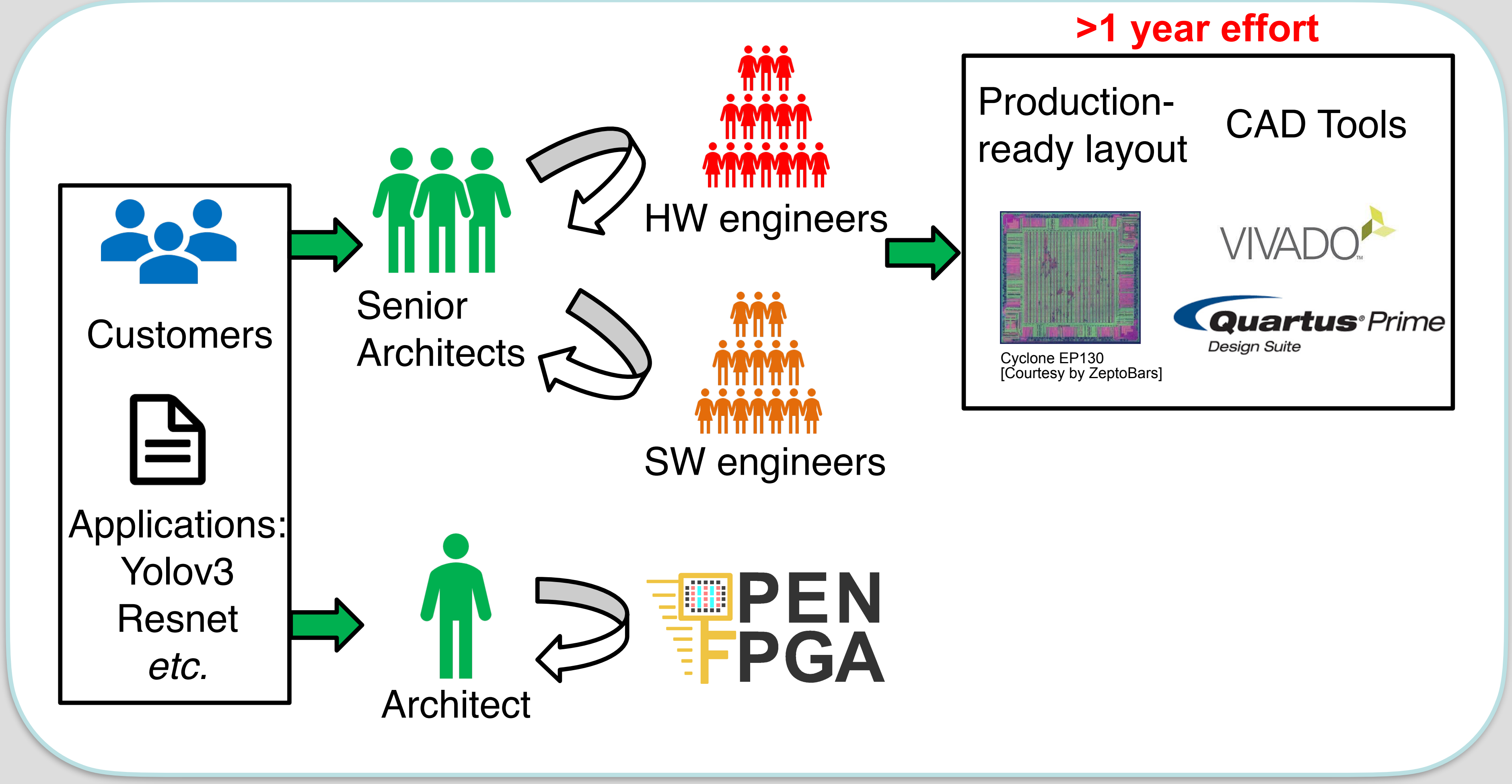

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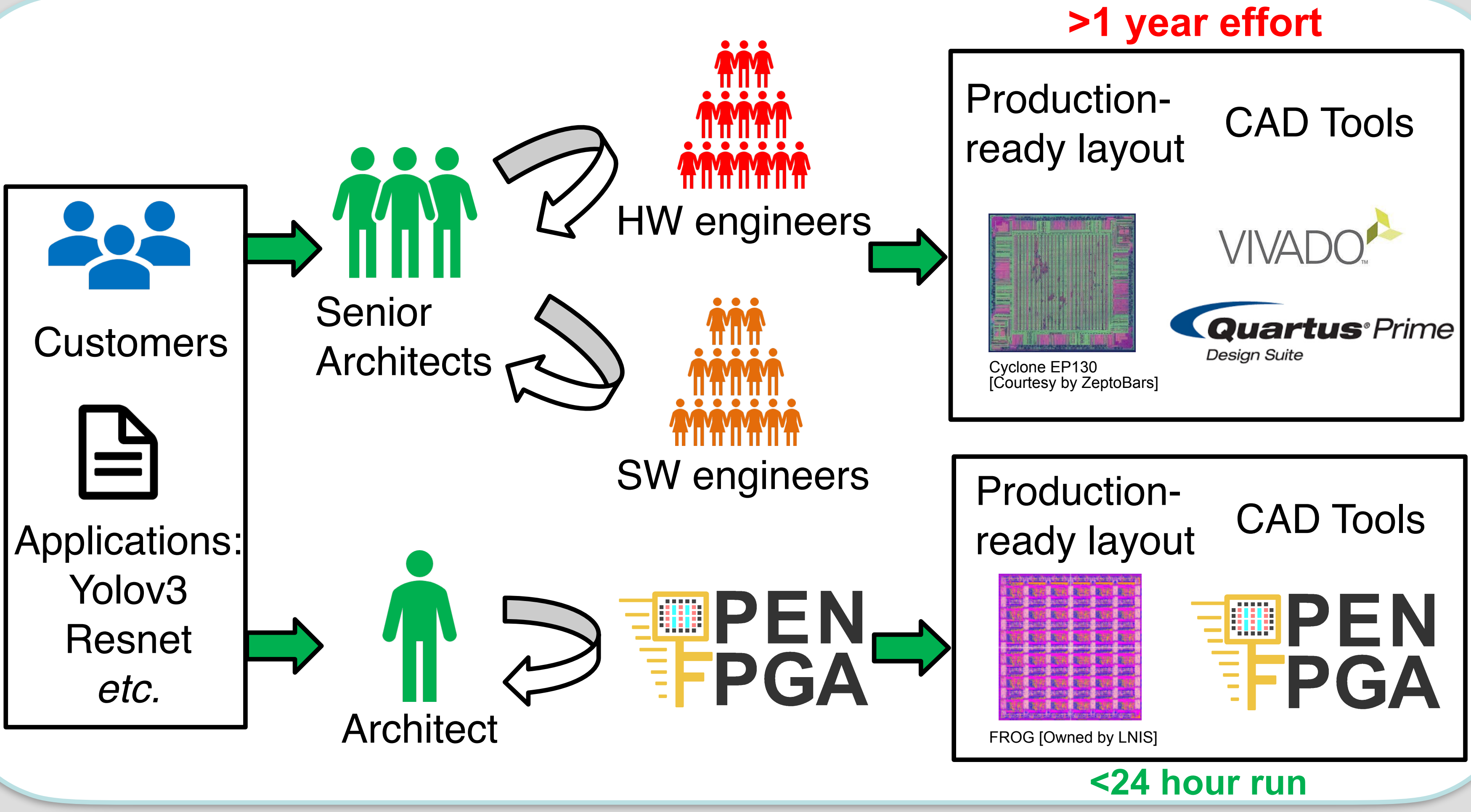

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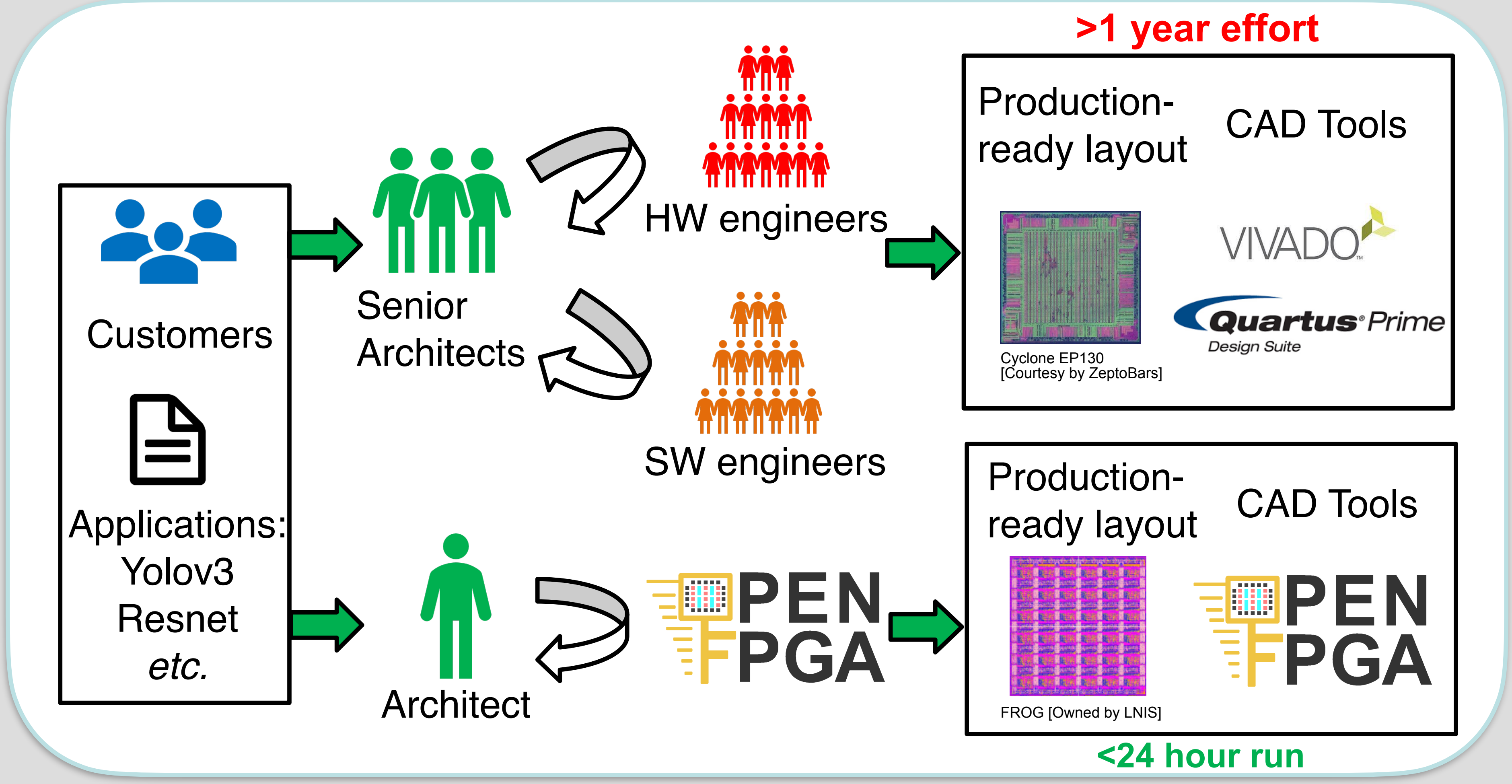

✓ Complete FPGA and eFPGA generation (10+ commercial and academic tape-outs)

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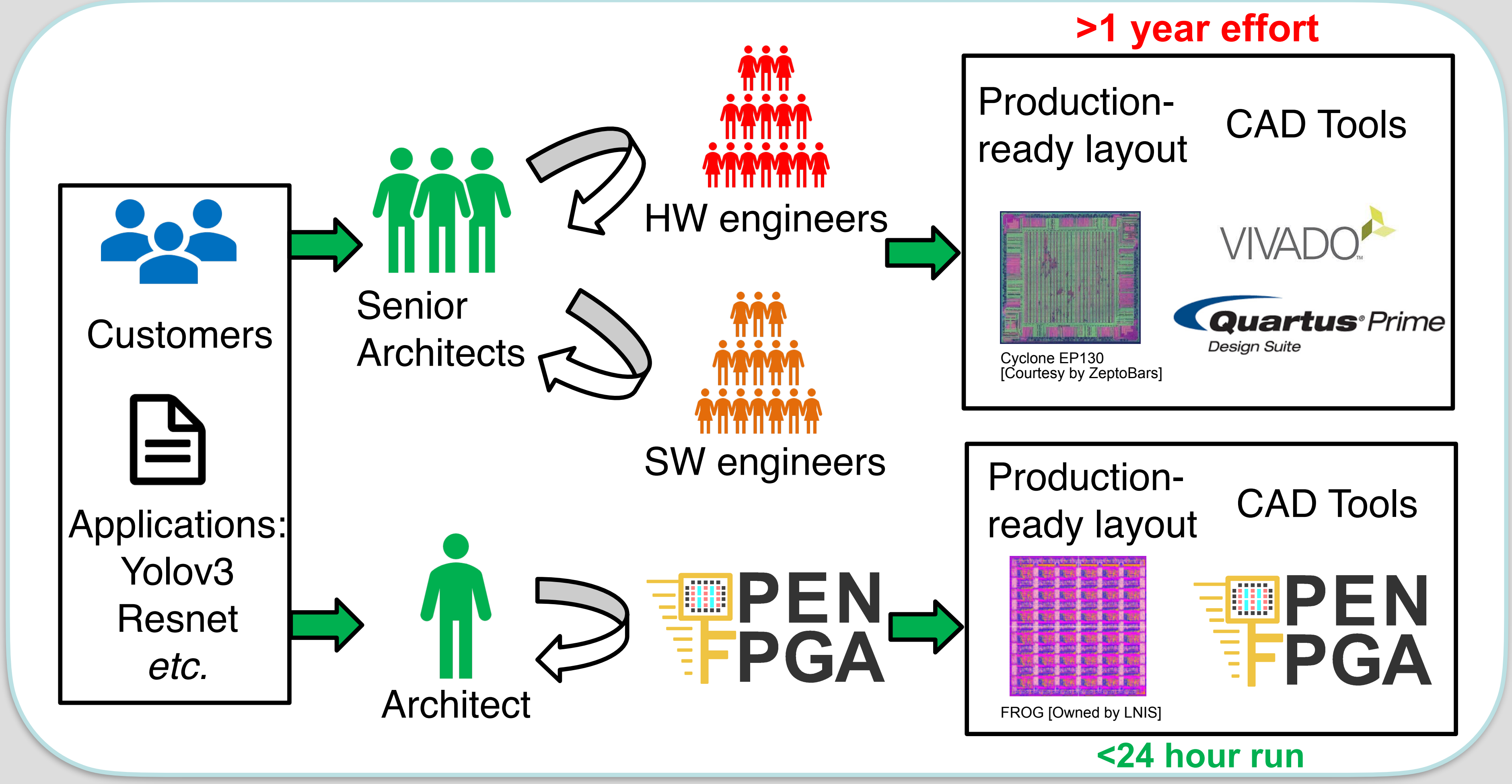

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✓ Fully customizable modern architecture (100+ tested)

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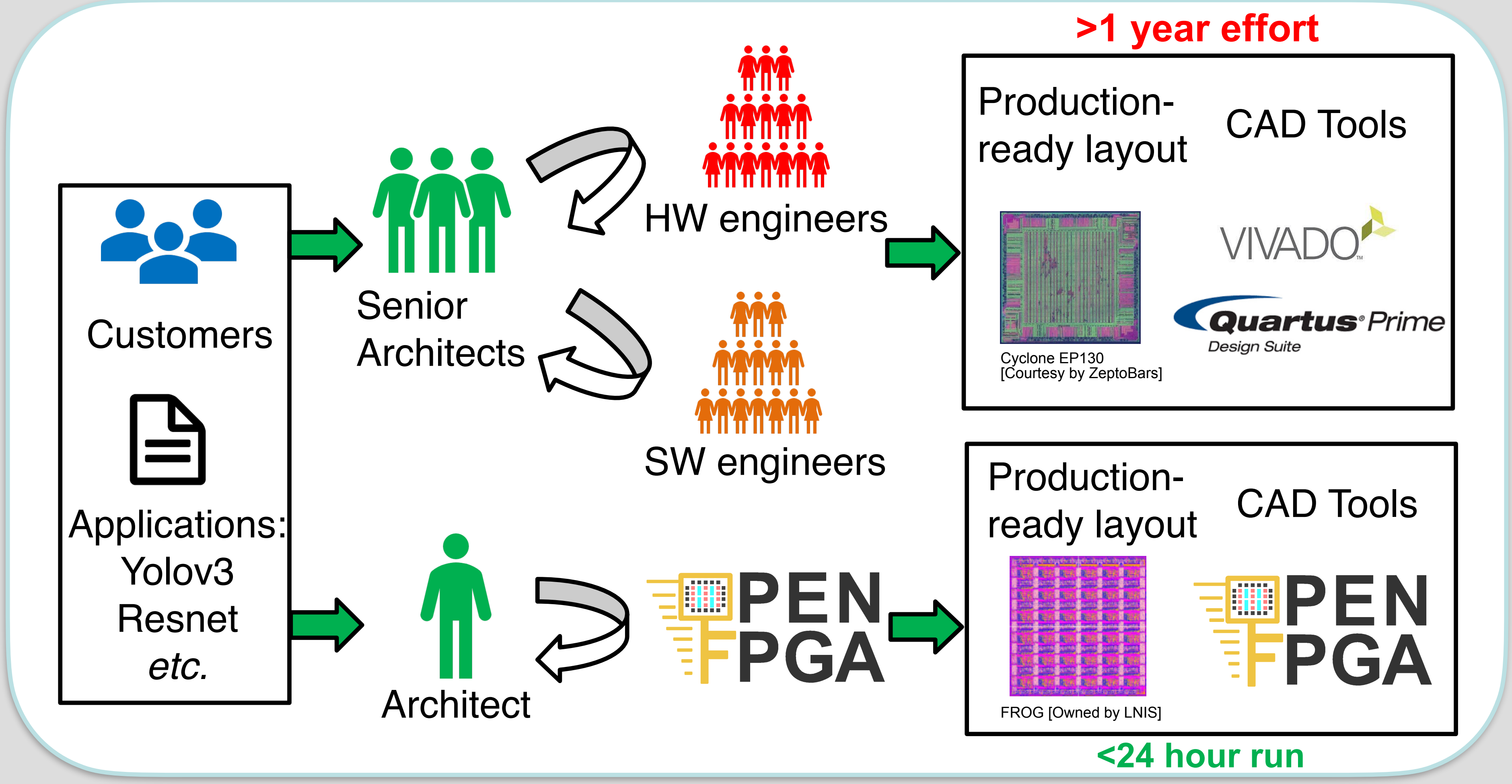

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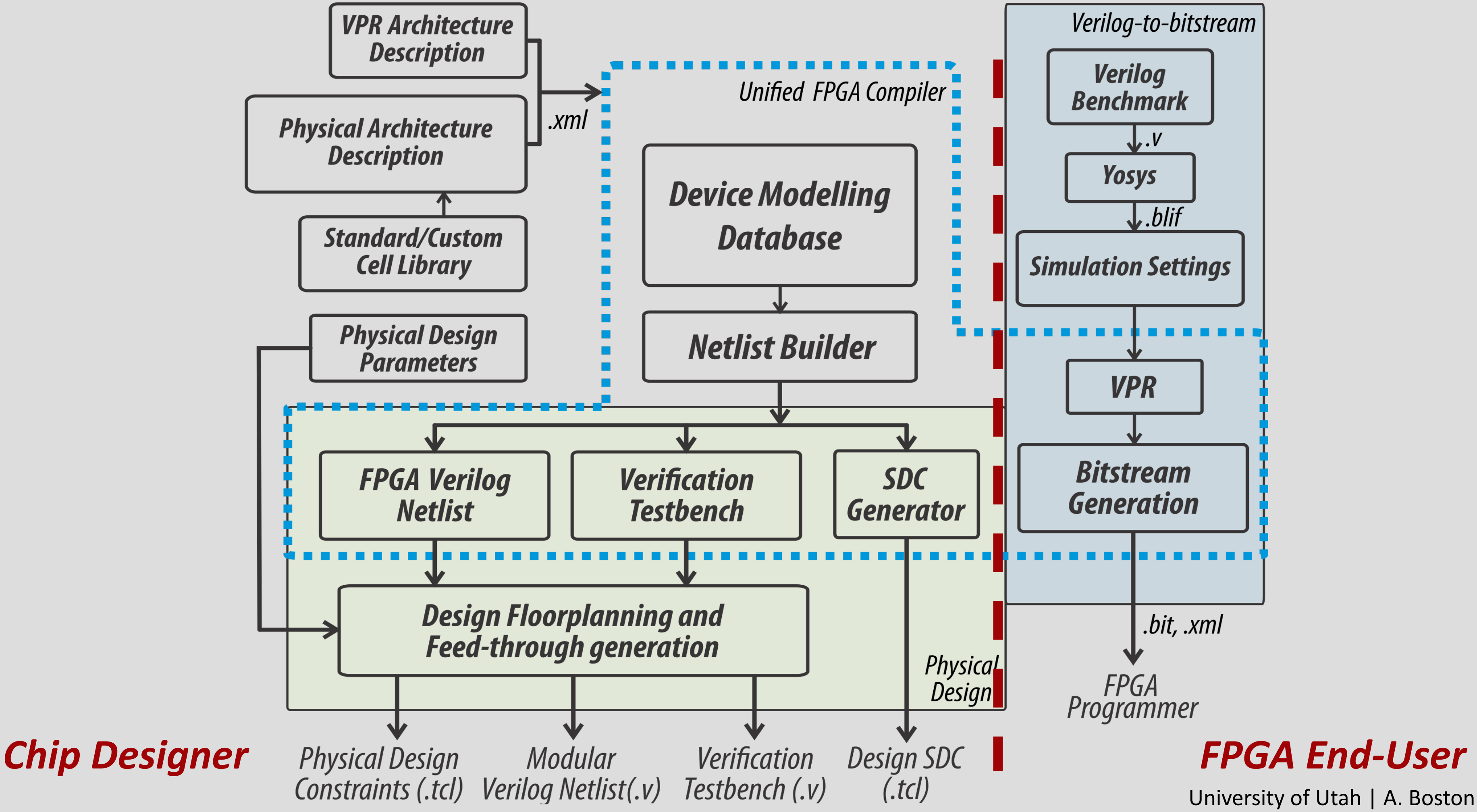
- ✓ Complete FPGA and eFPGA generation (10+ commercial and academic tape-outs)
- ✓ Fully customizable modern architecture (100+ tested)
- ✓ Optimized for fast physical design (150k-LUT+ FPGA < 24 hr)

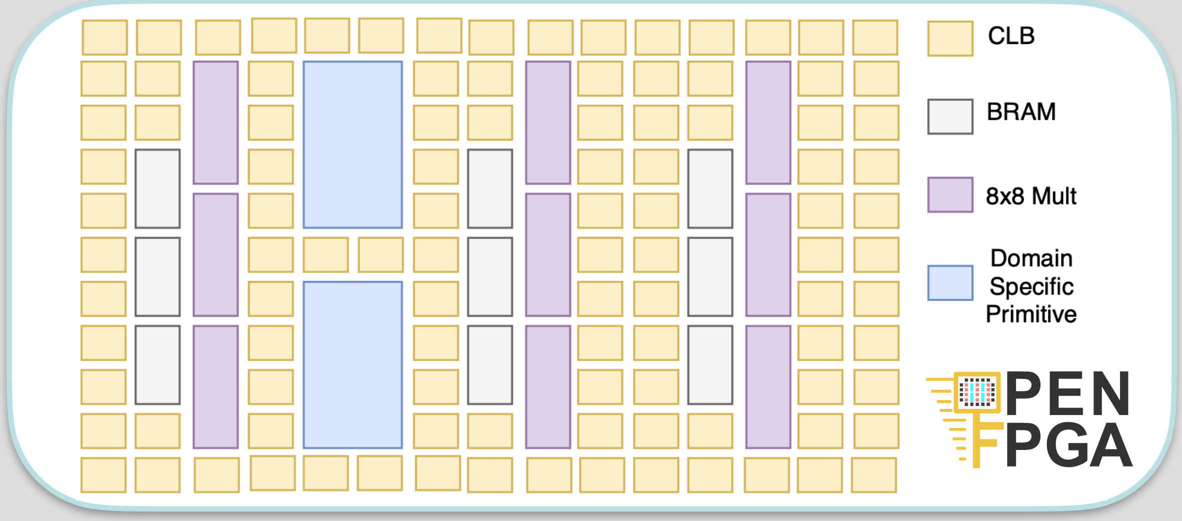
OpenFPGA - In a nutshell

- Unified code base for fabric generation, design verification and end-user bitstream generation


VPR Architecture Description
Physical Architecture Description
.xml
Standard/Custom Cell Library
Physical Design Parameters
Unified FPGA Compiler
Device Modelling Database
Netlist Builder
FPGA Verilog Netlist
Verification Testbench
SDC Generator
Design Floorplanning and Feed-through generation
Physical Design
Verilog-to-bitstream
Verilog Benchmark
.v
Yosys
.blif
Simulation Settings
VPR
Bitstream Generation
.bit, .xml
FPGA Programmer
Chip Designer
Physical Design Constraints (.tcl)
Modular Verilog Netlist(.v)
Verification Testbench (.v)
Design SDC (.tcl)
FPGA End-User

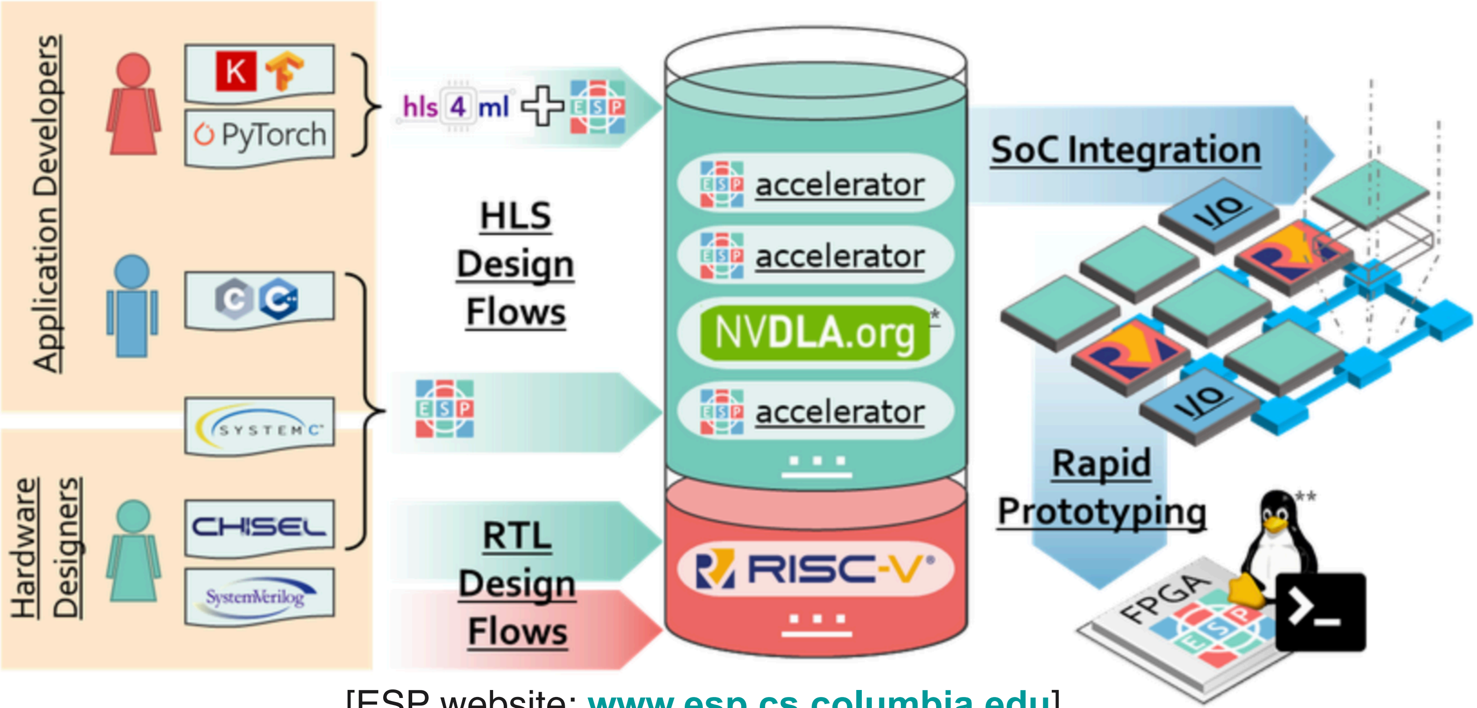
Domain-Specific eFPGAs

- OpenFPGA enables DSE and prototyping of highly customizable eFPGA fabrics
  - Best fit fabric architecture - k6_n8 vs. k4_n8
  - Appropriately sized fabric - 16×16 vs. 32×32
  - Balanced compute, memory, and routing resources
  - Domain-specific primitives to improve PPA
  - <u>Optimizing eFPGA lowers PPA trade-off for post-silicon reconfigurability</u>



SoC integration with ESP

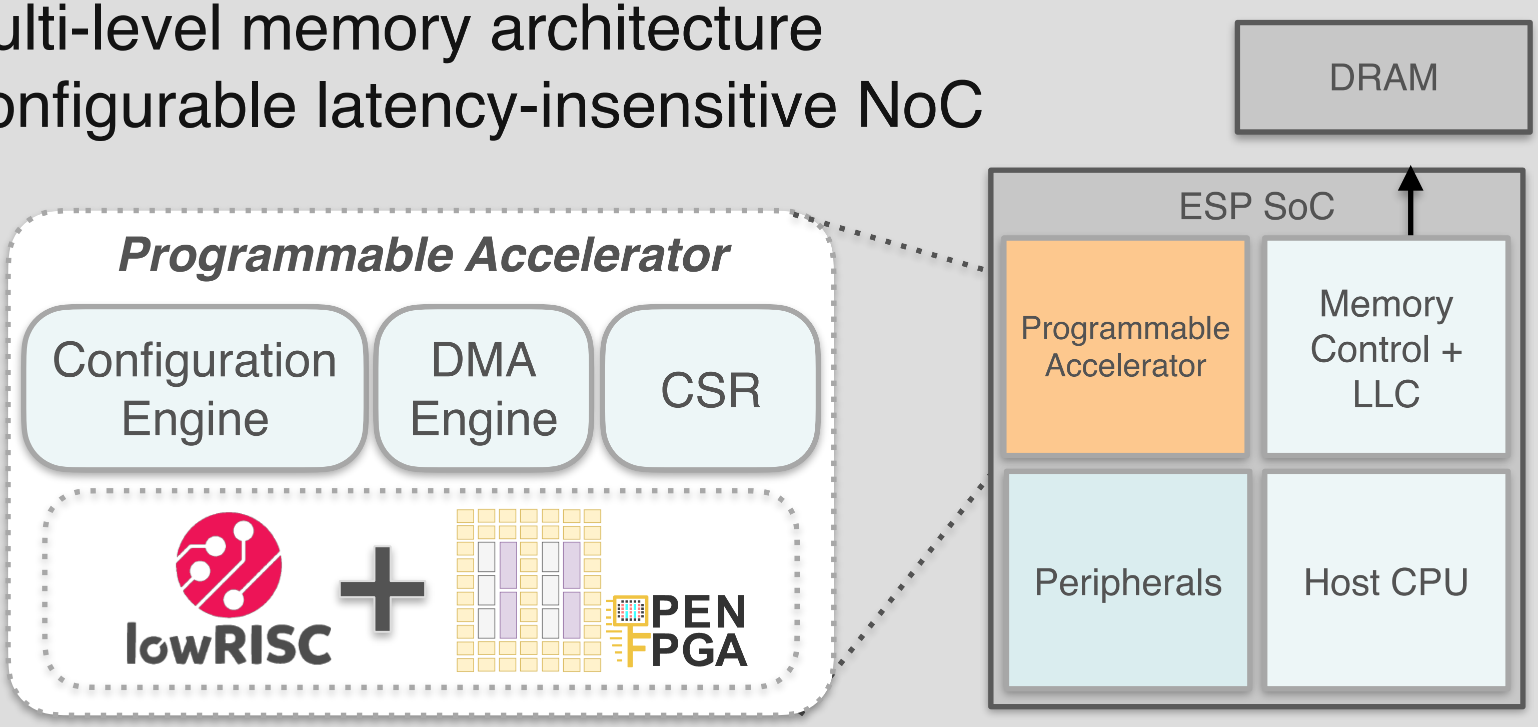
- ESP provides automated design flow for SoC development
- Supports different accelerator designs
- Push-button SoC generation and application mapping
- Rapid FPGA prototyping



[ESP website: www.esp.cs.columbia.edu]

2×2 SoC Architecture

- Programmable Accelerator Tile
  - RISC-V + eFPGA
- Host CPU
  - Manages SoC
  - Invokes accelerators
- Multi-level memory architecture
- Configurable latency-insensitive NoC



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- Acceleration of TensorFlow Lite workloads

- Approach combines aspects of user-friendly general purpose compute with ASIC performance and parallelization
- TensorFlow Lite → Heterogeneous SoC
- Toolchain enables HW DSE and PPA evaluation for RISC-V ML ISA extension architectures

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- *low power* - improved HW PPA compared to fully “soft-core”
- *flexible* - maintains post-silicon reconfigurability of CCU
- *low development effort* - TensorFlow Lite interoperability

Future Work: eFPGA Evaluation

- **DSE of eFPGA based on ISA extensions**
  - Determine the best fit eFPGA architecture
  - Appropriately size fabric to reduce overhead
  - Identify domain-specific primitives to improve PPA

- **Compare RISC-V coupling strategies**
  - Should the RISC-V hard-block be embedded directly in the eFPGA fabric or located outside of the eFPGA fabric?

- **Demonstrate the advantages of hard-block RISC-V**
  - Compare soft-core RISC-V on baseline FPGA architecture to a hard-block implementation in terms of power, area, and operating frequency

Future Work: System Level Evaluation

- **Execute TensorFlow Lite Models on proposed architecture**
  - Compare standalone RISC-V to proposed eFPGA enhanced architecture
    - Execute ML models with and without ISA extensions
    - Is the slow down of eFPGA worth the parallelization across all TensorFlow Lite benchmarks?
- **Show flexibility of eFPGA to accomodate several varying ML models**
  - Perform inference of varying ML tasks using the same architecture
- **Leverage open-source tool flow to evaluate hardware, *i.e.*, area, power, energy per inference**
  - SOTA works often evaluate only speedup of ML models with ISA extensions

Thank you for your attention

Questions?

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