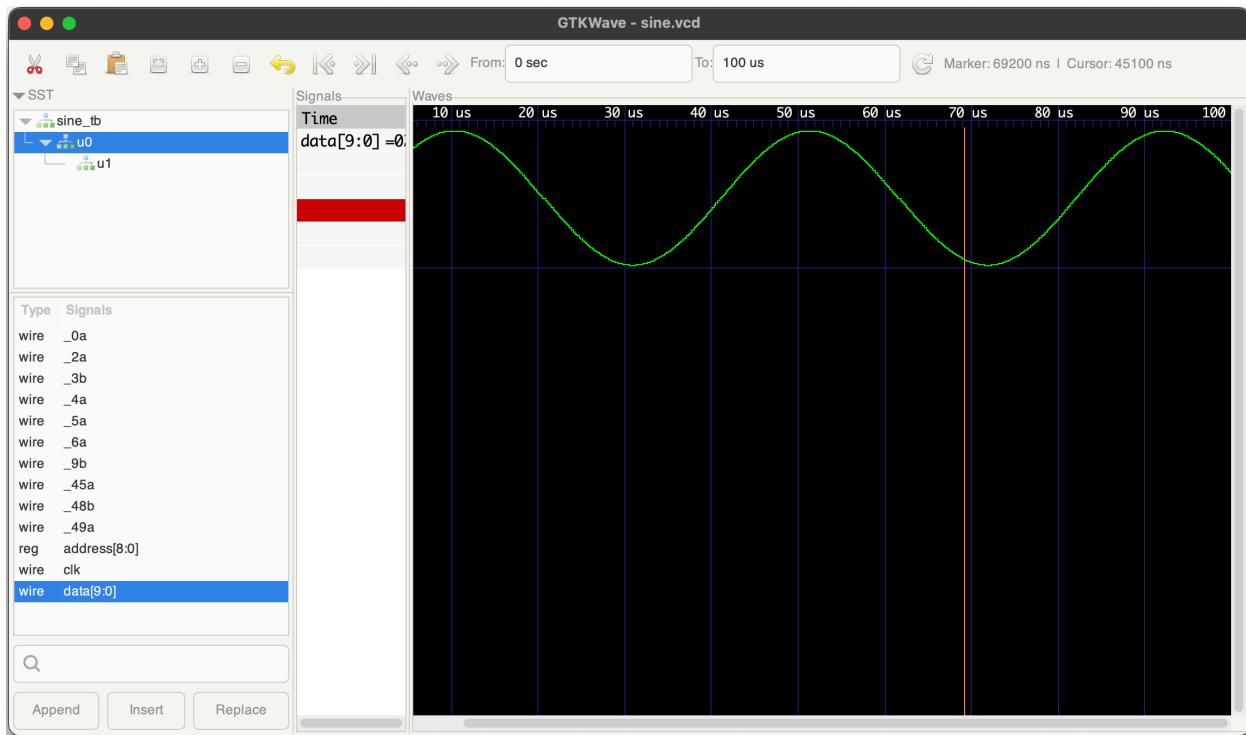


## Mini Project 3 Report

The design of my circuit mostly inherited the “sine” example. Since we are working with the constraints of 128 9-bit samples, I changed the memory module a bit. First, I changed the size of sample\_memory array as we only need to store 128 samples now. I then added a finite state machine in the always loop, using read\_address as a counter to see what stage of the sine wave we are currently in, and doing the corresponding manipulations. For each 9-bit sample, I just doubled its value so it has a range of 0-1024 instead of 0-512, also making sure that each wave cycle is supplied by 512 10-bit samples.

After changing the code, I simulated with GTKWave, which produced the result below.



I also used an oscilloscope to measure the VOUT pin of the DAC.

