

# Scalable Multi-Axis FOC on FPGA for Permanent Magnet Synchronous Motors

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## Abstract

Brushless Direct Current (BLDC) motors are widely utilized in robotics due to their lower maintenance needs and higher efficiency compared to brushed motors [3]. However, BLDC motors need a controller to operate. Field-oriented control is one way to control such a motor. This thesis explores the simultaneous control of multiple BLDC motors on a single FPGA through pipelining the FOC logic. The proposed FOC-core provides a platform for further motor control development with easy-to-replace modules used within. The FOC core contains pipelined logic for Clarke, Park, inverse Park -transformations, and the use of a pipelined CORDIC algorithm to enable possibilities for more advanced PWM techniques. The PWM generation and PI control are done through non-pipelined logic. Surrounding this Core, an implementation of multi-axis FOC has been created with 12 sets of motor configurations, where the corresponding resource usage has been reported. The proposed core and the outcome of the utilization reports have shown that sharing logic through pipelining in FOC is possible and can be beneficial when controlling multi-axis robots.

## 1 Introduction

This is a Short report for the FOC-Core that has been created. For a more in extensive background, report and analysis chapter, the full thesis is available at [1]. Most of the sections are partially or directly copied from the full thesis.

### 1.1 Motivation

Robotics and robotic manipulators have seen wide adoption in tasks that were previously performed by humans. One such example is the quadrupedal walked Spot [6] by Boston Dynamics that can be seen performing autonomous inspections in industrial facilities [5]. To control such a system, control on multiple levels is required. The lowest level of control of such a manipulator is the control of currents passing through the electrical motors. In the Open Dynamics robot (ODR)[12] a set of brushless direct current (BLDC) motors is used for the movement of the robot. The motors are powered by drivers which again are controlled by a system optimizing the flow of current. Such a system can include Trapezoidal Control, Sinusoidal Drive control, Simplified Vector control, and

Field Oriented Control (FOC)[7]. When researching robotics and electric motor fundamentals one might want to expand those underlying controllers. This could be an expansion in the complexity of controllers or an expansion in the number of motors controlled by a single chip. Controlling multiple motors through a single chip might reduce the hardware complexity as fewer controllers are needed. In both cases, it is important to know the insides of the selected motor-control system.

Utilizing Field Programmable Gate Arrays (FPGAs) a researcher can update and test multiple motor controllers on the same hardware. Having an open core for multi-axis control will also expand the possibilities for said researcher. By utilizing an open core, future research can expand upon said core with experimental code and newer algorithms. Said systems can enable research and implementations of "state of the art" algorithms for use in motor control. One of the methods enabling an FPGA to control multiple motors simultaneously is multiplying a single core until it matches the number of motors. Such a method can increase the resource consumption within the chip. One way computers have been able to utilize resources more effectively has been through the pipelining of instructions [15]. One approach to reduce resource consumption in an FOC system is the introduction of pipelining within multiple components in the FOC core. Studying and analyzing the effect of pipelining FOC on FPGA is therefore a goal of this thesis. The motivation is fueled by the desire to utilize fewer resources while providing a platform for future implementations of more complex functionalities.

## 2 Background and Related Works

### 2.1 FOC

Field Oriented Control, in short FOC, is a control methodology for BLDC motors [20]. FOC works by applying a magnetic field to the rotor that is  $90^\circ$  degrees on the rotor's magnetic field. When this is done correctly we get the maximum efficiency out of the current we send through the motor, as the torque is applied perpendicular to the motor and no torque repels or contracts towards the center of rotation [11]. A FOC system measures the currents in the electrical coils and transforms them into the  $I_q, I_d$  domain, where the d axis follows the rotor and the q axis is normal to the d-vector. This is done through the Clarke [4] and park [17] transformations. The set-point of the currents  $I_q$  and  $I_d$  are controlled by the user or an outer control loop for positioning/velocity. An inner controller/ model uses the setpoint and measurements to calculate what voltages to apply in the d,q domain following the rotor. The set-point values for this controller are often set to  $I_q = I_{desired}$  and  $I_d = 0$  as we want the induced current to generate torque. An inverse park transformation is done to convert our vectors to stationary frame ( $\alpha, \beta$ ). The deduced components are then used in a PWM/PDM creation scheme. The method of PWM/PDM creation may vary from implementation to implementation, but some common ones are SPWM [19] and SVPWM. Both of the mentioned schemes create a vector with the magnetic coils for a field that rotates the rotor.

### 2.2 FPGA-Based Robotics and Automation

An article on "fpgainsights" starts with the statement: "Innovation is king in the rapidly changing industries of robotics and automation. Hardware and software distinctions are becoming increasingly hazy because of Field-Programmable Gate Arrays (FPGAs), which have become essential parts. Robots are now equipped with FPGAs, which enable real-time data processing, quick execution of sophisticated algorithms, and quick environment adaptation." [18]. In this article, it is concluded that

FPGAs have started a new area within the field of robotics and automation. Throughout the article, multiple applications of FPGAs are mentioned. One such application mentioned is Real-Time control, which includes motor control and control loops.

### 2.3 A Survey of FPGA-Based Robotic Computing

The survey named "A Survey of FPGA-Based Robotic Computing" by Zishen Wan and Bo Yu et al.[21] provides a comprehensive overview of FPGA-based robotics and the previous research conducted in this domain. The survey discusses the benefits of FPGA and FPGA + SoC implementations over traditional CPU and GPU implementations. During the survey, a focus has been on the acceleration of robotic application workloads, perception, localization, and planning and control<sup>1</sup>. The survey indicates that FPGAs can be well suited for robotics and that "FPGA can achieve more than 10x better performance and energy efficiency compared to the CPU and GPU implementations." for some specific implementations. It is also mentioned that "the authors believe that FPGAs are the best compute substrate for robotic applications [...] robotic algorithms are still evolving rapidly, and thus any ASIC-based accelerator will be months or even years behind the state-of-the-art algorithms". However, it is also mentioned that FPGAs are not the mainstream platform for robotics as they are harder to program, and the supply of FPGA engineers is limited.

### 2.4 Rapid prototyping

A multi-axis FOC system was created in the thesis "Rapid prototyping -development, and evaluation of Field Oriented Control using LabView FPGA" by Joakim E. and Luciano H. [8]. Their report concluded that controlling multiple motors with FOC using the same FOC loop is possible without losing performance. However, it is stated that due to timing problems in the multi-axis implementation, they could not control more than two motors simultaneously. They also concluded that if optimizations were to be made, it would be possible to control up to four motors. The new limiting factor would then originate from a limitation in the amount of digital IO. A total of two designs were created using LabView [22]. One was designed for single-axis control, while the other supported multi-axis control.

## 3 Implementation

Several HDL files had to be created to implement a pipelined FOC core. The Hardware Description Language of choice was VHDL 2008. The multiple modules included in the design have their own respective file and have some configuration possibilities through a configuration VHDL file. The inputs and outputs from the core have some special data types that scale their width with the number of motors selected in the configuration file. Those data types mainly consist of arrays of signed/unsigned numbers and arrays of logic vectors. The input and output width from the processing system and the sensors can be defined in a configuration file. The FOC-core and all its constituent modules can be found at [1], representing my original work. More information can be found in the thesis uploaded to the same GitHub page.

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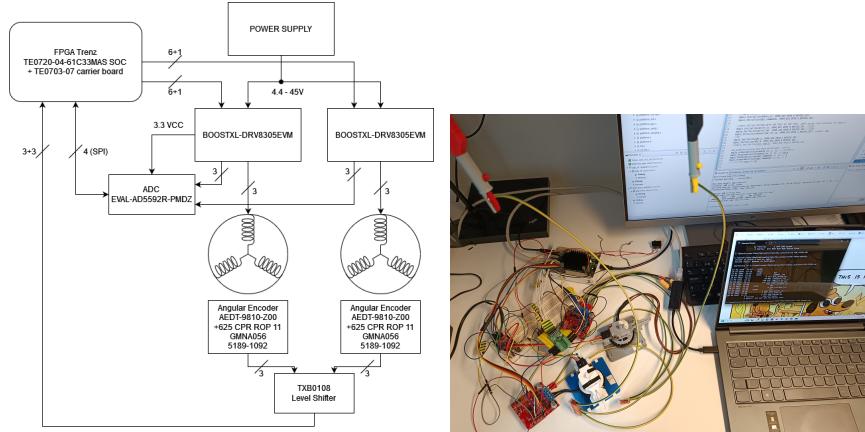
<sup>1</sup>computation of how the robot should maneuver

### 3.1 Hardware

The hardware used in for the operation of two BLDC motors are:

- 1x Trenz TE0720-04-61C33MAS [10]
- 2x T-MOTOR MN4004-21 KV400 [16]
- 2x Texas Instruments BOOSTXL-DRV8305EVM [2]
- 2x (AEDT-9810-Z00 + 625 VPR ROP GMNA056 5189-1092) [13]
- 1x 8-channel Bi-directional Logic Level Converter [14]
- 1x EVAL-AD5592R-PMDZ-ND [9]
- 1x Generic powersupply in the range 1-45V
- 6x 4.7 kΩ resistor
- Nx Jumperwire + Breadboard

The hardware was set up according to diagram 1a



### 3.2 FOC core

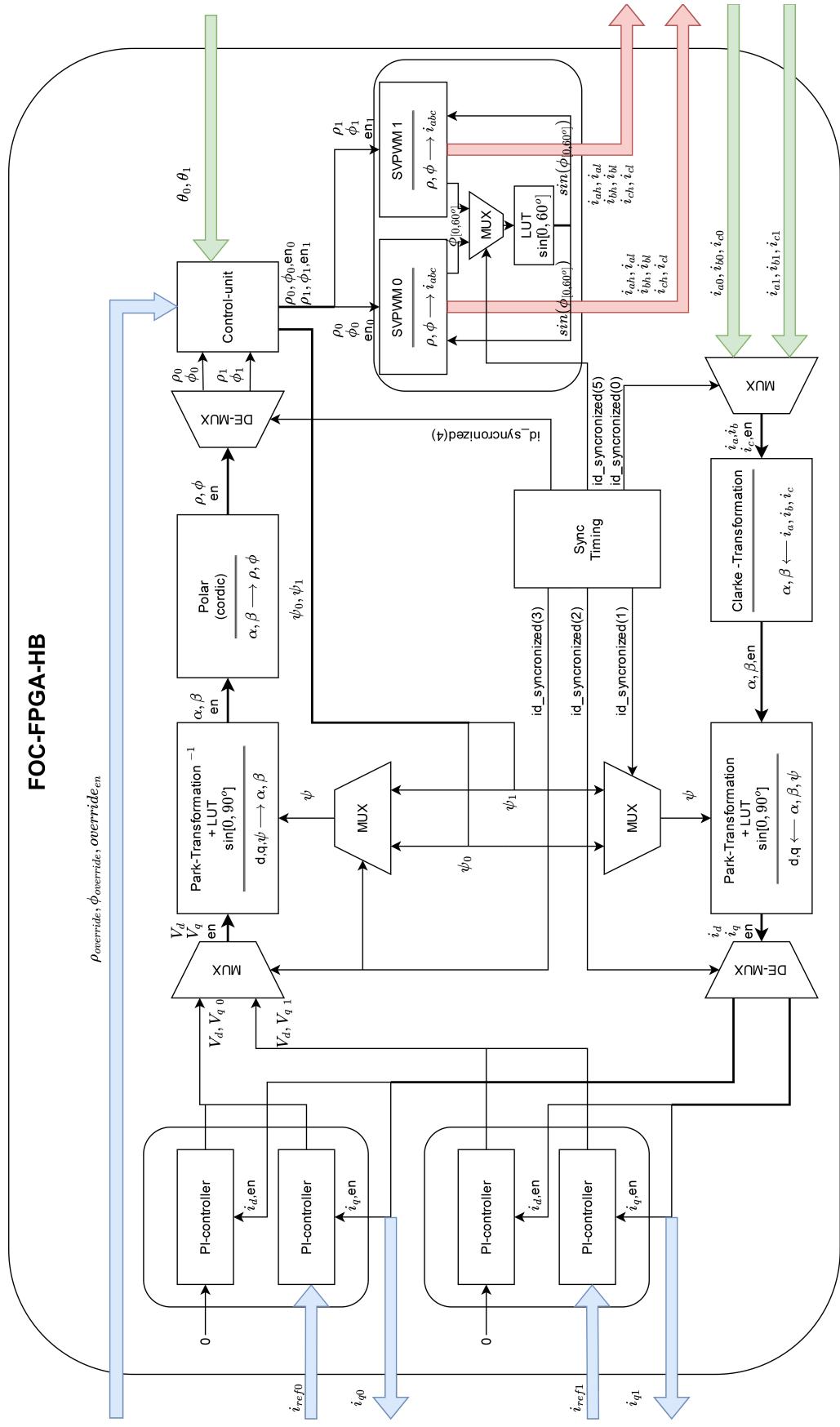


Figure 2: A diagram over the FOC core that has been implemented. The symbols used within the diagram are explained in table 1

Symbol	Explanation
$i_{ref}$	Desired current draw
$i_q$	Current draw along q in d,q - frame
$i_d$	Current draw along d in d,q - frame
$V_q$	Voltage along q in d,q - frame
$V_d$	Voltage along d in d,q - frame
$\psi_m$	Electrical angle for motor m
$\alpha$	Position $\alpha$ in $\alpha, \beta$ - frame
$\beta$	Position $\beta$ in $\alpha, \beta$ - frame (Electrical)
$\rho$	Amplitude in polar-coordinate frame
$\phi$	Angle in polar-coordinate frame
$\theta_n$	Mechanical angle for motor n
en	Strobed enable signal
$override_{en}$	Enable signal for override. If 1 then $\rho_{override}$ and $\phi_{override}$ is used for control instead of iq
id_synchronized(n)	Synchronization id signal for shared logic. At position n motor m is being calculated
$i_{am}$	Current in coil a for motor m
$i_{bm}$	Current in coil b for motor m
$i_{cm}$	Current in coil c for motor m
$i_{ah}, i_{al}$	PWM signal for $a_{high}$ and $a_{low}$ output
$i_{bh}, i_{bl}$	PWM signal for $b_{high}$ and $b_{low}$ output
$i_{ch}, i_{cl}$	PWM signal for $c_{high}$ and $c_{low}$ output
LUT $\sin[0, x^\circ]$	LUT containing sinusoidal values for angles between 0 and $x^\circ$
Blue arrow in	Data from outer control-system into core for control
Blue arrow out	Data from core to outer control-system
Green arrow	Sensor data
Red arrow	PWM Signals

Table 1: Symbols used within the diagram of the FOC core (figure 2)

## 4 Experiments and results

The experiments conducted for the main thesis found at [1] consisted of creating a pipelined core for FOC. The core was then mapped to physical IO pins on an FPGA to constrain the design into valid real-world implementations. After an implementation in Vivado had been created, a series of reports were created: Power, Utilization, and Timing reports. An image of the implementation on the device was taken. For each subsequent implementation, the number of motors controlled by the FOC was increased by one. An increase by one motor meant an additional 16-bit AXI GPIO interface needed to be added to control the  $i_q$  parameter. The IO required by the motor was also mapped to physical pins.

The implementations for 1 and 2 motors were tested in the real world to ensure they functioned correctly. The real-world sanity test consisted of programming the SoC and FPGA and connecting an external computer to send instructions. The external computer sent instructions for setting  $K_p=3000$ ,  $K_i = 0$ , and  $i_q = 200$  to the SoC. Note that the  $K_p, K_i$  values used in the PI controller have not been tuned, nor should they be used in a final product. The sanity test was conducted by visually inspecting the motor's rotation and sending the values  $i_q = -200$  and  $i_q = 400$  to the core. Both motors were tested simultaneously at different velocities/currents. The velocities were limited by internal friction and current draw. Implementations with quantities of motors exceeding two have not been tested due to time and availability limitations. The Utilization report was exported to spreadsheet (.xlsx) files for analyzing the consumption of slice LUTs, Slice Registers, and DSPs. The timing report was only used to verify that the logic could run at 100MHz, which was specified in the timing constraints.

### 4.1 Results

The total height of the bar plots is the total resource usage within the mentioned design. The Block Design mentioned in figure 3a, 3b and 4a shows the resources used for AXI interfaces and SoC that were used to gather instructions from an external computer. The compatibility layer consists of the components placed outside the core. Such components include the conversion of angles with the rotary encoder, an ADC SPI interface and the conversion and mapping of currents.

"**Shared logic**" in plot 4b, 5a and 5b contains modules: Clarke, Park, Inverse Park, Cordic, Control unit, all the Sinusoidal LUTs and the FOC-Top module . The "**Non-Shared logic**" contains the SVPWM modules and the PI controllers as these modules need 1 and 2 instantiations per motor in the system. The total of Shared + Non-Shared logic is contained within the FOC-Core (Green in plot 3a, 3b and 4a).

Figure 6 illustrates the resource usage in the Trenz FPGA, reported as a percentage. A usage of 100% indicates the utilization of all available resources within the specified resource type. The FPGA contains 53200 slice-LUTs, 106400 Slice registers, 220 DSPs, and 150 IO ports.

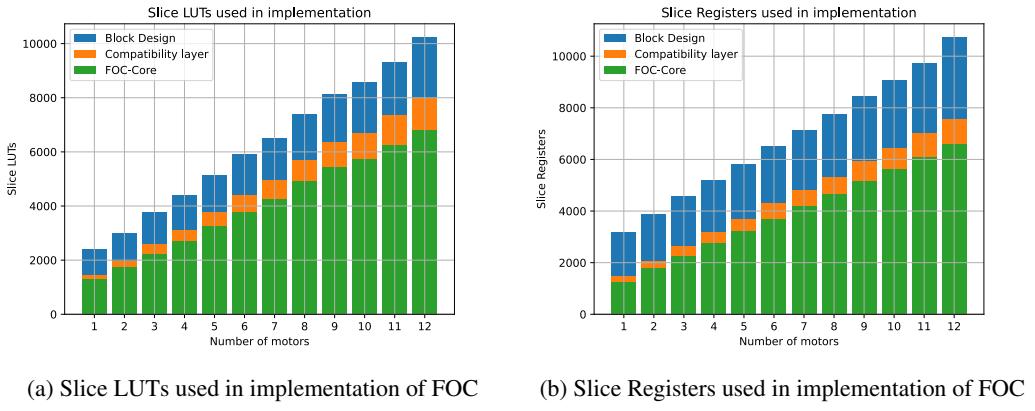


Figure 3: Resource usage in implementation

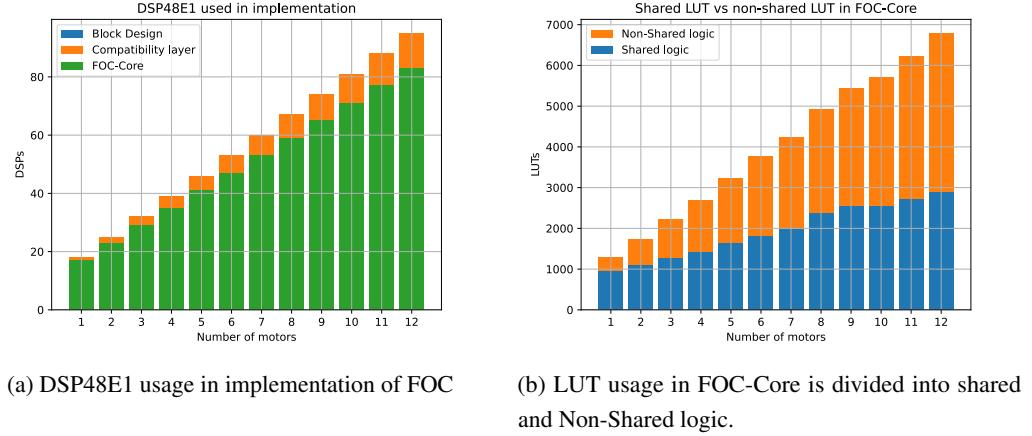


Figure 4: DSP usage in implementation (Left), Shared vs. Non-shared logic LUT usage (Right)

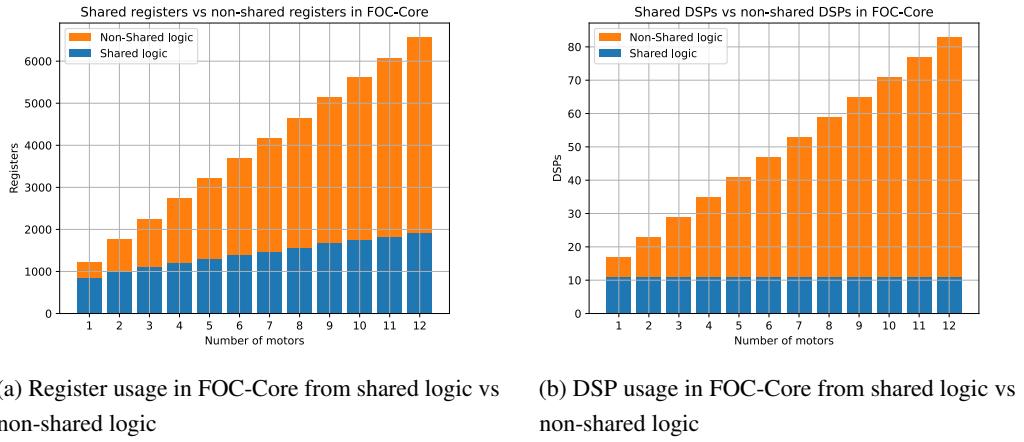


Figure 5: Shared vs Non-shared logic.

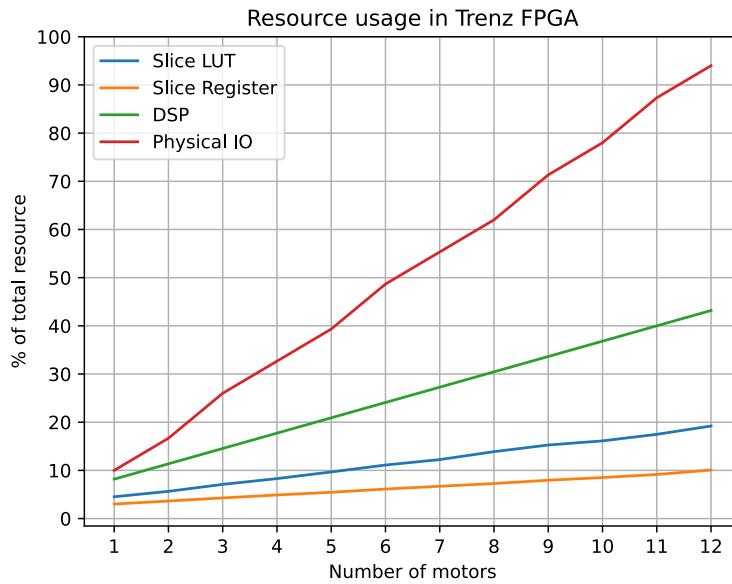


Figure 6: Quantity of resources consumed by the design on the Trenz FPGA. The quantity is given as a percentage. The FPGA contains 53200 slice-LUTs, 106400 Slice registers, 220 DSPs, and 150 IO ports.

For the discussion and Conclusion, please read visit the full thesis at [1].

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