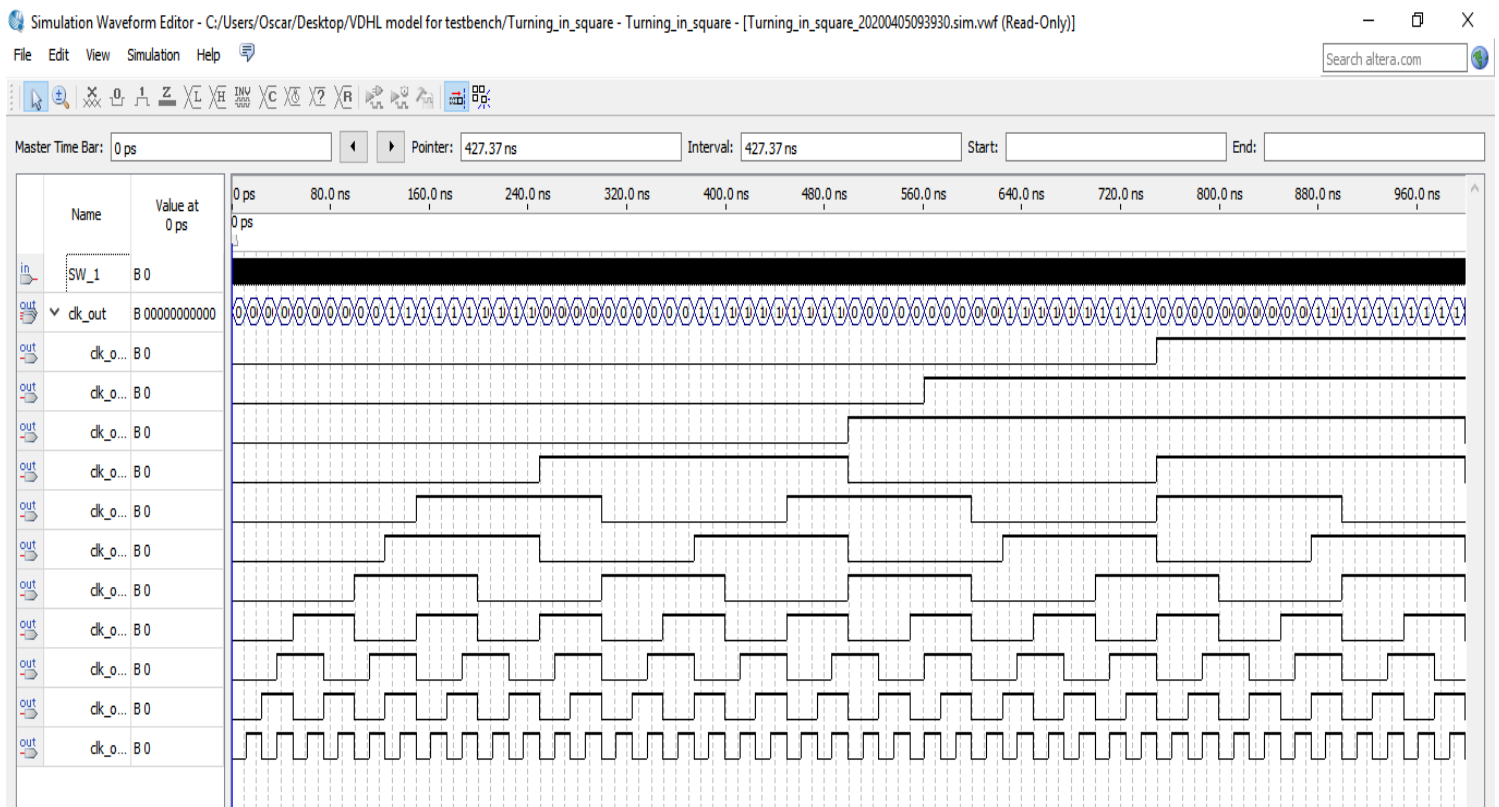
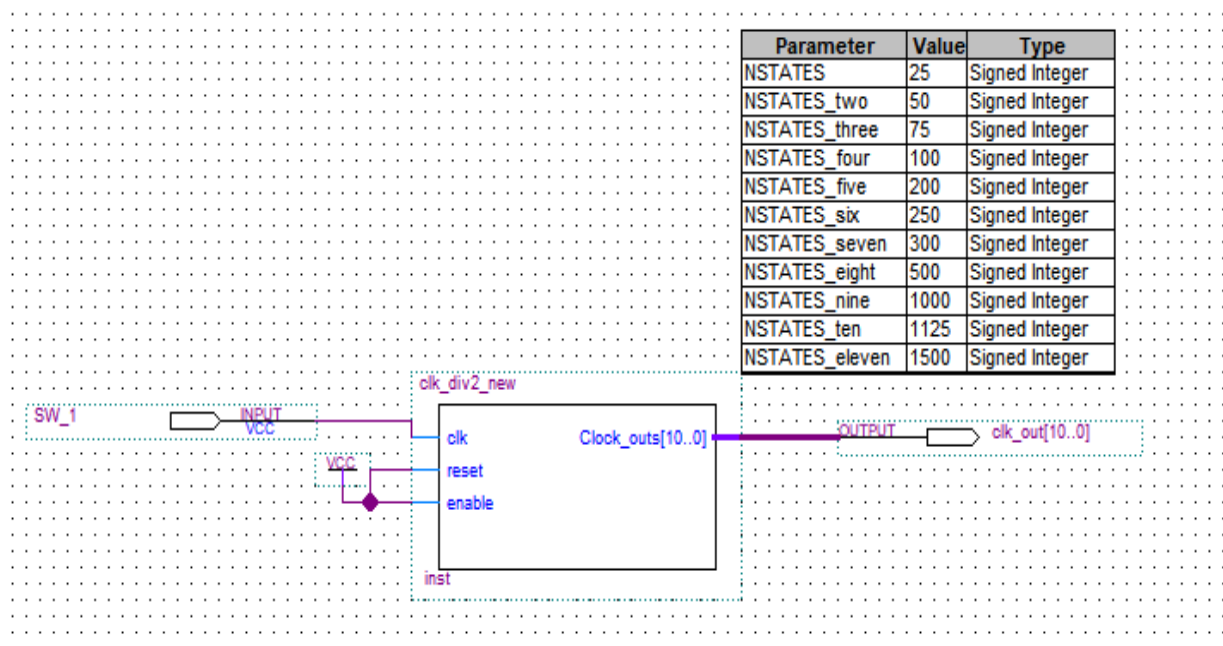


10 Clocks



Where SW_1 represents an input clock and the others are the clockouts.



The code for this is called 10 clocks on a notepad file.

The screenshot displays a Verilog HDL code editor with a circuit diagram for a 2-bit adder. The circuit includes two 4-bit accumulators (inst14acc and inst15), a 2-bit FSM (inst24), and various logic gates (AND2, OR2, NOT1). Inputs include HAIL_one, HAIL_two, reset, and VCC. Outputs include clkout_one, clkout_two, and clkout. The circuit is designed to add two 2-bit numbers and output the result in a 4-bit accumulator.

Block diagram of the Hall sensors module (inst13). The module has three inputs: Hall_one, Hall_two, and reset, all connected to VCC. It has five outputs: clkout_one, clk_first_fsm, Forwads, turn, and clkout_two, all connected to OUTPUT. The module is labeled inst13.

Simulation Waveform Editor - C:/Users/Oscar/Desktop/VD/IL model for testbench/Turning_in_square - Turning_in_square - [Turning_in_square_20200405110053.sim.vwf (Read-Only)]

File Edit View Simulation Help

Search altera.com

Master Time Bar: 0 ps Pointer: 106.92 ns Interval: 106.92 ns Start: End:

Name	Value at 0 ps
hall	B 00
Reset	B 0
clk_before_fsm	B 1
clk_out_one	B 0
clk_out_two	B 0
Forwards	B 1
Turn	B 0

Timing diagram showing signals over time (60.0 ns to 200.0 ns). The signals are: hall (B 00), Reset (B 0), clk_before_fsm (B 1), clk_out_one (B 0), clk_out_two (B 0), Forwards (B 1), and Turn (B 0).