题目 4 方法 1

1. RTL 代码描述

3-8 译码器模块采用题目 3 中模块

模 8 计数器模块

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
entity counter_8 is
--  Port ( );
port(
clk: in std_logic;
count: out std_logic_vector(2 downto 0)
);
end counter_8;

architecture Behavioral of counter_8 is
signal tmp:std_logic_vector(2 downto 0):="000";
begin
count<=tmp;
process(clk)
begin
if(clk'event and clk='1') then
    if tmp="111" then
        tmp<="000";
    else
        tmp<=tmp+1;
    end if;
end if;
end process;

end Behavioral;
```

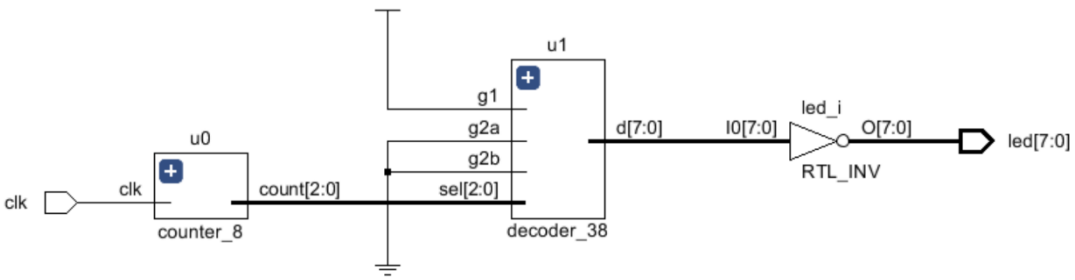
顶层模块

38 译码器为低电平有效，调用输出需要取反得到 led 输出

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity led_8 is
--  Port ( );
port(
clk: in std_logic;
led : out std_logic_vector(7 downto 0)
);
end led_8;

architecture Behavioral of led_8 is
component decoder_38
port(
g1,g2a,g2b: in std_logic;
sel: in std_logic_vector(2 downto 0);
d: out std_logic_vector(7 downto 0)
);
end component;
component counter_8
port(
clk: in std_logic;
count: out std_logic_vector(2 downto 0)
);
end component;
signal count: std_logic_vector(2 downto 0):="000";
signal led_tmp: std_logic_vector(7 downto 0):="11111110";
begin
u0: counter_8 port map(
clk=>clk,
count=>count
);
u1: decoder_38 port map(
g1=>'1',
g2a=>'0',
g2b=>'0',
sel=>count,
d=>led_tmp
);
led<=not led_tmp;
end Behavioral;
```

2.行为级描述原理图

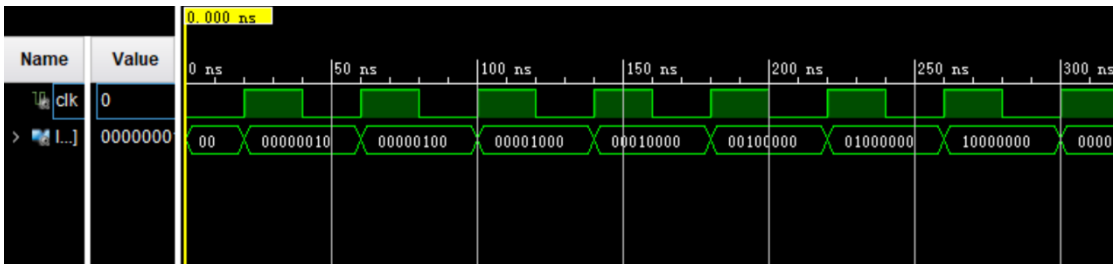


3.tb 测试代码（为加速仿真，将时间间隔设置为 20ns,实际应为 1s）

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity led_testbench is
--  Port ( );
end led_testbench;

architecture Behavioral of led_testbench is
component led_8
port(
clk: in std_logic;
led : out std_logic_vector(7 downto 0)
);
end component;
signal clk: std_logic :='0';
signal led: std_logic_vector(7 downto 0) :="00000001";
begin
u0:led_8 port map(
clk=>clk,
led=>led
);
process
begin
wait for 20ns;
clk<=not clk;
end process;
end Behavioral;
```

4.仿真波形图



5.RTL 综合后原理图

6.资源占用结果

Utilization **Post-Synthesis** | Post-Implementation

Graph | **Table**

Resource	Estimation	Available	Utilization...
LUT	6	20800	0.03
FF	3	41600	0.01
IO	9	170	5.29
BUFG	1	32	3.13

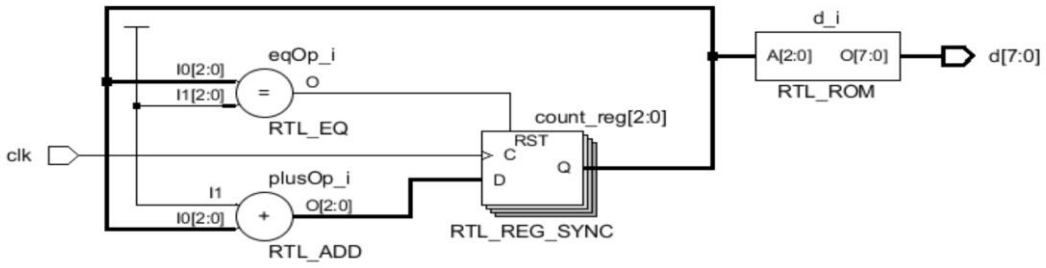
题目四 方法二

1. RTL 代码描述

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
entity led_8_2 is
port(
clk:in std_logic;
d: out std_logic_vector(7 downto 0)
);
end led_8_2;

architecture Behavioral of led_8_2 is
signal count: std_logic_vector(2 downto 0):="000";
begin
process(clk)
begin
if (clk'event and clk='1')then
    if(count="111") then
        count<="000";
    else
        count<=count+1;
    end if;
end if;
end process;
process(count)
begin
case count is
    when "000" => d<="00000001";
    when "001" => d<="00000010";
    when "010" => d<="00000100";
    when "011" => d<="00001000";
    when "100" => d<="00010000";
    when "101" => d<="00100000";
    when "110" => d<="01000000";
    when "111" => d<="10000000";
    when others => d<="00000000";
end case;
end process;
end Behavioral;
```

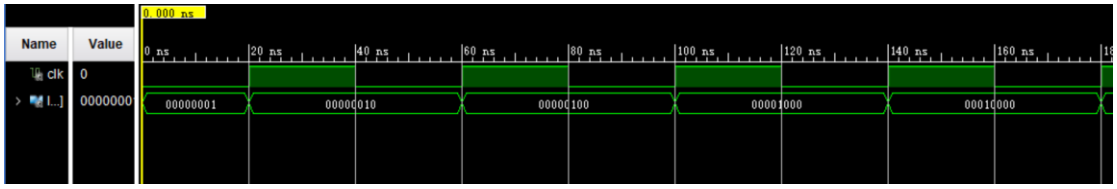
2. 行为级描述原理图



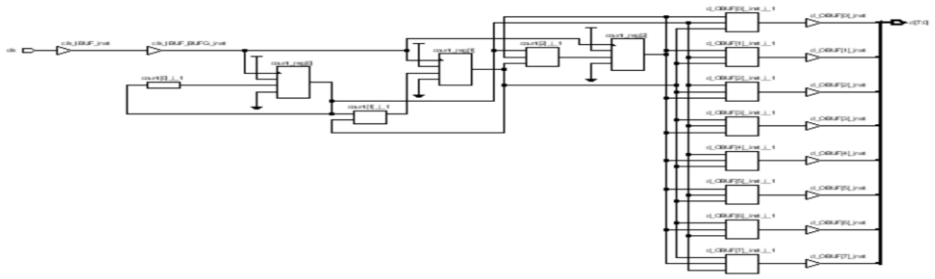
3. 3.tb 测试代码（为加速仿真，将时间间隔设置为 20ns,实际应为 1s）

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity led_testbench is
end led_testbench;
architecture Behavioral of led_testbench is
component led_8_2
port(
clk: in std_logic;
d : out std_logic_vector(7 downto 0)
);
end component;
signal clk: std_logic :='0';
signal led: std_logic_vector(7 downto 0) :="00000001";
begin
u0:led_8_2 port map(
clk=>clk,
d=>led
);
process
begin
wait for 20ns;
clk<=not clk;
end process;
end Behavioral;
```

4. 仿真波形图



5. RTL 综合后原理图



6．资源占用结果

Utilization **Post-Synthesis** | Post-Implementation

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Resource	Estimation	Available	Utilization...
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