

# MEC: An Open-source Fine-grained Mapping Equivalence Checking Tool for FPGA

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**Abstract**—Technology mapping is an essential step in EDA flow. However, the function of the circuit may be changed after technology mapping, and equivalence checking (EC) based verification is highly necessary. The traditional EC method has significant time and resource constraints, making it only feasible to carry out at a coarse-grained level. To make it efficient for technology mapping, we propose a fine-grained method called MEC, which leverages a combination of two approaches to significantly reduce the time cost of verification. The local block verification approach performs fast verification and the global graph cover approach guarantees correctness. The proposed method is rigorously tested and compared to three EC tools, and the results show that MEC technique offers a substantial improvement in speed. MEC not only offers a faster and more efficient way of performing EC on technology mapping but also opens up new opportunities for more fine-grained verification in the future.

**Index Terms**—Technology mapping, equivalence checking, Fine-grained, FPGA

## I. INTRODUCTION

Technology mapping, an essential process in logic synthesis, transforms a technology-independent logic network into a network with logic blocks. In FPGA technology mapping [1], the logic network is transformed into a  $k$ -LUT network, where each  $k$ -LUT block can represent any Boolean function with an input size less than or equal to  $k$ , due to the reconfigurability of the LUTs which are similar to SRAMs. Making the verification process of technology mapping more cost-effective and having a debug tool available are important considerations to improve the efficiency and accuracy of the process.

Equivalence Checking is also an important step of Electronic Design Automation (EDA) flow and is commonly used to prove that two representations of a digital circuit exhibit exactly the same behavior. It can also guarantee the correctness of technology mapping. As illustrated in Fig. 1, EC is usually performed after each step to ensure that the behavior has not changed during the current step. And the coarse-grained EC directly performs verification on the output of two circuits. With the growth in the size of Very Large Scale Integrated (VLSI) Circuits, the time spent on the verification step has increased to almost 70% [2] in IC-flow.

Reducing the time of the EDA flow can be achieved by making the verification process more efficient, and there have been numerous efforts in this direction. Goldberg et al. [3] introduced SAT to solve the equivalence checking prob-

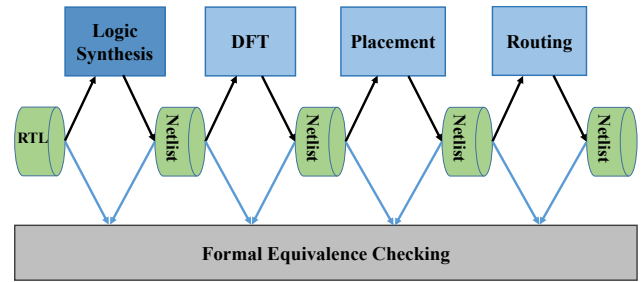


Fig. 1. Verification for EDA flow.

lem and showed that it is a more robust and flexible engine for Boolean reasoning than BDD-based methods. And this led to the widespread use of SAT-based equivalence checking. Cook showed that the SAT problem is NP-complete in [4], triggering further research aimed at reducing the complexity of the problem for SAT solvers. This also means that cost time can be reduced by reducing the size of the circuit. Alan et al. [5] mainly reduced the cost by using more intelligent simulation and introducing SAT-sweep to find function-equivalent node-pairs to reduce the solution space, further enhancing the SAT-based method. There are also other approaches to speed up verification. Feng et al. [6] reduced the checking scale by early inserting cutpoints into the RTL, allowing for verification through these cutpoints, but this approach carries the risk of changing the design.

It is possible to conduct fine-grained verification if the verification method can be made more efficient. This paper focuses on the equivalence checking of FPGA technology mapping in logic synthesis. Inspired by [7], which applies FPGA technology mapping to speed up SAT solver, we can make a fast verification by incrementally checking the equivalence of the mapping result network and its original network in topological order.

Our contributions can be divided into three parts:

- We prove that the verification on technology mapping can be based on local-block-verification and global-graph-cover, and propose a highly efficient method for EC on technology mapping.
- We release a debug tool for technology mapping, MEC<sup>1</sup>, and it can also expose the detailed equivalence information for the local block to make a quick debug.
- We compare MEC with three EC tools, the results of the experiment show that MEC offers a substantial

<sup>1</sup><https://github.com/nlwmode/MEC>.

improvement in speed.

The rest of this paper is organized as follows: Section II provides background information on technology mapping and SAT-based equivalence checking. Section III gives an illustration of the details of our proposed tool, MEC. Section IV shows the framework of our work. Section V presents the results of our experiments on equivalence checking during technology mapping. Finally, conclusion and future work are summarized in Section VI.

## II. PRELIMINARIES

In this section, we consider the verification on FPGA technology mapping. And we will introduce some of the basics we might need later.

A Boolean Network is a *directed acyclic graph* (DAG) which the nodes corresponding to logic gates and the edges corresponding to wires between gates. A node  $n$  has zero or more *fanins* and *fanouts*, fanins mean the nodes that flowed in and fanouts mean the nodes that flowed out. The *primary inputs* (PIs) are nodes without fanins and the *primary outputs* (POs) are nodes without fanouts. A *fanin/fanout cone* of node  $n$  is the subset nodes of the network reachable through the fanin/fanout edges from  $n$ .

As for choice-related computation, we need to extend the traditional DAG with additional properties of displayed function-equivalent or function-complementary edges between nodes. The function-equivalent edges refer to the bi-directional solid arrow line and the function-complementary edges refer to the bi-directional dotted arrow lines. A *representative node* of a network is the node without any displayed function-equivalent or function-complement edges in a network. The *choice class* is the set of nodes that are displayed function-equivalent or function-complementary in a network. And only one representative node is needed for this class to connect all its fanouts. The *choice node* is the node that is not the representative node in a choice class. The *regular network* is the network that all the nodes are representative nodes, and it does not have any choice class. The *choice network* is the network with some choice classes. In a choice network, nodes in a choice class are connected by a linked list and are connected by a bi-directional solid arrow if the choice node is function-equivalent to its representative node. If not, the arrow is bi-directional dotted.

For cut-based technology mapping, a *cut*  $c$  of node  $n$  is a subset of nodes of transitive fanin cone that each path from a PI to  $n$  passes through at least one node of  $c$ , in short,  $n$  is the root, and  $c$  are the leaves. A *trivial cut* of node  $n$  is the node itself. A *non-trivial cut* includes all the nodes that are found on the paths from the root to leaves. A *k-bounded network* is a network where the number of fanins of any node that does not exceed  $k$ , and also a cut is *k-feasible* if the number of nodes in it does not exceed  $k$ .

A *mapping* of a network means that each non-PI node assigned a  $k$ -feasible cut also called *representative cut*. So we can easily get the mapping result for each non-PI node's representative cut from POs to PIs incrementally, and the reached nodes are used, the covered nodes are hidden in a cut as an internal part of logic block.

A *miter*  $m$  of two Boolean networks  $f$  and  $g$ ,  $f$  and  $g$  have the same PIs and POs, is the merged network that adding XOR gates to the same corresponding outputs for  $f$

and  $g$ , then adding a big OR gate for these XOR gates. It is easy to do equivalence checking by the miter network.

## III. TRADITIONAL TECHNOLOGY MAPPING AND VERIFICATION

In this section, we will outline the basic flow for FPGA technology mapping and provide details on SAT-based equivalence checking.

### A. Traditional FPGA Technology Mapping

Algorithm 1 depicts the traditional FPGA technology mapping flow as implemented in ABC [8]. In the following subsections, we will delve into the details of each step of the algorithm process.

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#### Algorithm 1 Traditional FPGA technology mapping

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**Input:** Network  $G$ , cut size  $k$   
**Output:** Mapping result  $mr$   
 /\* merge the internal optimized networks to reduce bias \*/  
 1:  $CG \leftarrow \text{compute\_choice\_network}(G)$   
 /\* compute all  $k$ -feasible cuts at each node \*/  
 2:  $\text{cut\_enumeration}(CG, k)$   
 /\* compute min-depth representative cut for each node \*/  
 3:  $\text{depth\_oriented\_mapping}(CG, k)$   
 /\* update representative cut at each node to optimize area \*/  
 4:  $\text{area\_recovery}(CG, k)$   
 /\* compute the set of nodes used in the final mapping \*/  
 5:  $mr \leftarrow \text{derive\_final\_mapping}(CG, k)$   
 6: **return**  $mr$

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#### 1) Choice network generation:

Due to the bias [9] of technology-independent optimizations, meaning that the lowest-cost network may not obtain the best mapping result, we can reduce the bias by merging the internal optimized networks into a choice network that retains the local structure of each selected network. In this way, we can obtain a better mapping result compared to each individual network.

#### 2) Cut enumeration:

Cut enumeration [10] serves as the foundation for cut-based optimization and technology mapping. Given two cut sets,  $CS_1$  and  $CS_2$ , the merge operation of the cut sets,  $CS_1 \diamond CS_2$ , is defined as:

$$CS_1 \diamond CS_2 = \{u \cup v | u \in CS_1, v \in CS_2\} \quad (1)$$

As for technology mapping, we also need to add one constraint to equation (1):  $\{|u \cup v| \leq k\}$  which means that the new merged cut's size is no more than  $k$ . And we can define the equation to compute each node's  $k$ -feasible cut: for convenience, let  $\Phi(n)$  be the set of  $k$ -feasible cuts for two-input node  $n$ ,  $n_1$  and  $n_2$  denote to  $n$ 's fanins:

$$\Phi(n) = \left\{ \begin{array}{l} \{\{n\}\} : n \in PIs \\ \{\{n\}\} \cup \Phi(n_1) \diamond \Phi(n_2) : \text{otherwise} \end{array} \right\}. \quad (2)$$

To begin with, each node will be assigned a trivial cut consisting of itself. Then, the cut set for each node will be generated incrementally in topological order by merging the cut sets of its children, according to equation (2). To balance the trade-off between memory, time, and mapping result, the priority cut algorithm [11] is usually adopted, which only saves better cut sets according to some sorting criteria for optimization or technology mapping.

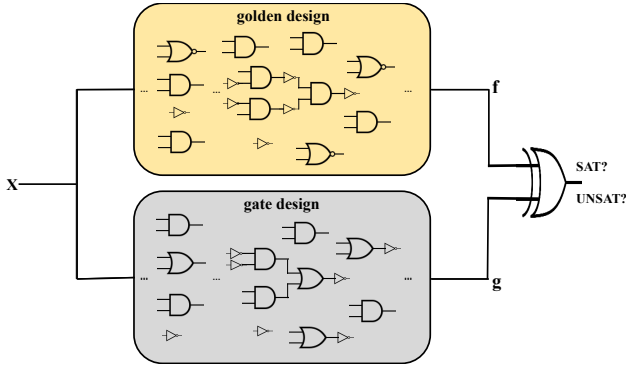


Fig. 2. The miter network for  $f$  and  $g$ .

### 3) Derive mapping result:

Depth-oriented mapping provides an initial representative cut assignment for each node to achieve a depth-optimal mapping result. However, there is still room for improvement in terms of area. The area recovery step involves finding a more area-efficient cut to be used as the representative cut, while maintaining the constraint of depth.

After the steps above are completed, we can extract the mapping result by traversing the network in reverse topological order and collecting the representative cuts of the used nodes. This step ensures that the entire network is covered. It should be noted that trivial cuts can not be representative cuts for internal nodes, as we must ensure full coverage of the network.

## B. SAT-based Equivalence Checking

Fig.2 illustrates the scheme for SAT-based equivalence checking. Due to the property of XOR gates, the equivalence of  $f$  and  $g$  can easily be checked by checking the satisfiability of the miter network. In detail, the process involves first transforming the miter network into CNF form using the Tseitin transformation [12] and then checking it with SAT solver.

We can say that  $f$  and  $g$  are equivalent only if the miter network is UNSAT, meaning that  $f$  and  $g$  have the same output for any input signals. On the other hand, if the miter network is SAT, it means that there are some input signals that result in different outputs for  $f$  and  $g$ , and therefore  $f$  and  $g$  are non-equivalent.

## IV. VERIFICATION ON TECHNOLOGY MAPPING

In this section, we will illustrate the details of our proposed algorithm for verification on FPGA technology mapping, MEC. We will also prove that the results obtained from our algorithm are equivalent to those obtained from the miter network.

Our core idea is to reduce the size of the problem, and we can optimize the checking problem by combining local block verification and global graph cover. Miter-based equivalence checking for the two networks is time-consuming for technology mapping and therefore not practical for verification here. However, our proposed algorithm, logic block-based equivalence checking, can produce the same results in much less time and also provides local structure information for debugging technology mapping.

### A. Equivalence Checking on Technology Mapping

Algorithm 2 displays the complete flow of our proposed algorithm. We emphasize that our proposed algorithm can be adopted to combinational network and sequential network. Theorem 1 also confirms the correctness of our method's checking results.

**Definition 1.** (*greatest node set (GNS)*). Let  $N$  be a set of nodes of original network ( $OG$ ), and  $\preceq$  be the partial ordering relation referred to the directed edge. If  $(N, \preceq)$  is a partial ordering set with only a greatest element  $ge \in N$ . We call above greatest element  $ge$  as greatest node, and all greatest nodes compose greatest node set ( $GNS$ ).

**Theorem 1.** A mapping network ( $MG$ ) equivalents to its original network ( $OG$ ) if each logic block in  $MG$  equivalents to its covered network.

**Proof.** A mapping is a set of representative cuts for used nodes in the network, and the used nodes are the  $GNS$  in  $OG$ . And the corresponding nodes  $CNS$  to  $GNS$  in  $MG$  can be easily obtained during deriving mapping.  $GNS$  guarantees the global cover and its internal nodes are only connecting fanin cone and fanout cone, and have no logic function. Therefore, we can get the verification result of  $MG$  and  $OG$  by checking the equivalence based on  $GNS$  and  $CNS$  in topological order.

**Definition 2.** (*corresponding pair set (CPS)*). For a node pair  $(i, j)$ , if  $i \in GNS$  in  $OG$ , and  $j$  is its corresponding node in  $MG$ , we call this node pair as corresponding pair, and  $CPS$  is the set of corresponding pair.

### Algorithm 2 Verification on Technology Mapping

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**Input:** network  $OG$  before mapping,  
mapping result network  $MG$

**Output:** Equivalent or not

- 1: initialize  $error = false$
- 2: collecting the  $CPS$  for  $OG$  and  $MG$
- 3: topologizing  $CPS$
- 4: **for**  $np$  in  $CPS$  **do**
- 5:     **if**  $error == true$  **then**
- 6:         **return** ! $error$
- 7:     **else**
- 8:          $error = checking\_logic\_block(np, OG, MG)$
- 9:     **end if**
- 10: **end for**
- 11: **return** ! $error$

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#### 1) Equivalence checking on combinational mapping:

As illustrated in Algorithm 2, after technology mapping, we obtain the mapping network  $MG$  for its original network  $OG$ . The variable  $error$  indicates the presence of bugs in the current mapping network. First, we collect the injective corresponding node set  $CPS$  which can expose the corresponding node-pairs between  $OG$  and  $MG$ . The processing order is important because it is meaningless to check for equivalence after node-pair  $np$  if we find that its logic block is not equivalent to its covered network. After ordering the  $CPS$  in a topological manner, we perform the equivalence checking incrementally. If we find that a node's logic block is not equivalent to its covered network in  $CPS$ , the program will return "false"; otherwise, the algorithm will continue checking until the last element in  $CPS$  and return "true". Thus,  $CPS$  guarantees the global cover and the local block checking performs a fast verification.

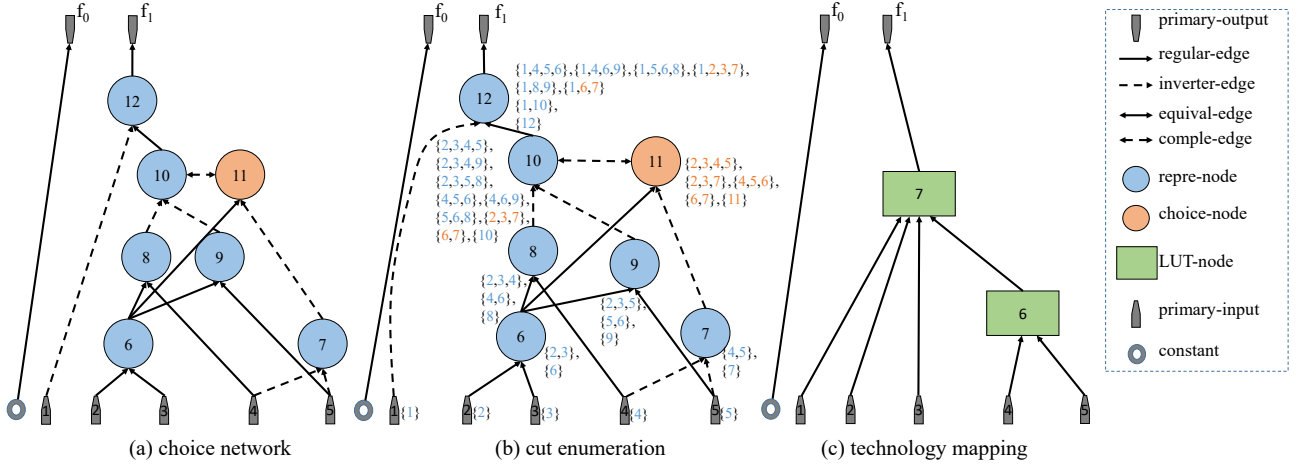


Fig. 3. The technology mapping on choice network.

**Example 1.** Fig. 3 (b) and (c) illustrate the cut enumeration and FPGA technology mapping steps for network  $OG$ . After the multi-iterated cut selection, the best representative cut for each node is determined. Then, the mapping network is derived in reversed topological order, and the ordered node set is  $\{12, 1, 10, 11, 8, 9, 6, 7, 2, 3, 4, 5, 0\}$ . Based on this order vector, cut  $\{1, 2, 3, 7\}$  is selected as the representative cut of node-12 first, and the node set  $\{1, 10, 11, 8, 9, 6, 2, 3, 7\}$  is covered, with the uncovered node set being  $\{7, 4, 5, 0\}$ . Then, cut  $\{4, 5\}$  is selected as the representative cut of node-7 and node-0 is directly connected to the output. Thus, all nodes in  $OG$  are covered, and the mapping network  $MG$  is derived. As for verification on technology mapping, we first collect the injective corresponding node set  $CPS$ , according to the deriving mapping process, and which is  $\{\{12, 7\}, \{7, 6\}, \{0, 0\}\}$ . Next, we sort  $CPS$  in topological order, yielding  $\{\{0, 0\}, \{7, 6\}, \{12, 7\}\}$ . After these steps, we can perform verification for each logic block one by one according to  $CPS$ . Node-0 can be trivially verified because it is a constant node. If a bug is found in  $CPS$  during the checking step, the process will stop and return “false”. Otherwise, it will return “true” once all node-pairs in  $CPS$  have been checked.

#### 2) Equivalence checking on sequential mapping:

Sequential mapping is built upon the combinational mapping method for its combinational network between registers. It is straightforward to prove that equivalence can also be checked using equivalence checking on combinational mapping because the registers will not be altered.

### B. Equivalence Checking on Logic Block

Algorithm 3 shows the details for the equivalence checking on logic block. It is easy to add constraint of logic block for regular networks, but choice networks are different and the difference will be discussed in this part. In order to distinguish it from  $OG$ , the internal node is called block in  $MG$ . And we refer to the  $OG$ 's node in  $np$  as  $fn$  and to the  $MG$ 's node in  $np$  as  $sn$ .

**Definition 3. (regular block).** The *regular block* is a block with one root node and its limited fanin cone, and each node in its cone must be representative node.

**Definition 4. (choice block).** The *choice block* is a block with one root node and its limited fanin cone, and there are some choice nodes in its fanin cone.

### Algorithm 3 checking logic block

**Input:** node-pair  $np$ , network  $OG$  before mapping, mapping result network  $MG$ ,  
**Output:** Equivalent or not  
1: initialize  $error = \text{false}$ , SAT solver  $s$   
2:  $v_1 \leftarrow \text{add\_constraint\_of\_logic\_block}(np, MG, s)$   
3:  $v_2 \leftarrow \text{add\_constraint\_of\_covered\_network}(np, OG, s)$   
4:  $\text{add\_xor\_constraint}(s, v_1, v_2)$   
5: **if**  $s$  is SAT **then**:  
6:      $error = \text{true}$   
7: **else**  
8:      $error = \text{false}$   
9: **end if**  
10: **return** ! $error$

#### 1) Checking for regular block:

As illustrated in Algorithm 3, checking equivalence for a regular block is straightforward. The variable  $error$  indicates that the current logic block is not equivalent to its covered network. First, we add the constraint for the logic block of  $sn$ . The block's truth table can be directly obtained and transformed into Conjunctive Normal Form (CNF) using Boolean operators, so we add this CNF to the SAT solver  $s$  through Tseitin transformation and return a temporary variable  $v_1$  for this logic block. Next, we need to consider adding the constraint of the covered network of the logic block in  $OG$ .

Thanks to the fact that there are no choice classes in  $OG$  for regular network, we can directly traverse from  $fn$  to its block's leaves to collect the covered nodes. The traversed nodes are guaranteed to be the block's covered network due to the property of  $k$ -feasible cuts. Hence, we can add constraints to the covered nodes using Tseitin transformation and return another temporary variable  $v_2$  for root  $sn$ . Finally, we need to add the XOR constraint to  $s$  between  $v_1$  and  $v_2$ , and check the satisfiability of  $s$ . If  $s$  is SAT, it means that some bugs have occurred here, otherwise, this logic block is deemed to be correct.

**Example 2.** As shown in Fig. 3(c), node-6 of  $MG$  is a regular block according to its covered node set  $\{4, 5, 7\}$  in  $OG$ . And we can do logic block verification following



Algorithm 3. In *MG*, we start by adding constraints for block-6. The truth table of block-6 can be directly obtained from the mapping network and is  $\{0001\}$ , and left for the truth table is low-bit. We need to assign the distinct sat ids to the nodes for  $s$ , and the node-4, node-5 and block-6 are assigned the ids 1,2,3. Then we can get the constraints  $((\bar{1} + \bar{3})(\bar{2} + \bar{3})(1 + 2 + 3))$  of block-6's truth table  $\{0001\}$  using Tseitin transformation, and return the sat id of block-6. In *OG*, we also need to assign the distinct sat ids to the covered nodes for  $s$ . node-4 and node-5 are the same in *MG*, so their sat ids are retained, and node-7 is assigned the id 4. We can then add the constraints  $((\bar{1} + \bar{4})(\bar{2} + \bar{4})(1 + 2 + 4))$  for node-4, node-5 and node-7 using Tseitin transformation, and return the sat id of node-7. Finally, we add the xor constraint for the returned sat ids  $\{3,4\}$ , and then solve the  $s$  to get the checked value “true”.

### 2) Checking for choice block:

Choice networks differ from the regular networks on displayed choice class in the network. It is more difficult to add constraints to the covered network by traversing from  $fn$  to the block's leaves in choice networks, as the choice node can break the property of  $k$ -feasible cuts, meaning that it may not be possible to reach the leaves from the root. However, the representative node saves the best cuts of the choice nodes in its choice class, allowing the fanin cone of the choice nodes can be visited by their original fanout cone. Additionally, thanks to the topological order, the covered nodes can be collected from the block's leaves to root  $fn$ , which may result in collecting redundant nodes, but the solver's result remains unaffected. The other steps are the same as in regular networks.

**Example 3.** As shown in Fig. 3(c), it is clear that block-7 of *MG* is a choice block and its exact covered node set is  $\{12,1,11,6,7,2,3\}$  in *OG*. In *MG*, we add the constraints for block-7 first, and its truth table is  $\{0101,0101,0001,0101\}$ . We assign the distinct sat ids to nodes for  $s$ , and node-1, node-2, node-3, block-6 and block-7 are assigned the id  $\{1,2,3,4,5\}$ . Then we get the constraints of its truth table is  $((\bar{1} + 4 + 5)(\bar{1} + \bar{3} + 5)(\bar{1} + \bar{2} + 5)(2 + 3 + 4 + 5)(1 + 5))$ , and we return the sat id of block-7. In *OG*, collecting the covered node set by traversing from root to leaf nodes can be costly when the choice class is large. We first collect the redundant candidate-covered nodes from leaf nodes to the root direction, and the candidate node set is  $\{1,2,3,7,6,11,8,9,12\}$ . Compared to the exact covered nodes above,  $\{8,9\}$  are redundant nodes, but this does not affect the checking result. The candidate node set  $\{7,6,11,8,9,12\}$  is assigned the sat ids  $\{6,7,8,9,10,11\}$ , and  $\{1,2,3\}$  retain their original sat ids. Then, we add the constraints of these candidate-covered nodes by Tseitin transformation until the root node-12, and return the sat id of node-12. Finally, we add the xor constraint for the returned sat ids  $\{5,11\}$ , and then solve the  $s$  to get the checked value “true”.

## V. MEC FRAMEWORK

In this section, we will briefly introduce the system component diagrams required for FPGA technology mapping and the parts related to MEC are the ones that we mainly focus on.

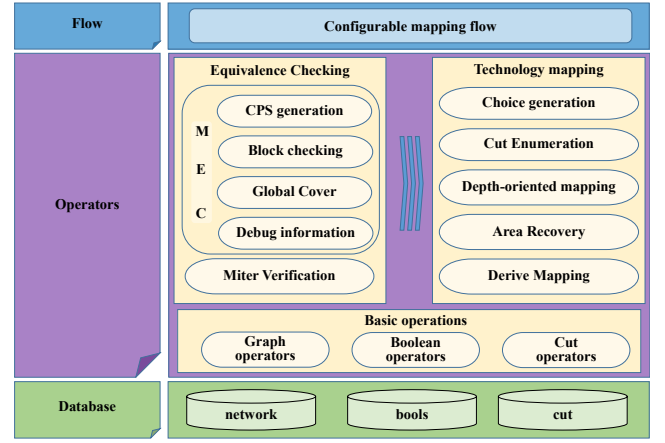


Fig. 4. The framework of MEC.

Fig. 4 shows our system components for the technology mapping process. It consists of three layers: the database layer, operators layer and flow layer. The database layer is consisted of basic data structures, mainly about the networks, cut and Boolean logic. Therefore, it can support graph-based manipulation and cut-based operators. The bools mainly includes truth table, SOP and CNF. The upper layer is the operators layer. With the support of the basic database, we can implement the FPGA technology mapping and equivalence checking. The top layer is the flow layer. We can make the mapping flow configurable through this layer. So it is convenient for the user to do more exploration for the mapping flow.

We will focus on the technology mapping flow supported by MEC. The input is a network for a combinational circuit. First, We will generate the choice network by merging the selected internal optimized networks. Next, we perform cut enumeration and the following is the multi-iteration and multi-criteria cut sorting to update the representative cut for each node. In the middle of this process, we can directly call MEC to do verification by “*ICS generation*”, “*Block checking*” and “*Global Cover*”. If bugs are detected by MEC, the problematic part can also be extracted and saved in a DOT format file by MEC’s “*Debug information*” for easier debugging. Finally, we can obtain the netlist by deriving the final mapping network. Therefore, MEC tool can support the equivalence checking at fine-grained level during technology mapping and is more efficient.

## VI. EXPERIMENT

### A. Setup

We implement MEC tool in C++ based on the data structure of lsils [13], and we used minisat [14] as the SAT solver. All procedures run on an Intel(R) Xeon(R) Platinum 8260 CPU with 2.40GHz, 24 cores and 128GB RAM. We perform experiments on EPFL benchmark [15]. This benchmark contains 10 arithmetic circuits and 10 control/random circuits with circuit sizes ranging from 0.1k to 210k.

### B. Results

For convenience, *MEC* refers to our proposed algorithm; *MTR* refers to purely perform verification on the miter of the mapping network and its original network, then checking by SAT solver without any tricks; *FML* refers to

TABLE I. Runtime comparison between MEC, MTR, FML and CEC tools.

Type	Name	Size	Level	Coarse-grained Time (sec)		Fine-grained Time (sec)		Speedup
				FML	MTR	MEC	CEC	
arithmetic	adder	1277	255	3.5	0.16	<b>0.02</b>	0.77	38.92
	bar	3472	12	13.13	6.73	<b>0.05</b>	1.55	30.97
	div	57376	4372	109,128	timeout	<b>49.2</b>	417.74	8.49
	log2	32093	32060	37,859.1	timeout	<b>45.91</b>	105.9	2.31
	max	3378	287	29.74	0.51	<b>0.27</b>	1.67	6.08
	multiplier	27191	274	546.44	timeout	<b>3.32</b>	30.4	9.14
	sin	5441	225	167.17	timeout	<b>0.7</b>	11.39	16.33
	sqr	24747	5058	timeout	timeout	<b>25.7</b>	153.37	5.97
	square	18549	250	180.33	timeout	<b>0.58</b>	51.61	88.09
	hyp	214592	24801	timeout	timeout	<b>473.53</b>	11331.81	23.93
random	priority	1107	250	3.93	0.099	<b>0.013</b>	0.13	9.71
	cavlc	704	16	3.69	0.022	<b>0.0057</b>	0.08	14.04
	arbiter	12096	87	30.36	12.48	<b>0.157</b>	4.95	31.51
	i2c	1490	20	4.33	0.053	<b>0.0115</b>	0.22	19.00
	ctrl	182	10	1.67	0.0014	<b>0.0013</b>	0.01	7.86
	dec	313	3	1.52	0.0066	<b>0.0024</b>	0.04	16.37
	int2float	272	16	2.19	0.0039	<b>0.002</b>	0.02	10.10
	mem_ctrl	48041	114	451.79	12,487.1	<b>4.52</b>	43.09	9.53
	router	318	54	1.8	0.003	<b>0.0025</b>	0.01	4.02
	voter	14760	70	45.12	200.13	<b>0.46</b>	15.61	33.58
Average	-	-	-	-	-	<b>30.2</b>	608	20.13

directly perform verification on these two networks by the Synopsys Formality Q-2019.12-SP1; CEC refers to perform verification on these two networks by the cec command of abc, and we transform the gate-level netlist into aig file and the original as its inputs. We set 100 hours as the timeout for this comparison.

As shown in Table I, it depicts that the coarse-grained methods FML and MTR's performance are poor, there are even some timeout cases of arithmetic circuits. However, it also shows that the fine-grained methods MEC and CEC can also solve all the circuits within timeout constraints. MEC achieves the best average time result and can solve most cases within 1 second; CEC also performs good due to its exploration of the potential function-equivalent node-pairs to reduce the solver space.

We also compare the speed-up between MEC and CEC. MEC can be up to 88x faster than CEC and the average speed-up is 20x. These results show that MEC is very efficient for verification on technology mapping, which would greatly improve the efficiency of verification.

## VII. CONCLUSION

In this paper, we proposed an efficient algorithm for verification on technology mapping, and we release an open-source FPGA mapping verification tool, MEC. The experimental results show that MEC can solve all the cases and get most results within seconds, outperforming the miter-based method and even the commercial formality tool. In the future, our focus will be directed towards the following areas: (1) Accelerating MEC through parallelization. Our verification algorithm for technology mapping is based on local logic blocks, which has a lot of room for parallelization; (2) Our proposed algorithm has the potential for performing verification between the network in technology mapping and place-and-route (PnR) steps, as long as the behavior of the registers remains unchanged.

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