

Yet Another White Rabbit running on a low-cost, generic FPGA board

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project archive at https://github.com/oscimp/wr_acorn



June 17, 2025

Context and outline

- ▶ White Rabbit (WR) supported boards require two dedicated oscillators for generating the digital phase detector (DMTD)
- ▶ WR as feature of generic boards (RF signal acquisition and synthesis, **Software Defined Radio – SDR**) requires getting rid of this requirement
- ▶ ⇒ **timing library compatible with any existing FPGA based acquisition/synthesis board** (at the expense of performance)
- ▶ Use of clocking circuits internal to the FPGA for generating WR clocks ^a
- ▶ Demonstration on Enjoy Digital's Acorn CLE215+ board...
- ▶ ... Xilinx Artix-7 A100T FPGA / 1 Gb DDR ⇒ start from Nikhef's CLBv3 design and Missing Link Electronics' 2024 contribution¹²

^aSee “More challenging than I can imagine” on slide 8 of D. Charlet & al, *Performance evaluation of a versatile and low-jitter White Rabbit board* at 13th White Rabbit Workshop, CERN (Mar. 2024)

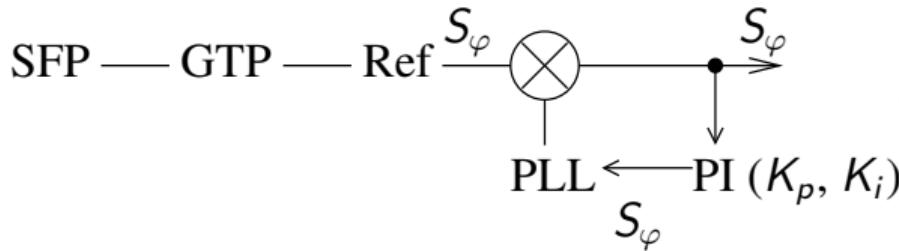


²<https://enjoy-digital-shop.myshopify.com/products/litex-acorn-baseboard-mini-sqrl-acorn-cle215>

¹²13th White Rabbit Workshop (CERN), <https://www.missinglinkelectronics.com/wp-content/uploads/2024/03/MLE-Light-Rabbit-Presentation-at-13th-White-Rabbit-Workshop.pdf>

VCO-less DMTD implementation and phase detection characterization

What element of the control loop is limiting overall performance?



All control loop steps characterized in the frequency domain (phase noise at $f_{Fourier}$ offset from carrier) and time domain (Allan deviation)

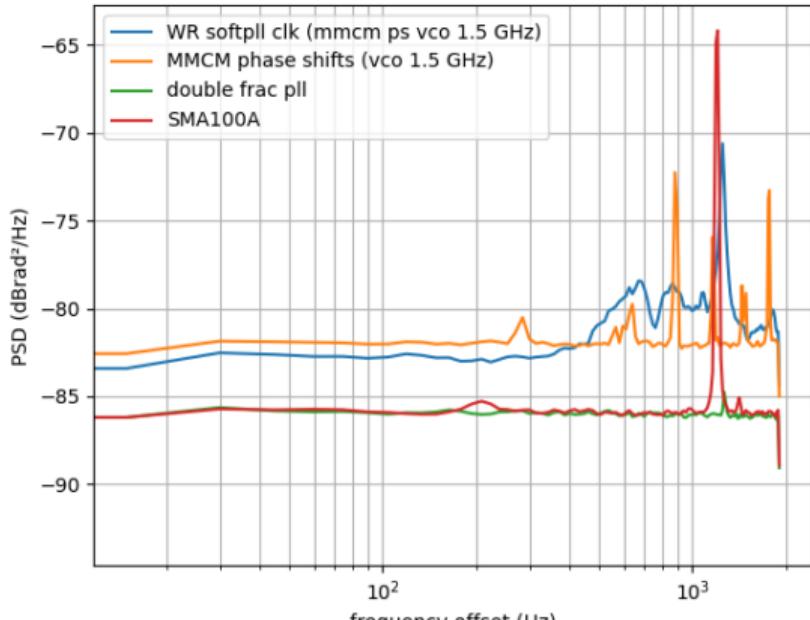
- ▶ Initial tests of CMOD-A7 Artix-7 generic board
- ▶ PLL frequency $f_{PLL} = 62.5$ MHz and beatnote $f_b = 3$ kHz \Rightarrow counter c converted to phase as

$$\varphi = 2\pi c \cdot f_b / f_{PLL}$$

- ▶ phase to phase noise density

$$S_\varphi = \sigma_\varphi^2 / f_b @ f_b$$

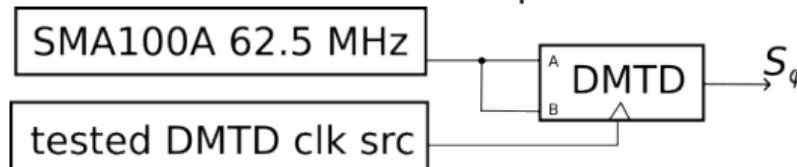
- ▶ phase spectral density using pwelch \rightarrow



VCO-less DMTD implementation and phase detection characterization

What element of the control loop is limiting overall performance?

DDMTD characterization setup



All control loop steps characterized in the frequency domain (phase noise at $f_{Fourier}$ offset from carrier) and time domain (Allan deviation)

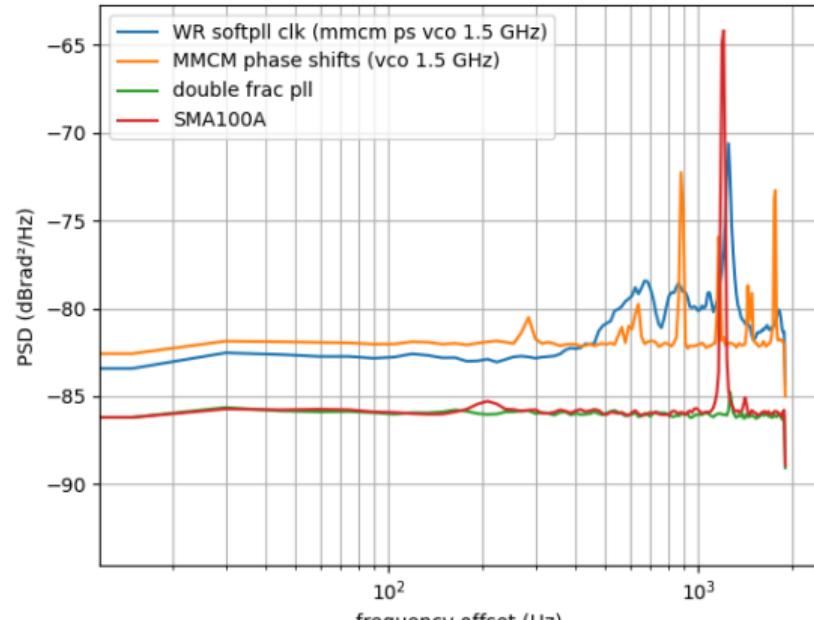
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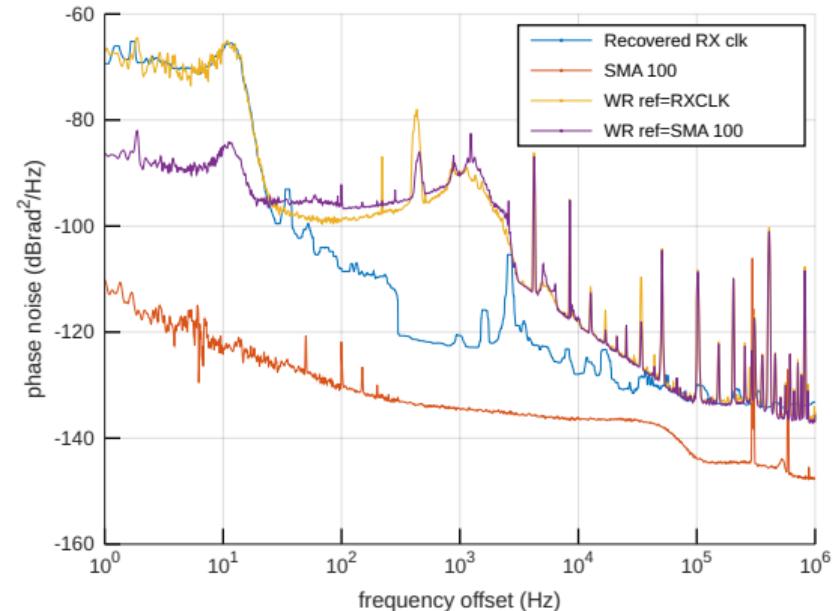
- ▶ phase to phase noise density

$$S_\varphi = \sigma_\varphi^2 / f_b @ f_b$$

- ▶ phase spectral density using pwelch →



Reference clock characteristics



- ▶ 1 - 20 Hz : limited by RX clk from GTP
- ▶ 20 Hz - 3.8 kHz : limited by DMTD and/or softpll
- ▶ 3.8 kHz – : limited by VCO (MMCM with phase-shifts)

HDL implementation on CLE215+: https://github.com/oscimp/wr_acorn

- ▶ board/acorn/ - FPGA-internal HDL
 - ▶ Manifest.py - hdlmake imports
 - ▶ wr_acorn_pkg.vhd - hdl header
 - ▶ xwrc_board_acorn.vhd - logic around xwrc_platform_xilinx and xwrc_board_common
 - ▶ xwrc_board_common expose dac interfaces outputs and clock inputs
 - ▶ traditional WR convert data+load to I²C/other dac protocol
 - ▶ VCO-less WR convert data+load to MMCM's phase-shift control
- ▶ top/acorn_ref_design/ - FPGA/board interface files
acorn_wr_ref_top.xdc - set io pins and allow internal clocking of the GTP ports
- ▶ syn/acorn_ref_design/ - synthesis related files add custom bitstream.tcl to allow internal clocking of the GTP ports
- ▶ platform/Xilinx - add generic to allow internal clocking of the GTP ports

LiteX implementation on CLE215+ & M2SDR:

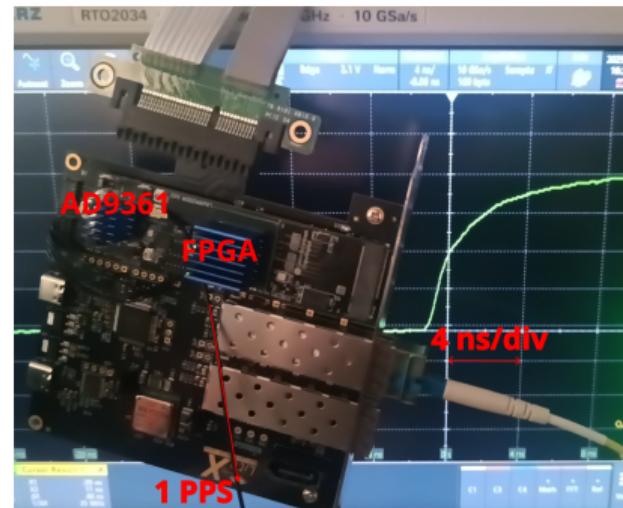
https://github.com/enjoy-digital/litex_wr_nic

```
wrc# pll stat
softpll: mode:3 seq:ready n_ref 1 n_out 1
irqs:123226 alignment_state:0 HL1 ML1 HY=23493 MY=40133 DelCnt=0 setpoint:13037 refcnt:66565 tagcnt:53
softpll: ptracker0: enabled 1 n_avg 512 value 13575
wrc# gui
SPA7 WRPC Monitor wrpc-v5.0-ohwr-9-g5ac04dd5-dirt | Esc/q = exit; r = redraw

TAI Time: 2023-03-03-11:55:43 UTC offset: 37 PLL mode: BC state: Locked
---+-----+-----+-----+
# | MAC | IP (source) | RX | TX | VLAN
---+-----+-----+-----+
0 | 22:33:44:55:66:77 | | 555 | 183 | 0
--- HAL ---|----- PPSI
Itf | Frq | Config | MAC of peer port | PTP/EXT/PDETECT States | Pro
---+-----+-----+-----+
wr0 | Lck | auto | 70:b3:d5:91:ea:f0 | SLAVE /IDLE /EXT_ON | R-W
Pro(tocol): R-RawEth, V-VLAN, U-UDP

----- Synchronization status -----
Servo state: White-Rabbit: TRACK_PHASE

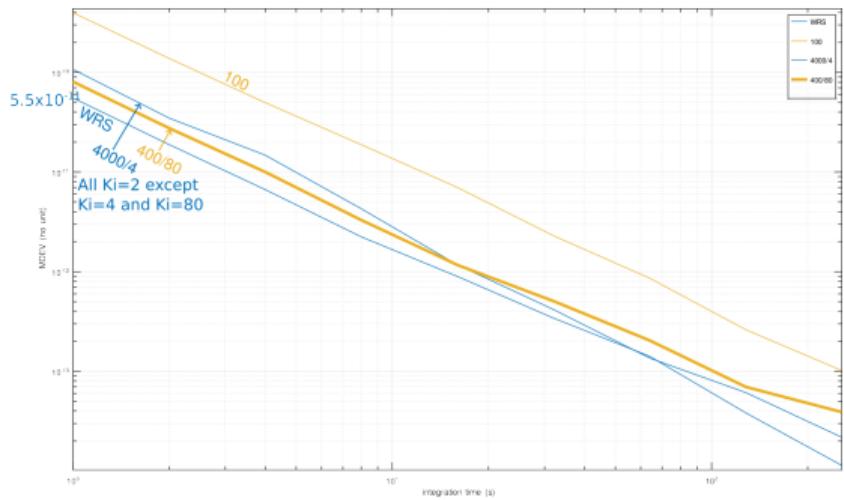
--- Timing parameters ---
meanDelay : 284.572 ns
delayMS : 284.572 ns
delayMM : 1097.210 ns
delayAsymmetry : 0.000 ns
delayCoefficient : +0.0000000000000000 fpa 0
```



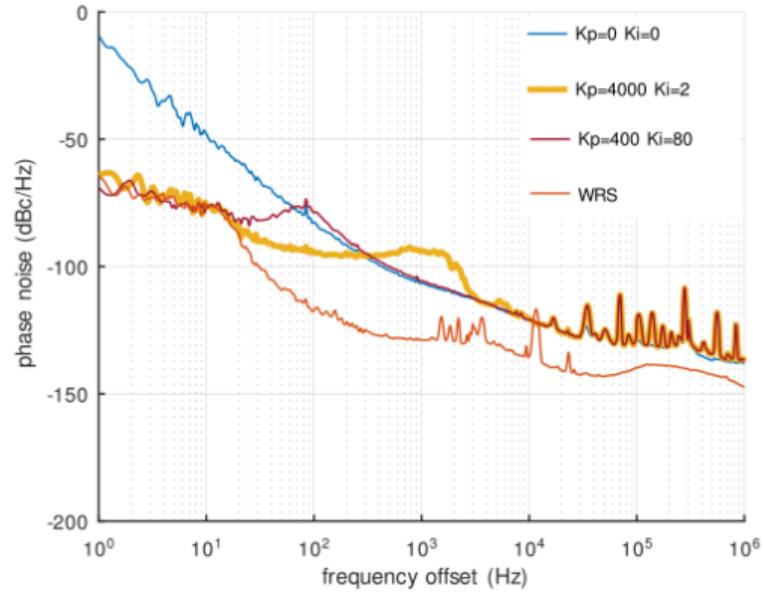
M2SDR running White-Rabbit PTP core with 1 PPS output

Results: Acorn CLE215+

Tuning software phase locked-loop (PLL) control coefficients



Modified Allan deviation: phase flicker noise



Phase noise (Rohde & Schwarz FSWP, all 10 MHz except LiteX 62.5 MHz scaled)

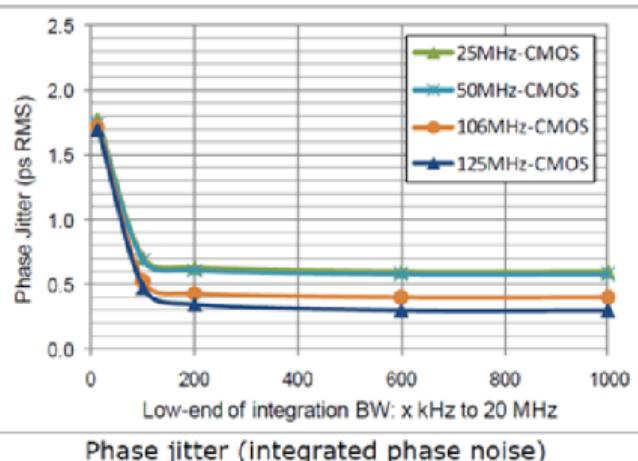
Results: Acorn CLE215+

Tuning software phase locked-loop (PLL) control coefficients
ASDMPL series

Plastic SMD MEMS Clock Oscillator

Nominal Performance Parameters (Unless specified)

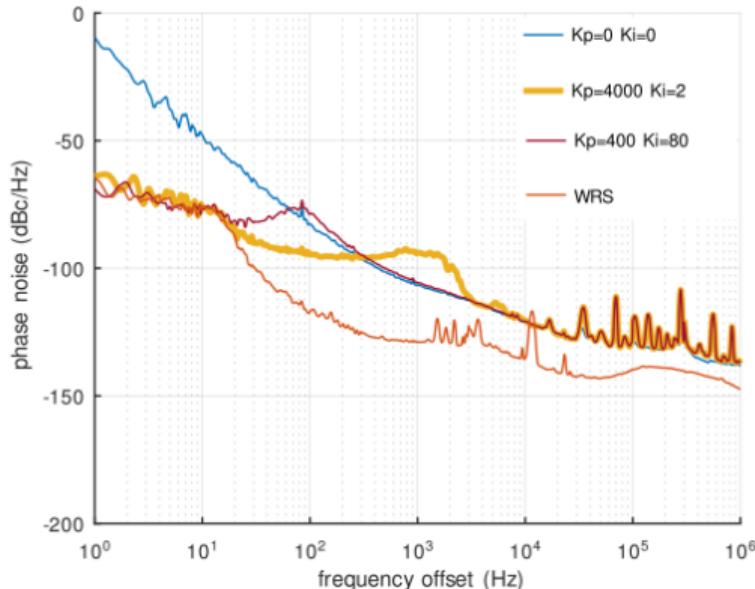
CMOS OUTPUT



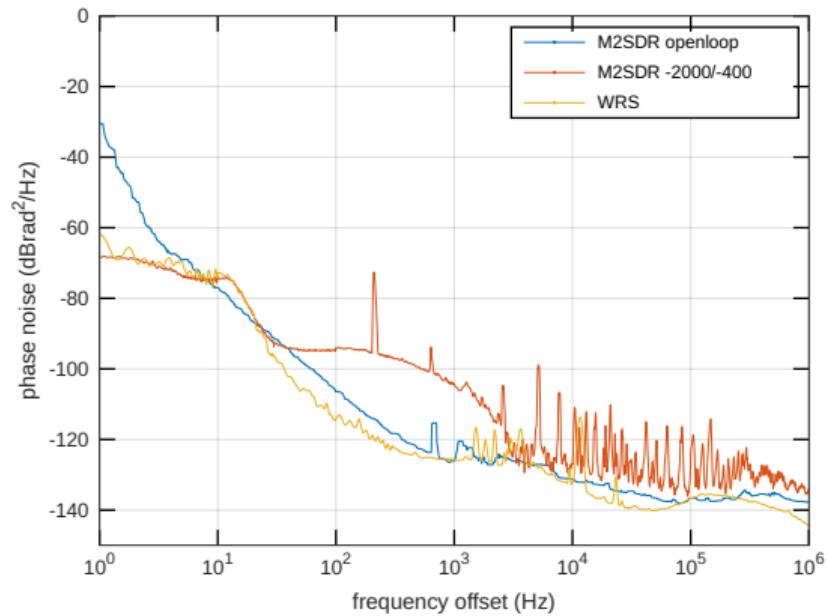
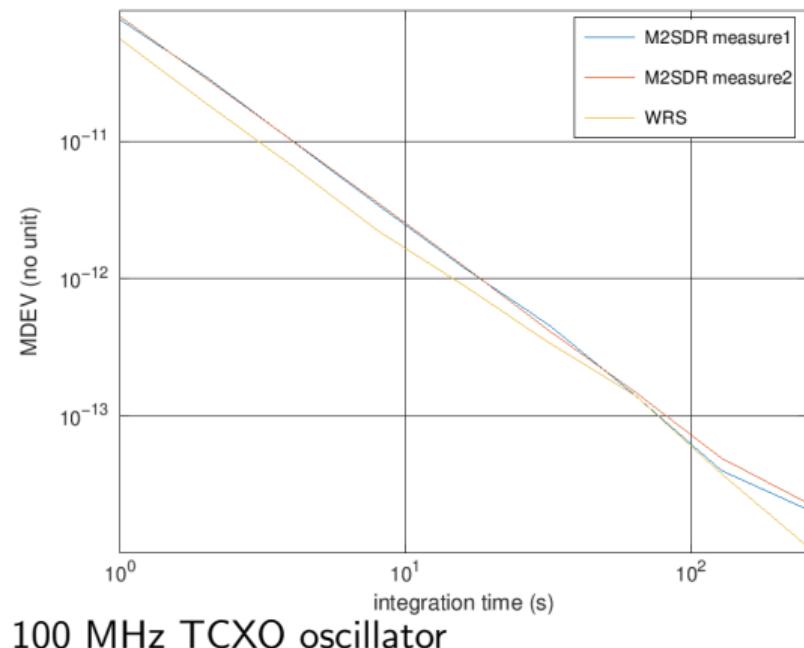
Low quality 200 MHz MEMS oscillator
ASDMPLV-200.000MHZ)

(Abracon

Phase noise (Rohde & Schwarz FSWP, all 10 MHz
except LiteX 62.5 MHz scaled)



Results: M2SDR

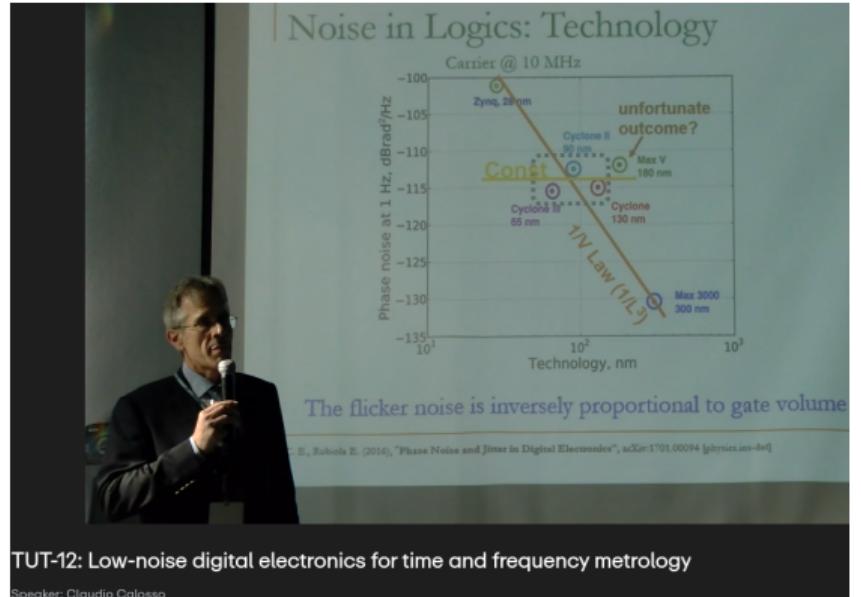


Conclusion & perspectives

- ▶ Initial steps for becoming familiar at FEMTO-ST with WR architecture and internals on Artix7
 - ▶ Functional demonstration, repository at
https://github.com/oscimp/wr_acorn
 - ▶ Impact of internal oscillator usage on phase noise and Allan deviation performance
 - ▶ In progress: port to M2SDR with its AD9361 frontend

Acknowledgements:

- ▶ Peter Jansweijer (Nikhef) for updating the CLBv3 design,
 - ▶ Frederik Pfautsch (Missing Link Electronics) for committing the various VCO-less implementations,
 - ▶ Florent Kermarrec and Gwenhael Goavec-Merou (Enjoy Digital) for providing the hardware boards and LiteX implementations
 - ▶ CERN's White Rabbit team (Tomasz Wlostowski, Tristan Gingold & others)
 - ▶ Claudio Calosso (INRIM) for fruitful discussions ↗



TUT-12: Low-noise digital electronics for time and frequency metrology

Speaker: Claudio Galazzo

Impact of FPGA gate size and phase noise performance during the 2025 IFCS Tutorial on low noise digital electronics ^a

^aC.E. Calosso & E. Rubiola *Phase noise and jitter in digital electronics*, Proc EFTF (2014) 374–376 at <https://arxiv.org/pdf/1701.00094>