

## A riscv isa simulator in Rust.

[github.com/shady831213](https://github.com/shady831213)

# Terminus

<https://riscv.org/exchange/software>

RARS	<a href="#">github</a>	MIT	Benjamin Landers
Renode	<a href="#">website</a> , <a href="#">github</a>	MIT	<a href="#">Antmicro</a>
Ripes	<a href="#">github</a>	MIT	Morten Borup Petersen
RISC-V Virtual Prototype	<a href="#">website</a> , <a href="#">github</a>	MIT	Vladimir Herdt (University of Bremen, <a href="#">AGRA</a> )
TinyEMU	<a href="#">website</a>	MIT	Fabrice Bellard
Spike	<a href="#">github</a>	BSD 3-clause	Andrew Waterman & Yunsup Lee (SiFive)
Swerv-ISS	<a href="#">github</a>	GPL – 3	Joseph Rahmeh (Western Digital)
VLAB	<a href="#">VLAB Works</a>	Proprietary	<a href="#">ASTC</a>
WebRISC-V	<a href="#">github</a>	BSD 3-clause	Gianfranco Mariotti, Roberto Giorgi (University of Siena)
PQSE	<a href="#">website</a>	Proprietary	<a href="#">PQShield</a>
riscv-rust	<a href="#">website</a> <a href="#">github</a>	MIT	Takahiro Aoyagi
terminus	<a href="#">github</a>	MIT	<a href="#">Yang Li</a>
Vulcan	<a href="#">github</a>	MIT	Victor Miguel de Morais Costa
riscv-vm	<a href="#">github</a>	MIT	Aidan Dodds

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# Terminus

► <https://github.com/shady831213/terminus>

- ☒ RV32/64I
- ☒ MADFC
- ☒ M/S/U privilege
- ☒ Pass all riscv\_tests
- ☒ CLINT and Timer
- ☒ HTIF console
- ☒ FDT generation
- ☒ Multi Cores
- ☒ Boot Linux
- ☒ Emu mode binary
- ☒ Boot Linux(smp)
- ☐ Publish to crate.io
- ☒ PLIC
- ☒ VirtIO console
- ☒ VirtIO disk
- ☒ VirtIO network
- ☒ framebuffer
- ☒ VirtIO keyboard
- ☒ VirtIO mouse
- ☐ debug mode
- ☐ other extensions(b, v ...)

# Why Terminus?

- ▶ Just for fun, 疫情期间找点事情
- ▶ 学一手Rust, 写个不是太简单的东西
- ▶ 更深理解RISCV的体系结构, 动手做一遍
- ▶ <https://bellard.org/tinyemu>

# Why Rust?

- ▶ 体验一门新的语言
- ▶ 快
- ▶ 方便的构建工具，容易使用的单元测试框架
- ▶ 轮子
- ▶ 泛型，宏，模式匹配，闭包。。。。

# How?

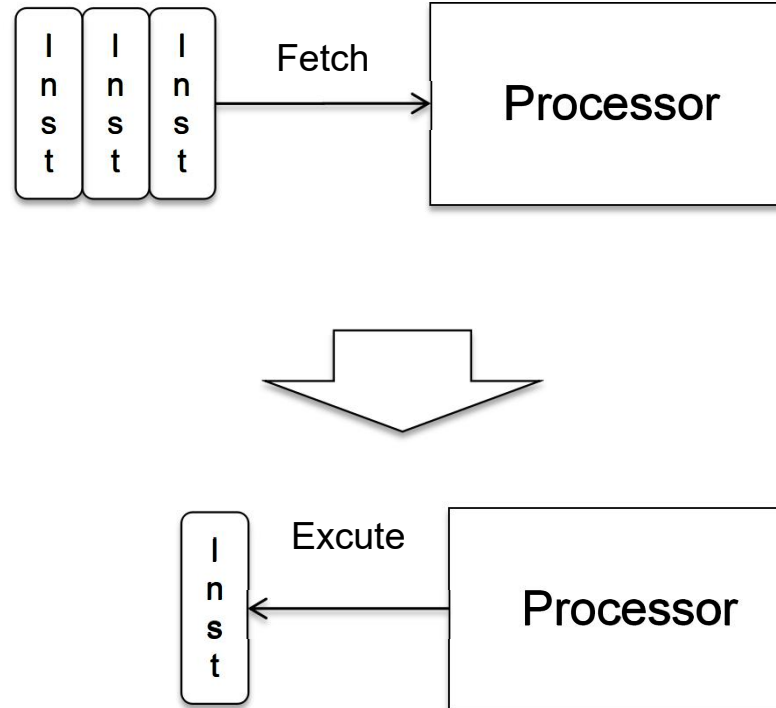
## ► Processor 是什么?

### ► 状态

- 寄存器
- csr
- pc
- icache, dcache, tlb..
- ...

### ► 改变状态的操作

- 指令
- 中断
- ...



# How?

```
pub struct Processor {  
    xreg: [u64; 32],  
    pc: RegT,  
}
```

```
pub struct Instruction(Box<dyn InstructionImp>);
```

```
pub trait Execution {  
    fn execute(&self, p: &mut Processor) -> Result<(), Exception>;  
}
```

# How?

- ▶ 指令如何描述?
  - ▶ 我希望是:
    - ▶ 指令改变processor 的一系列状态
    - ▶ 每条指令应该是可以独立描述的
    - ▶ 每条指令的属性应该是集中定义的
    - ▶ 要方便添加新的指令
    - ▶ 指令应该是无状态的
    - ▶ 相似的指令应该是可以被抽象的



# How?

## ► 指令如何描述?

```
trait Jump: InstructionImp {  
  fn jump<F: Fn(&ProcessorState, Wrapping<RegT>) -> Wrapping<RegT>>(&self, p: &mut Processor, target: F) -> Result<(), Exception> {  
    let offset: Wrapping<RegT> = Wrapping(sext( value: ((self.imm(p.state().ir()) >> 1) << 1) as RegT, len: self.imm_len()));  
    let t = target(p.state(), offset).0;  
    if let Err(_) = p.state().check_extension( ext: 'c') {  
      if t.trailing_zeros() < 2 {  
        return Err(Exception::FetchMisaligned(t));  
      }  
    } else if t.trailing_zeros() < 1 {  
      return Err(Exception::FetchMisaligned(t));  
    }  
    let pc = t;  
    p.state_mut().set_pc(pc);  
    let rd : u32 = self.rd(p.state().ir());  
    let value = *p.state().pc() + 4;  
    p.state_mut().set_xreg( id: rd, value);  
    Ok()  
  }  
}
```

```
#[derive(Instruction)]  
#[format(I)]  
#[code("0b????????????????0000?????1100111")]  
#[derive(Debug)]  
struct JALR();
```

```
impl Jump for JALR {}
```

```
impl Execution for JALR {  
  fn execute(&self, p: &mut Processor) -> Result<(), Exception> {  
    self.jump(p, target: |state, offset| { offset + Wrapping(*state.xreg(self.rs1(state.ir())) })  
  }  
}
```

```
#[derive(Instruction)]  
#[format(J)]  
#[code("0b????????????????????????????1101111")]  
#[derive(Debug)]  
struct JAL();
```

```
impl Jump for JAL {}
```

```
impl Execution for JAL {  
  fn execute(&self, p: &mut Processor) -> Result<(), Exception> {  
    self.jump(p, target: |state, offset| { offset + Wrapping(*state.pc()) })  
  }  
}
```

# How?

- ▶ 指令如何描述?
  - ▶ 怎么实现?
    - ▶ PROC MACRO
    - ▶ [https://github.com/shady831213/terminus/blob/master/proc\\_macros/src](https://github.com/shady831213/terminus/blob/master/proc_macros/src)

# How?

## ► Decode?

- (编码 -> 某个指令实例) -> 应该是个decode tree
- 有什么特点?
  - 最大深度32
  - 应该是稀疏的
  - 运行时是不变的
  - 是被所有processor共享的
- 所以我希望:
  - decode tree 应该是单例的
  - decode tree 应该可以支持分布式的节点插入
  - decode tree 应该可以路径压缩
  - decode tree 在建立时完成所有可变操作, 而在建立完成后时不变的
- <https://github.com/shady831213/terminus/tree/master/src/processor/decode>

# How?

## ► Decode?

- decode tree 应该可以支持分布式的节点插入?
  - <https://crates.io/crates/linkme>
  - 把slice放到link到特殊的section, 有平台依赖的限制

# How?

- ▶ 测试?

- ▶ <https://github.com/riscv/riscv-tests>
- ▶ [https://github.com/shady831213/terminus/blob/master/top\\_tests/riscv\\_tests.rs](https://github.com/shady831213/terminus/blob/master/top_tests/riscv_tests.rs)

## What's next?(If I have time to do :))

- ▶ Support Debug
  - ▶ Support More Extension, b, v...
  - ▶ Try run other OS...
- 
- ▶ Other arch...
  - ▶ More device...

谢谢！