Osaze Y. Shears

Computer Hardware Engineer
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Objective

To serve as a computer programming and hardware engineering instructor and provide students with the critical skills need to make an impact in the computer science and engineering industries.

Education

Virginia Polytechnic Institute and State University, Blacksburg, Virginia *GPA: 4.0*
M.S. Student in Computer Engineering *May 2022*
- **Research:** Reservoir Computing Accelerator Design for Low-Power, Mobile Computing
- **Lab:** Multifunctional Integrated Circuits and Systems (MICS)
- **Recognitions:** Bradley Research Fellowship, New Horizon Graduate Scholars

George Mason University, Fairfax, Virginia *GPA: 3.97*
B.S. in Computer Engineering *May 2018*
- **Coursework:** Digital Circuit Design for ASICs/FPGAs • Object-Oriented Programming • Machine Learning
- **Recognitions:** Summa Cum Laude • Chairman's Award • Outstanding Academic Performance Award • Honors College

Work Experience

Virginia Polytechnic Institute and State University *Blacksburg, Virginia*
Graduate Research and Teaching Assistant *August 2020 - Present*
- Performed research tasks under the Multifunctional Integrated Circuits and Systems (MICS) group
- Provided instructional and grading support for *ECE 2514: Computational Engineering*

Colvin Run Networks, Inc. *McLean, Virginia (Remote)*
Hardware Engineering Associate *June 2021 - Present*
- Provided Colvin Run with information about the FPGA and ASIC design and verification process to guide the development of Copia, a microelectronics supply chain security platform
- Developed a Zynq-7000 SoC-based platform to perform hardware accelerated spectrum sensing and demonstrate Copia's use cases

BAE Systems *Manassas, Virginia*
Digital Logic Design Engineer *May 2018 - July 2020*
- Constructed UVM testbenches to perform logic verification tasks for hardware blocks inside of radiation hardened ASICs
- Performed design for test pattern generation and bring-up tasks on the RAD5545 single-board computer
- Mentored a team of interns in programming software to perform memory test and repair tasks

Projects

Virginia Polytechnic Institute and State University *Blacksburg, Virginia*
Hybrid FPGA-ASIC Delayed Feedback Reservoir *January 2021 - May 2021*
- Developed a hybrid delayed feedback reservoir (DFR) accelerator on the Zynq-7000 SoC with an ASIC
- Demonstrated the accelerator on a spectrum sensing task to demonstrate its application in emerging 5G systems

BAE Systems & Virginia Microelectronics Consortium (VMEC) *Manassas, Virginia*
Memory Built-In Self Test Integration *May 2017 - August 2017*
- Partnered with BAE Systems and VMEC to research Memory Built-In Self Test (MBIST) integration on ASICs
- Developed VHDL and Verilog template files to automate the integration of MBIST into a BAE System's ASIC designs
- Created thorough documentation to detail the MBIST generation and integration process

Technical Skills

Languages SystemVerilog/Verilog • Universal Verification Methodology (UVM) • VHDL • Python • C/C++ • Java • MATLAB
Software Xilinx Vivado • Mentor Graphics ModelSim • Cadence Xcelium • TSSI WaveMaker+ • Xcode • PSpice