Osaze Y. Shears

Computer Hardware Engineer
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Objective

To design and employ embedded systems, application-specific integrated circuits (ASICs), field-programmable gate arrays (FPGAs) and microprocessor technology for advancing the fields of high performance computing, machine learning and artificial intelligence.

Education

Virginia Polytechnic Institute and State University, Blacksburg, Virginia *GPA: TBD*
Ph.D. Student in Computer Engineering *May 2025*

- **Research:** Spiking Neural Networks for Machine Learning on Edge Devices
- **Recognitions:** Bradley Research Fellowship

George Mason University, Fairfax, Virginia *GPA: 3.97*
B.S. in Computer Engineering *May 2018*

- **Coursework:** Digital Circuit Design for ASICs/FPGAs • Operating Systems • Microprocessors • Object-Oriented Programming • Machine Learning
- **Recognitions:** Summa Cum Laude • Chairman's Award • Outstanding Academic Performance Award • Honors College

Technical Skills

Languages SystemVerilog/Verilog • Universal Verification Methodology (UVM) • VHDL • Python • C/C++ • Java • MATLAB
Software Mentor Graphics ModelSim/Questa • Cadence Xcelium • Vivado • TSSI WaveMaker+ • Xcode • PSpice

Work Experience

Virginia Polytechnic Institute and State University *Blacksburg, Virginia*
Graduate Teaching Assistant *August 2020 - Present*

- Provided course instructional and grading support for *ECE 2514: Computational Engineering*

BAE Systems *Manassas, Virginia*
Digital Logic Design Engineer *May 2018 - July 2020*

- Constructed UVM testbenches to perform logic verification tasks for hardware blocks inside of radiation hardened ASICs
- Performed design for test pattern generation and bring-up tasks on the RAD5545 single-board computer
- Mentored a team of interns in programming software to perform memory test and repair tasks

Projects

George Mason University *Fairfax, Virginia*
Project L.E.N.S.: A Robotic Eye using Artificial Muscles *Aug. 2017 - May 2018*

- Worked in a team of six students to develop a Raspberry Pi controlled robotic eye system using silver coated nylon thread as artificial muscles
- Researched approaches to dynamic image stabilization and 3D image tracking using C, Python and the OpenCV library
- **Awards:** Outstanding Senior Design Project Award • Volgenau School of Engineering Advisory Board Award

BAE Systems & Virginia Microelectronics Consortium (VMEC) *Manassas, Virginia*
Memory Built-In Self Test Integration *May 2017 - August 2017*

- Partnered with BAE Systems and VMEC to research Memory Built-In Self Test (MBIST) integration on ASICs
- Developed VHDL and Verilog template files to automate the integration of MBIST into a design
- Created thorough documentation to detail the MBIST generation and integration process
- Presented project deliverables to an audience of 30 Electrical & Computer Engineering professionals