ECE 407/507 Digital VLSI Systems Design

Comprehensive Grading Rubric

All student groups are required to submit an IEEE format Project report and a ZIP archive as part of their final project submission. The Project report should follow the two-page double-column format, a sample report has also been provided for students. The ZIP file should include the complete set of build artifacts generated during the project. This includes the final GDSII, DEF, LEF, and Verilog files, all relevant log files, as well as the JSON ".pkg.json" package file generated by SiliconCompiler. Additionally, students should include any constraint or configuration files used during synthesis and layout, as well as a README.txt file explaining the folder structure and instructions to reproduce the design. Failure to include all required files may result in a deduction of points under the 'Results Folder Submission' criteria. The Rubric structure is defined for a total of 100 points, which is described below:

1. Abstract and Introduction (10 pts)

Criteria	Points
Clearly states project goals and outcomes	3
Provides relevant technical context (e.g., SoC, PicoRV32, Sky130)	3
Motivates the significance of the design and tools used	2
Briefly outlines methodology	2

2. System Design and Architecture (15 pts)

Criteria	Points
Accurate and complete block diagram or architecture overview	5
Clear description of the system components (e.g., processor, SRAM)	5
Justification for chosen hardware modules/extensions	5

3. Methodology and Tools (15 pts)

Criteria	Points
RTL-to-GDSII flow steps clearly explained	5
Description of macro integration (e.g., blackbox, placement constraints)	5
Evidence of design verification steps (e.g., Monte Carlo analysis)	5

4. Implementation and Results (25 pts)

Criteria	Points
Functional integration of SRAM into the PicoRV32 core	5
Area, frequency, and performance metrics reported and interpreted	5
Screenshots or figures of layouts, dashboards, or terminal output	5
Discussion of timing, placement, and synthesis results	5
Handling of warnings/errors, and design constraints	5

5. Analysis (10 pts)

Criteria	Points
Interpretation of performance trade-offs and bottlenecks	4

Reasoning behind design decisions (macro size, die size, etc.)	3
Suggestions for improvement or future design considerations	3

6. Report Formatting and Figures (10 pts)

Criteria	Points
Consistency with IEEE project/report format (e.g., title, sections)	3
Clear and well-labeled figures/tables (Figs. 1–6, layout views, etc.)	3
Captions, references to figures in text, and formatting clarity	2
Visual organization, page alignment, and font consistency	2

7. References (5 pts)

Criteria	Points
Proper citation of sources and tools (e.g., GitHub, SiliconCompiler)	3
Use of IEEE or appropriate citation format	2

8. Results Folder Submission (10 pts)

Criteria	Points
Contains GDSII, LEF, and Verilog files, and logs from SiliconCompiler	5
Includes a JSON package or README.txt explaining how to reproduce key results	5