DATASHEET

AXS15231E

In-Cell IC Integrates 540-channel 6-bit Source Driver and GIP Gate Driver and Touch Panel Controller Into a Single Chip with TP Controller Supports Real Multi-Touch Capability

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Version V0.3
2025-12-09

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REVISION HISTORY

Date	Version	Description	Page	Author
2025/08/13	V0.1	Preliminary：Because the product is under function verification and early promotion, this specification is an initial version and subject to change	170	AXS
2025/09/02	V0.2	Modify DIN_SDA to be pulled high by default when not connected	15	AXS
2025/12/09	V0.3	Modify 3AH register description	35	AXS

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GENERAL DESCRIPTION

The AXS15231E highly integrates a-Si TFT LCD driver and Super in-cell Touch controller, is a 262,144-color System-on-Chip (SOC) driver LSI designed for small and medium size TFT LCD display, and is capable of supporting up to 360RGBx640(Dual gate) pixels in resolution. The 540-channel source driver can provide 6-bit resolution and generate 64 Gamma-corrected values with an internal D/A converter.

The AXS15231E is able to operate with a low-voltage IO interface. Incorporating multiple on-chip charge pumps, it can generate various voltage levels required by the gate and source drivers through a built-in power management system. The charge pump circuits are designed to operate without any external capacitors, enabling a capacitor-less configuration for internal voltage generation.

In addition, it supports functions such as PWM control for LED backlight, wake-up button enabling, respiratory light effects, and other features to provide customers with a better user experience.

In addition, the external Flash of AXS15231E can store not only the firmware used for Touch controller, but also the Initial code of LCD driver. After loading the initial code through the external Flash, the HOST only needs to send out "Sleep out" and "Display on" to turn on the LCD.

The built-in timing controller in the AXS15231E can support several functions to meet a wide variety of requirements for portable display applications. It provides several system interfaces, including MIPI/QSPI/DSPI/SPI/sRGB/RGB/MCU, which can be used to configure the system. Furthermore, it can also archive high speed display data transmission by using the MIPI interface.

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1. Features

1.1. Display

1. One-chip solution for color amorphous TFT-LCD with incell
   Display Resolution
   - Dual gate: 360RGB(up to 360,2 columns/step) x 640(up to 960,2 lines/step) in video mode
   - Single gate:180RGB(up to 180,2 columns/step) x 800(up to 1022,2 lines/step) in video mode(2 lines/step)
   - Dual gate: 320RGB(up to 320,2 columns/step) x 480 (up to 480,2 lines/step) or 360RGB(up to 360,2 columns/step)×400(up to 400,2 lines/step) in command mode
   - Single gate:180RGB(up to 180,2 columns/step) x 720(up to 720,2 lines/step) in command mode
2. On chip display RAM
3. Support low frame rate(60Hz/45Hz/30Hz/20Hz/10Hz)
4. Support in-chip OTP
   - OTP can stores VCOM setting
   - OTP can stores ID 1/2/3 setting
   - OTP can stores analog gamma setting
5. VCOM: -2.5V~0V (10mv/step)
6. Color depth : 565、666
7. Support 8-color and 2-color mode
8. Interface
   - MIPI:1 lane MIPI DSI:MIPI DSI2 V1.0 / V1.1 / V1.2, DCS：1.01.00 compatible，max speed 500Mbps
   - SPI/DSPI
   - QSPI
   - MCU: Parallel 8080-series MCU Interface (8-bit, 9-bit, 16-bit, and 18-bit)
   - RGB:16bit/18bit RGB interface
   - Serial RGB (888, 666, 565)
9. 1-dot/2-dot/4-dot/Column Inversion
10. Support 0 Flash
11. Support IGZO
12. Maximum VOP voltage：5.5V
13. 90 degree rotation function: Column resolution input and output do not exceed 360 columns

1.2. Touch

14. Embedded MCU
15. Support two-point detection
16. Point reporting rate 60Hz
17. Support single or double click gesture to wake up
18. Super self-capacitance detection technology
19. I2C/SPI data communication interface

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20. Internal ESD detection
21. 96 SX channels
22. Power saving mode
23. VDDI_TP and VDDI_DRV supplied independently

1.3. Power

24. 2-power mode
    - VCI：2.65V~3.6V，typ：3.3V
    - VDDI：1.65V ~ 3.6V，typ： 1.8V
25. 1-power mode
    - VCI/VDDI：2.65V~3.6V，typ：3.3V

1.4. Others

26. ESD
    - HBM≥2000V
    - MM≥200V
    - Latch up≥±200mA
27. COG Package
28. Operate temperature range: −30℃ to +85℃

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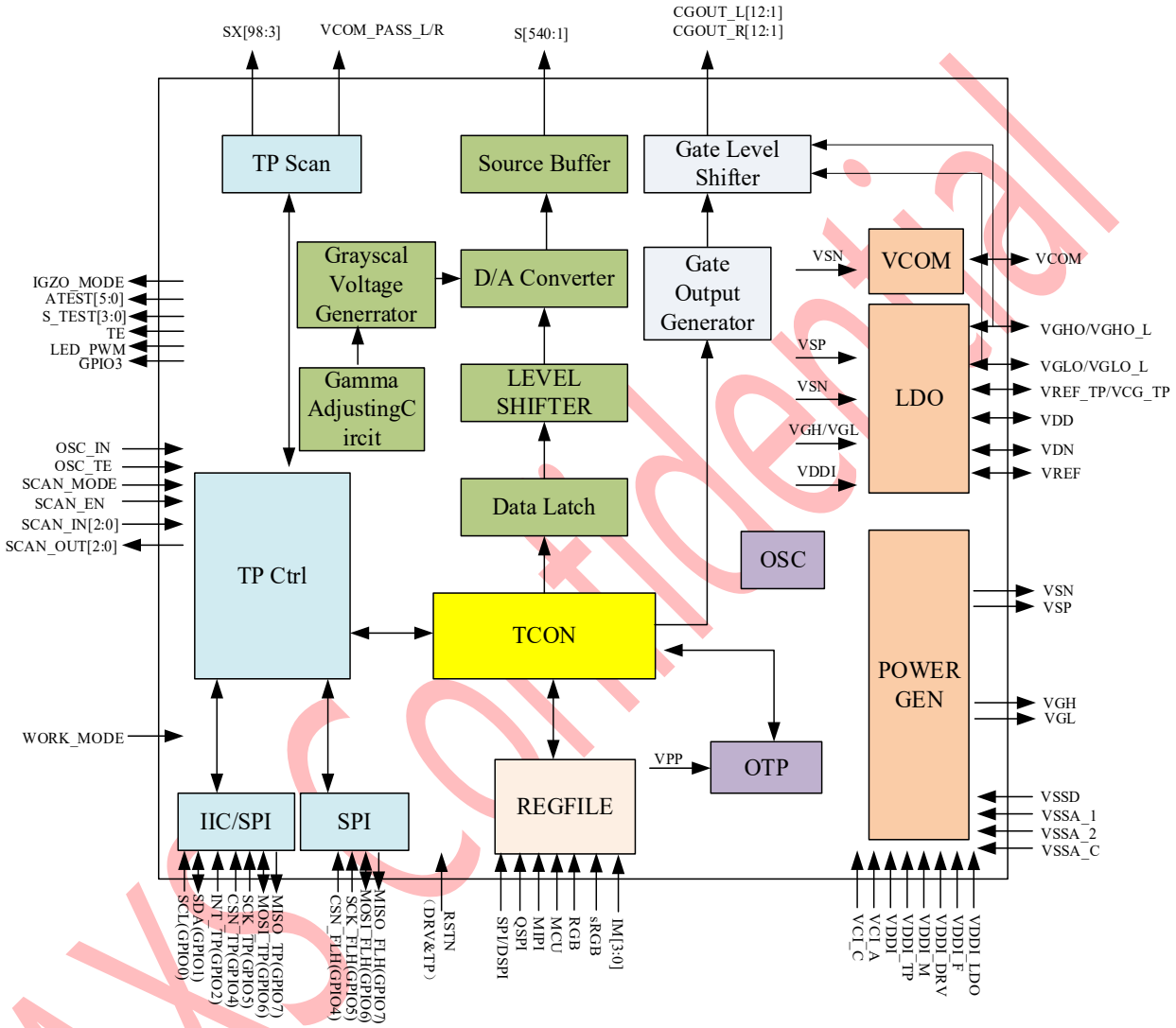
2. Block Diagram

2.1. Block Function



2.1.1. Touch Function

The touch part of AXS15231E mainly consists of the following components:

AFE Controller

AFE controller completes the scanning of the sensors in the touch panel, and sends the data of touch sensors after scanning to the MCU for data processing.

Embedded MCU

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MCU and SOC subsystems complete the control, data processing, LCD operation and coordination, HOST communication and other functions of the whole touch systems.

I2C/SPI serial interface

The Slave end of I2C/SPI in AXS15231E is the interface for touch communication with HOST. The control interface consists of two signals INT (is a GPIO, specified in the firmware) and RSTN (only one rstn-pin, shared by driver and touch). Whenever there is effective touch sensed on the touch screen, Touch controller will send data transfer request to the HOST via INT port, and complete the point report to the HOST. HOST can communicate with AXS15231E via I2C or SPI. HOST can also reset Touch controller through RSTN port.

External Flash

External Flash, used to store the Firmware, and LCD initialization code, can be added into the Touch controller.

Watchdog

Watchdog is used to ensure the stability of the chip when in operation

Internal voltage regulator

Internal voltage regulator generates 1.32V power supply, which is to provide power to logic circuit.

2.1.2. Touch Operation Mode

Touch controller has the following three operation modes:

Normal operating mode

In this mode, Touch controller scans the screen, and detects the touch actions.

Monitor Mode

In this mode, Touch controller scans the screen intermittently to save power.

Sleep mode

In this mode, Touch controller enters ultra low-power standby mode, HOST can only wake-up Touch controller via external signal or SPI/IIC/MIPI/QSPI to enter the normal operating mode. The power consumption in this mode is extremely small, and can greatly extend the standby time of mobile portable devices.

2.1.3. MCU

This section describes some critical features and operations supported by the 8051 compatible MCU.The figure below shows the overall structure of the MCU block. In addition to the 8051 compatible MCU core, we have added the following circuits.

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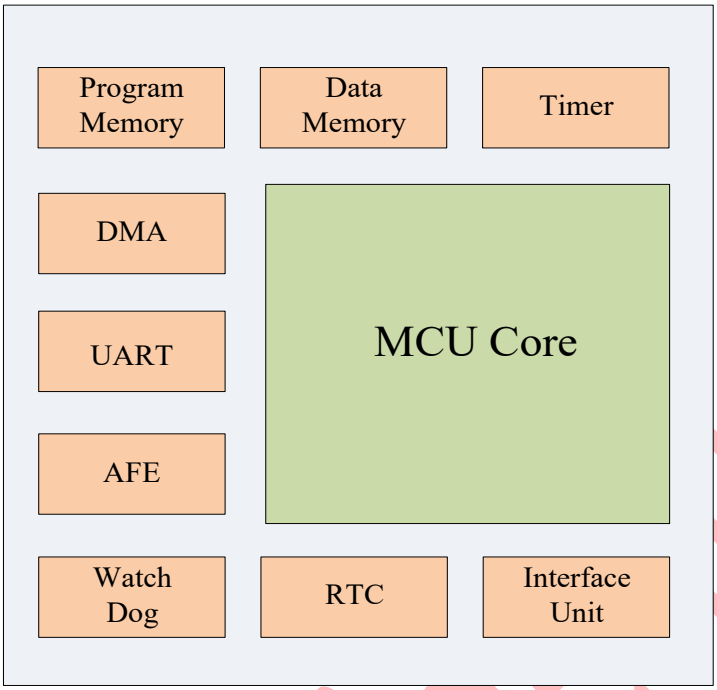
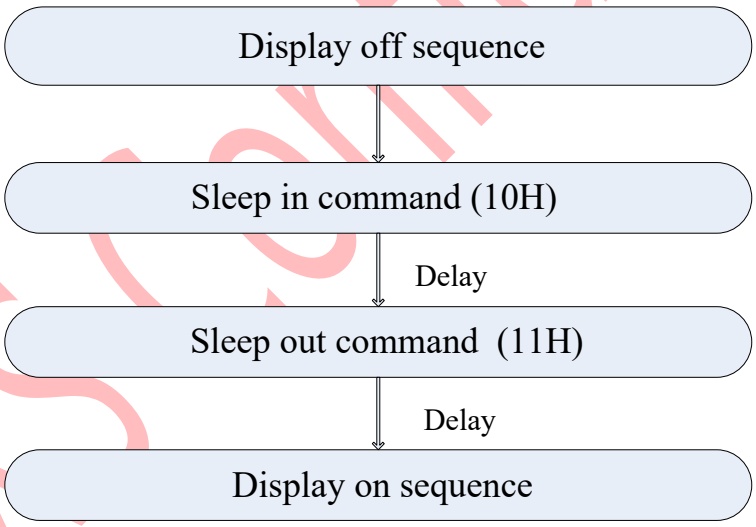


2.1.4. Sleep In/Out Sequence



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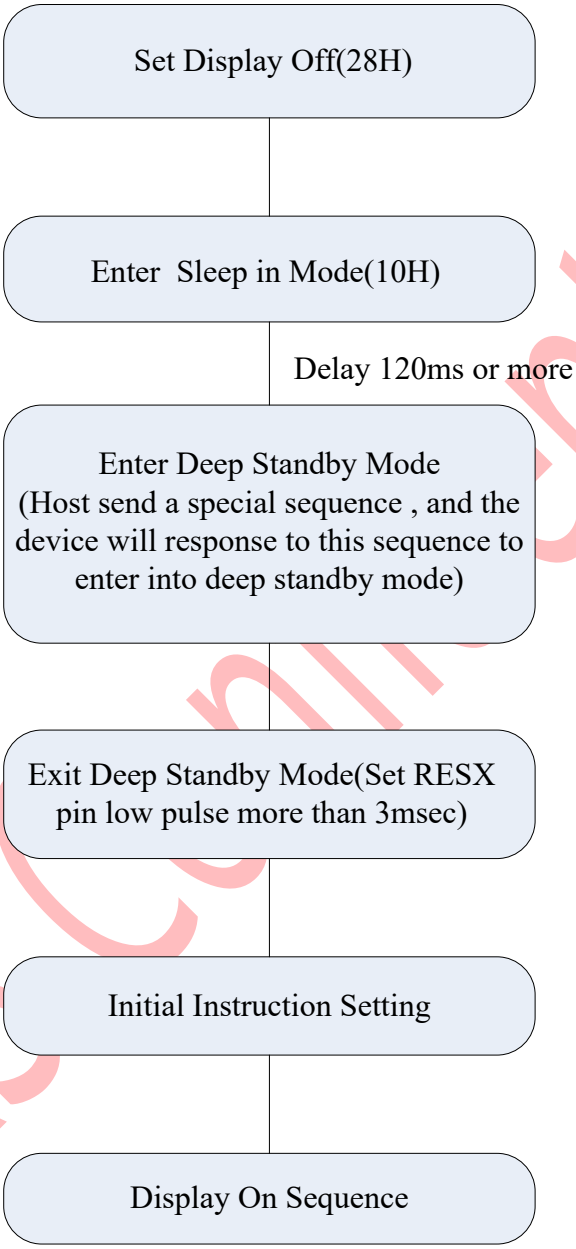
2.1.5. Deep Standby Mode enter/exit Sequence

Deep Standby Mode Sequence



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2.1.6. System interface

The AXS15231E supports the video data transmitted through the high-speed system interface, MIPI (Mobile Industry Processor Interface).

2.1.7. Grayscale voltage generating circuit

AXS15231E has true 6-bit resolution D/A converter, digital gamma cooperates with OP-AMP

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structure to enhance display quality. The grayscale voltage can be adjusted by grayscale data set in the γ-correction register.

2.1.8. Timing controller

AXS15231E has a timing controller, which can generate a timing signal for internal circuit operation such as gate output timing, image data accessing timing, etc.

2.1.9. Oscillator (OSC)

The AXS15231E has an internal oscillator to generate system clock.

2.1.10. Source driver circuit

AXS15231E consists of a 540-output source driver circuit.

2.1.11. Gate driver circuit

AXS15231E consists of a gate driver control circuit. The gate driver circuit outputs gate driver signals level at either VGHO or VGLO level.

2.1.12. LCD driving power supply circuit

The LCD driving power supply circuit generates the voltage levels VDD, VSP, VSN, VGH, VGL, VCOM for driving LCD. All these voltages can be adjusted by register setting.

3. Pin Description

3.1. Power Supply and Regulator pins

Name	I/O	Default value	Description
VCI_A	I	2.65V ~ 3.6V , typ:3.3V	External input voltage
VCI_C	I	2.65V ~ 3.6V , typ:3.3V	External input voltage
VDDI	I	1.65V ~ 3.6V , typ:1.8V	External input voltage
VDDI_TP	I	1.65V ~ 3.6V , typ:1.8V	External input voltage
VDDI_F	I	1.65V ~ 3.6V , typ:1.8V	External input voltage, for GPIO[7-4]
VDDI_LDO	I	1.65V ~ 3.6V , typ:1.8V	External input voltage, for LDO
VDDI_DRV	I	1.65V ~ 3.6V , typ:1.8V	External input voltage

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VDDI_M	I	1.65V ~ 3.6V , typ:1.8V	External input voltage for mipi-ldo
VSP	O	5.0V ~ 6.8V	Charge pump output voltage or External input voltage
VSN	O	-5.4V ~ -4.0V	Charge pump output voltage or External input voltage
VCOM	O	-2.5V ~ 0V , typ: -1V	Regulator output voltage
VDD	O	1.2V ~ 1.48V , typ:1.32V	Internal LDO output for digital power supply
VSSD	I	GND	Digital ground
VSSA_1	I	GND	Analog ground, connect to VSSD on FPC
VSSA_2	I	GND	Analog ground, connect to VSSD on FPC
VSSA_C	I	GND	Analog ground, connect to VSSD on FPC
VPP	I	8.0V ~ 8.5V , typ:8.25V	supply for OTP program
VDN	O	1.2V ~ 1.48V, typ:1.32V	Internal LDO output
VGH	O	10.4V ~ 15.9V	Power supply for VGHO.
VGHO_L	O	10V ~ 15V	connect to VGHO on FPC
VGHO	O	10V ~ 15V	Power supply for GIP positive or TP HIZ.
VGL	O	-14.2V ~ -7.6V	Power supply for VGLO.VGL is also the substrate voltage of the whole chip
VGLO_L	O	-13.5V ~ -7.0V	connect to VGLO on FPC
VGLO	O	-13.5V ~ -7.0V	Power supply for GIP negtive or TP HIZ.
VDDA_TP	O	VCI or VSP	TP power, connect to VCI/VSP on FPC
VREF	O	1.8V	Refrence voltage
VREF_TP	O	Supply by VSP:2.9~6.0V Supply by VCI:1.4~2.8V	Regulator output voltage for TP-AFE
S	O	Supply by VSP:2.9~6.0V Supply by VCI:1.4~2.8V	Regulator output voltage for TP-AFE

3.2. Drive interface logic pin

Name	I/O	Default value	Description
RSTN	I	1,pull up without control	This signal will reset the device and must be applied to properly initialize the chip.Signal is active low.pull up to avoid floating. Caution: TP and Driver share the same RSTN-PIN

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IGZO_MODE	I	0	0: for non-IGZO panel 1: for IGZO panel
LED_PWM	O	0,50pf	Backlight control setting pin.Output load 50pf
TE	O	0,50pf	output tearing effect signal from IC to host
CSX	I	1,pull up without control	**SPI：** Chip select input pin("Low" enable) in SPI slave ,pull up to avoid floating. This pin is not used for MIPI I/F, please connect to VDDI.
SCL	I	1,pull up without control	**SPI：** Synchronous clock signal in SPI slave, pull up to avoid floating. This pin is not used for MIPI I/F, please connect to VDDI.
RS	I	0,pull down without control	**SPI 4wire 8bits：** command or parameter selection in spi 4wire 8bits.
DIN_SDA	I	1,pull up without control	**SPI & QSPI**:This pin is not used for MIPI I/F, please connect to VDDI. 1.In QSPI mode:When cr_qspi_diomode=0, it used as QSPI_DIN0;When cr_qspi_diomode=1, it used as QSPI_DIN1. 2.In SPI 3wire/4wire When cr_qspi_diomode=0, it used as SPI_SDA;When cr_qspi_diomode=1, it used as MISO.
DIN_SDA_DUAL	I	0,pull down without control	**SPI & QSPI**:The second data input pin in spi dual data lane of spi slave.Default input.pull down to avoid floating.This pin is not used for MIPI I/F,please connect to VSSD. 1.In QSPI mode::When cr_qspi_diomode=0, it used as QSPI_DIN1;When cr_qspi_diomode=1, it used as QSPI_DIN0. 2.In SPI 3wire/4wire When cr_qspi_diomode=1, it used as MOSI.
VSYNC_QSPI_DIN2	I	1,pull up without control	**MCU & RGB & QSPI:** 1.Frame synchronizing signal of rgb interface. Used as csn of 8080 mcu interface for command mode. 2.In QSPI mode, it used as QSPI_DIN2
HSYNC	I	1,pull up without control	**MCU & RGB**:Line synchronizing signal of rgb interface. Used as d/cx of 8080 mcu interface for command mode.
DE_QSPI_DIN3	I	0,pull down without control	**MCU & RGB & QSPI**: 1.Data enable signal of rgb interface. Used as wr of 8080 mcu interface for command mode. 2.In QSPI mode, it used as QSPI_DIN3.
PCLK	I	0,pull down without control	**MCU & RGB**:pixel clock signal of rgb interface. Used as rd of 8080 mcu interface for command mode.
DB[17:0]	I	0,pull down without control	**MCU & RGB**:DB[17:0] input data of rgb interface. DB[17:0] of 8080 mcu interface for command mode.
IM[3:0]	I	0,pull down without control	select the input interface 1010:QSPI

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			1001:spi 3 wire 9bits dual data lane from driver spi
			1000:dbi 18bits;
			0111:dbi 16bits;
			0110:dbi 9bits;
			0101:dbi 8bits;
			0100:spi 4Wire 8bits dual data lane;
			0011:spi 3wire 9bits+rgb
			0010:spi 4wire 8bits+rgb
			0000:mipi
			1011:3wire spi+sRGB
			1100:4wire spi+sRGB

IM3	IM2	IM1	IM0	Interface	Connect Pin
0	0	0	0	MIPI	HS_DN,HS_DP,HS_CN,HS_CP,RSTN
0	0	1	0	SPI 4wire/8bits RGB	DIN_SDA(MISO),DIN_SDA_DUAL(MOSI),RS(D/CX),SCL,CSX,RSTN
0	0	1	1	SPI 3wire 9bits+rgb 16/18-bit	Video Stream Interface:DB[15/17:0],VSYNC_QSPI_DIN2,HSYNC, DE_QSPI_DIN3,PCLK
					Control Interface:DIN_SDA(MISO),DIN_SDA_DUAL(MOSI),SCL,CSX,RSTN
1	0	1	1	SPI 3wire +sRGB	Interface:DB[7:0], PCLK,VSYNCHSYNC,DE,CSX,SCL,DIN_SDA
1	1	0	0	SPI 4wire + sRGB	Interface:DB[7:0], PCLK,VSYNCHSYNC,DE,CSX,SCL,DIN_SDA,RS
0	1	0	0	SPI 4wire 8bits dual data lane	DIN_SDA,DIN_SDA_DUAL,RS(D/CX),SCL,CSX,RSTN
0	1	0	1	MCU 8080 8bits	DB[7:0],VSYNC_QSPI_DIN2(CSX),HSYNC(D/CX), DE_QSPI_DIN3(WRX),PCLK(RDX),RSTN
0	1	1	0	MCU 8080 9bits	DB[8:0],VSYNC_QSPI_DIN2(CSX),HSYNC(D/CX), DE_QSPI_DIN3(WRX),PCLK(RDX),RSTN
0	1	1	1	MCU 8080 16bits	DB[15:0],VSYNC_QSPI_DIN2(CSX),HSYNC(D/CX), DE_QSPI_DIN4(WRX),PCLK(RDX),RSTN
1	0	0	0	MCU 8080 18bits	DB[17:0],VSYNC_QSPI_DIN2(CSX),HSYNC(D/CX), DE_QSPI_DIN5(WRX),PCLK(RDX),RSTN
1	0	0	1	SPI 3wire 9 bits dual lane from drv SPI	DIN_SDA,DIN_SDA_DUAL,SCL,CSX,RSTN
1	0	1	0	QSPI	DE_QSPI_DIN3,VSYNC_QSPI_DIN2,DIN_SDA,DIN_SDA_DUAL,SCL,CSX,RSTN

Display Interface Note：

1. SPI:MISO to DIN_SDA,MOSI to DIN_SDA_DUAL,DCX to RS,SCK to SCL,CSN to CSX (cr_qspi_diomode=1 default)

2. QSPI:D0 to DIN_SDA_DUAL,D1 to DIN_SDA,D2 to VSYNC_QSPI_DIN2,D3 to DE_QSPI_DIN3,SCK to SCL,CSN to CSX (cr_qspi_diomode=1 default)

3. MCU:DB[17:0],CSN to VSYNC_QSPI_DIN2,DCX to HSYNC,WRX to DE_QSPI_DIN3,RDX to PCLK

4. RGB:DB[17:0],VSYNC to VSYNC_QSPI_DIN2,HSYNC to HSYNC,DE to DE_QSPI_DIN3,PCLK to PCLK

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3.3. Touch Related Pin

Name	I/O	Default value	Description
RSTN	I	weak pull up without control	This signal will reset the device and must be applied to properly initialize the chip.Signal is active low.pull up to avoid floating. Caution: TP and Drive share the same RSTN-PIN.
WORK_MODE	I	weak pull down without control	Selection of work mode,high represent 0 flash mode;low represent extern flash. need weak pull down to avoid floating.
	0	I2C	GPIO[0] : SCL GPIO[1] : SDA GPIO[4] : FLASH_CS GPIO[5] : FLASH_SCK GPIO[6] : FLASH_MOSI GPIO[7] : FLASH_MISO
	1	SPI	GPIO[4] : CS_SLAVE GPIO[5] : SCK_SLAVE GPIO[6] : MOSI_SLAVE GPIO[7] : MISO_SLAVE
GPIO[7:0]	I/O	open drain,IC internal pull up,4.7K;	work for I2C interface clock or data as I2C master,when WORK_MODE=0;GPIO[1:0] only used for I2C slave interface; GPIO[7:4] can used for spi master interface of flash or other function.
		50pf	work for spi interface or test output, when WORK_MODE=1,GPIO[7:4] only used for spi slave interface.
		when output,50pf;when input ,weak pull down and pull up with control	when output,50pf;when input ,weak pull down and pull up with control
OSC_TE	I	weak pull down without control	osc select;1:extern osc input.0:internal osc clock
OSC_IN	I	weak pull down without control	extern input osc clock
SCAN_MODE	I	weak pull down without control	selection of scan chain mode,active high.
SCAN_EN	I	weak pull down without control	enable of scan chain
SCAN_IN[2:0]	I	weak pull down without control	input data of scan chain
SCAN_OUT[2:0]	O	50pf	output data of scan chain
SX[98:3]	O	-	TP Sensor Pins

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3.4. MIPI Interface

Name	I/O	Default value	Description
HS_CP	I	MIPI Input	MIPI-DSI clock Lane positive-end input pin
HS_CN	I	MIPI Input	MIPI-DSI clock Lane negative-end input pin
HS_DP	I/O	MIPI Input /Output	MIPI-DSI data Lane 0 positive-end input/output pin
HS_DN	I/O	MIPI Input /Output	MIPI-DSI data Lane 0 negative-end input/output pin

3.5. Test/Dummy Signal/ Other

Name	I/O	Default value	Description
TS_SEL	I	Test signal	test pad
ATEST[5:0]	I/O	Test signal	test pad
BGR_CORE_SEL_PAD	I	Test signal	test pad
POR_MODE_SEL_PAD	I	Test signal	test pad
BGR_CORE_NPN_SEL_PAD	I	Test signal	test pad
S_TEST[3:0]	O	Test signal	test pad
VBG_PAD	O	Test signal	test pad
POCN_VCI_PAD	O	Test signal	test pad
RF_CHECK	I	-	Detect RF interference

3.6. Panel driver Signals

Name	I/O	Default value	Description
CGOUT_L[12:1]	O	GIP Output	Gate control signals for panel in left side of IC
CGOUT_R[12:1]	O	GIP Output	Gate control signals for panel in right side of IC
S[540:1]	O	Source driver Output	Output source driver signals. The D/A converted 64-gray-scale analog voltage output.
			Source output mapping with different resolution.
			360 RGB, (Source output from S1 to S540)

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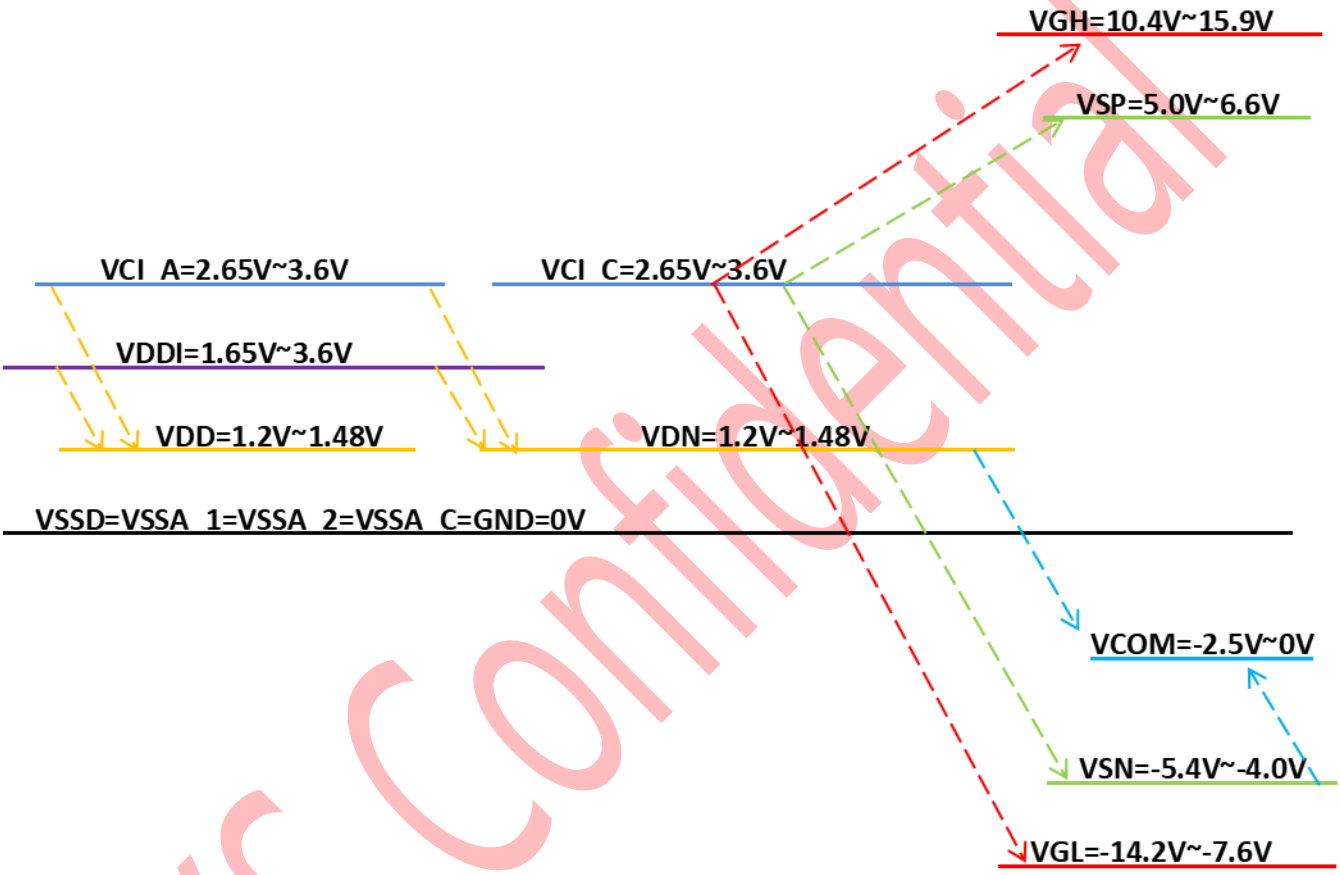
3.7. Power Block Diagram

The following is the power supply generation scheme, AXS15231E consists of VDDI and VCI_A/VCI_C as the input power supply, and other power supply levels are generated in the chip.

3.8. Power Supply Peripheral Circuit



Note: VDDI includes VDDI, VDDI_TP, VDDI_F, VDDI_LDO, VDDI_DRV, and VDDI_M.

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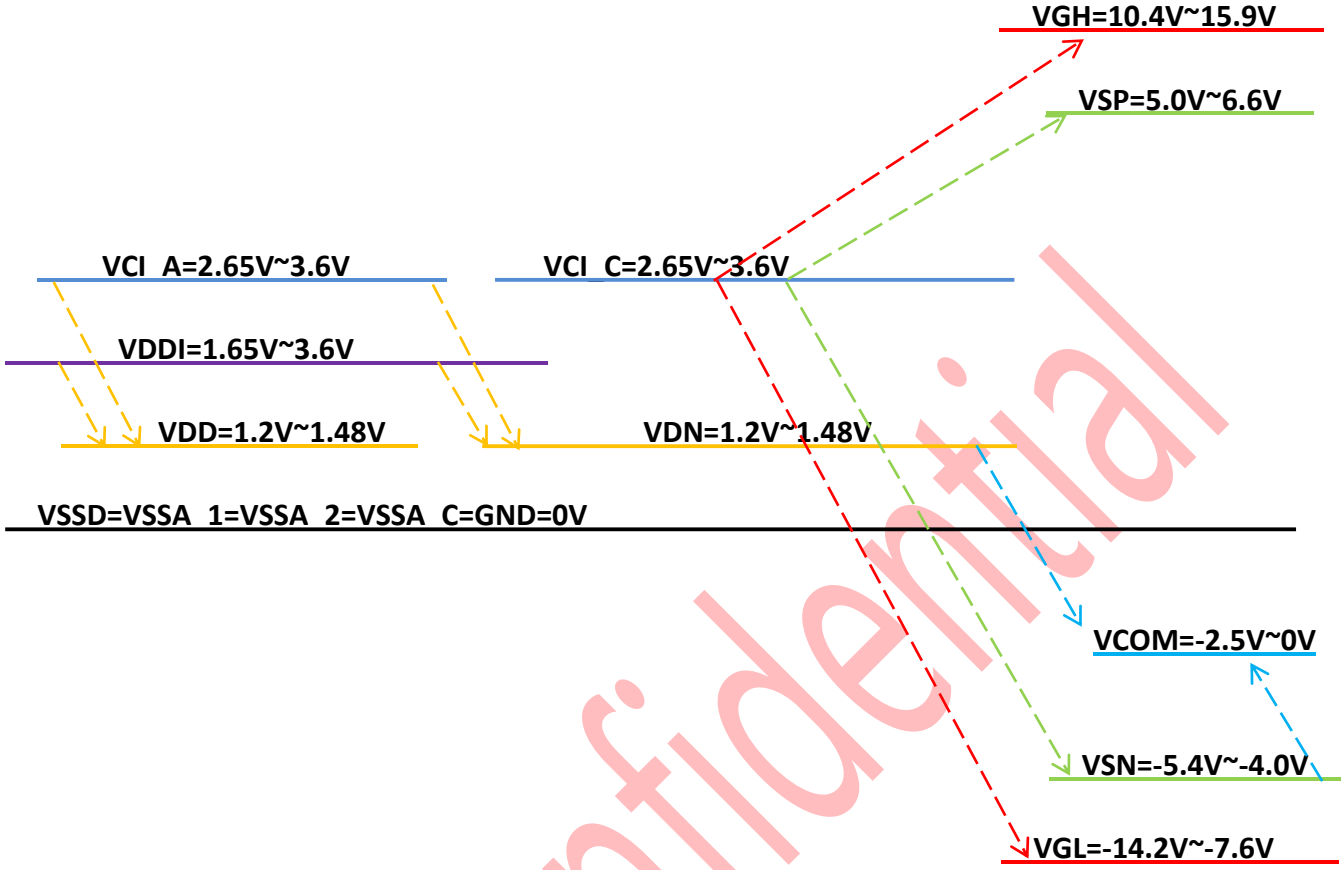

VDDI 包括：VDDI　VDDI_TP　VDDI_F　VDDI_LDO　VDDI_DRV　VDDI_M

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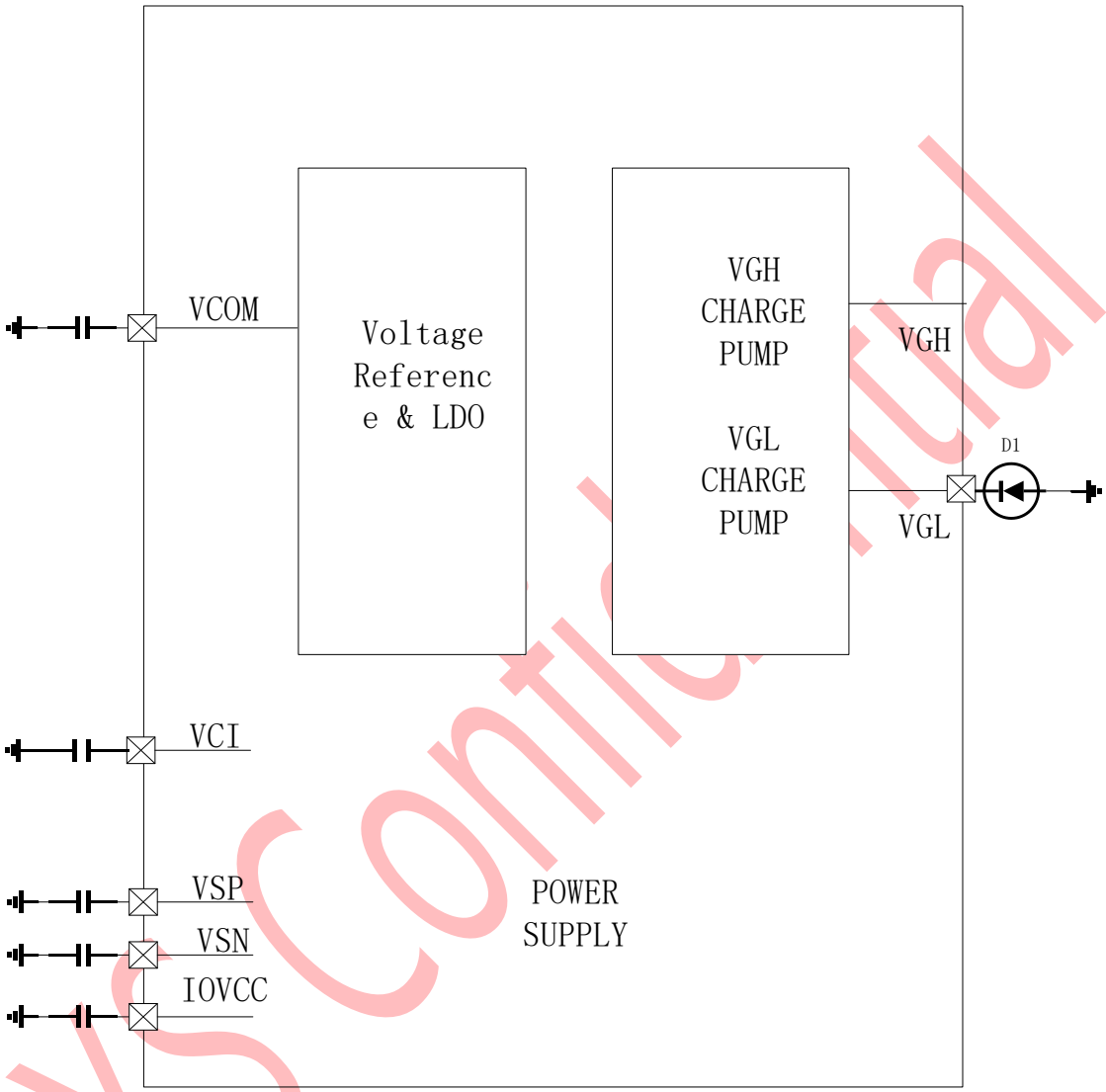

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3.9. Power Supply Peripheral Component List

No.	name	Signal name	Values	Max ability	Note
1	C1	IOVCC	1.0uF	10V	stabilizing capacitor
2	C2	VCI	1.0uF	10V	stabilizing capacitor
3	C3	VSP	4.7uF	10V	stabilizing capacitor
4	C4	VSN	4.7uF	10V	stabilizing capacitor
5	C5	VCOM	1.0uF	10V	stabilizing capacitor
6	D1	VGL	-	-	VGL - GND

*Note:please connect AXS if you have any question.

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4. INSTRUCTIONS

4.1. Outline

The AXS15231E supports high speed serial interface, MIPI, to configure the system via accessing command registers. While accessing the command registers, the information that indicates which register would be accessed should be sent first. After that, the new value can be updated via system interface. The MIPI-DSI is compliant with MIPI Alliance Standard for Display Serial Interface (DSI), Version 1.01.00 and D-PHY Version 1.00.00. Updating command instructions can also be accomplished by using all supporting system interfaces (MIPI, SPI, QSPI,DSPI and I-8080 8-bit parallel bus interface).

The AXS15231E has the following major categories of instructions:

(1). User Command List and Description.

(2). Manufacturer Command List and Description.

Since updating these instructions is asynchronous to the internal clock of the AXS15231E, the updating procedure will require no waiting cycles. Furthermore, the updating procedure will not interfere with the processing of the host controller, this makes instructions can be handled smoothly and efficiently.

The following contents of this chapter will describe the supported instructions in detail.

4.2. User Command List and Description

4.2.1. Introduction

After the H/W reset by RESX pin or S/W reset by SWRESET command, each internal register will return to the default state. The commands 10h, 20h, 21h, 28h, 29h, 36h will be updated only during V-sync periods while the module is in the “Sleep Out” mode to avoid abnormal visual effects, and will be updated immediately in the “Sleep In” mode.

4.2.2. System Command List

Name	Hex	Write/Read/ Command	Description	Parameter Number	Transmission
NOP	00h	C	No operation	0	MIPI/SPI/QSPI/DBI
SWRESET	01h	C	Software reset	0	MIPI/SPI/QSPI/DBI
RDDID	04h	R	Read display	3	MIPI/SPI/QSPI/DBI
RDNUMED	05h	R	Read Number of the Errors on DSI	1	MIPI/SPI/QSPI/DBI
RDDST	09h	R	Read display status	4	MIPI/SPI/QSPI/DBI
RDDPM	0Ah	R	Read display power	1	MIPI/SPI/QSPI/DBI
RDDMADCTL	0Bh	R	Read memory data access control	1	MIPI/SPI/QSPI/DBI
RDDIPF	0Ch	R	Read Interface Pixel Format	1	MIPI/SPI/QSPI/DBI
RDDIM	0Dh	R	Read display image	1	MIPI/SPI/QSPI/DBI
RDDSM	0Eh	R	Read display signal	1	MIPI/SPI/QSPI/D

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					BI
RDDSDR	0Fh	R	Read display self-diagnostic result	1	MIPI/SPI/QSPI/DBI
SLPIN	10h	C	Sleep in	0	MIPI/SPI/QSPI/DBI
SLPOUT	11h	C	Sleep out	0	MIPI/SPI/QSPI/DBI
PTLON	12h	C	Partial mode on	0	MIPI/SPI/QSPI/DBI
NORON	13h	C	Partial mode off(Normal)	0	MIPI/SPI/QSPI/DBI
INVOFF	20h	C	Display inversion off	0	MIPI/SPI/QSPI/DBI
INVON	21h	C	Display inversion on	0	MIPI/SPI/QSPI/DBI
ALLPOFF	22h	C	All pixel off	0	MIPI/SPI/QSPI/DBI
ALLPON	23h	C	All pixel on	0	MIPI/SPI/QSPI/DBI
ALLPFILL	24h	W	All pixel fill given color	3	MIPI/SPI/QSPI/DBI
GAMSET	26h	W	Gamma curve set	1	MIPI/SPI/QSPI/DBI
DISPOFF	28h	C	Display off	0	MIPI/SPI/QSPI/DBI
DISPON	29h	C	Display on	0	MIPI/SPI/QSPI/DBI
CASET	2Ah	W	Column address set	4	MIPI/SPI/QSPI/DBI
RASET	2Bh	W	Row address set	4	MIPI/SPI/QSPI/DBI
RAMWR	2Ch	W	Memory write	any length	MIPI/SPI/QSPI/DBI
RAMRD	2Eh	R	Memory read	any length	SPI/QSPI/DBI
RAWFILL	2Fh	W	Memory fill given color at window	3	MIPI/SPI/QSPI/DBI
PTLAR	30h	W	Partial start/end address set	4	MIPI/SPI/QSPI/DBI
PTLAR	31h	W	set_partial_columns	4	MIPI/SPI/QSPI/DBI
VSCRDEF	33h	W	Vertical scrolling definition	6	MIPI/SPI/QSPI/DBI
TEOFF	34h	C	Tearing effect line off	0	MIPI/SPI/QSPI/DBI
TEON	35h	W	Tearing effect line on	1	MIPI/SPI/QSPI/DBI
MADCTL	36h	W	Memory data access control	1	MIPI/SPI/QSPI/DBI
VSCRSADD	37h	W	Vertical scrolling start address	2	MIPI/SPI/QSPI/DBI
IDMOFF	38h	C	Idle mode off	0	MIPI/SPI/QSPI/DBI
IDMON	39h	C	Idle mode on	0	MIPI/SPI/QSPI/DBI
IPF	3Ah	W	Interface pixel format	1	MIPI/SPI/QSPI/DBI
RAMWRC	3Ch	W	Memory write continue	any length	MIPI/SPI/QSPI/DBI
RAMRDC	3Eh	R	Memory read continue	any length	SPI/QSPI/DBI

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TESCAN	44h	W	Set tear scanline	4	MIPI/SPI/QSPI/DBI
RDTESCAN	45h	R	Get tear scanline	4	MIPI/SPI/QSPI/DBI
WRDISBV	51h	W	Write display brightness value	1	MIPI/SPI/QSPI/DBI
RDDISBV	52h	R	Read display brightness value	1	MIPI/SPI/QSPI/DBI
WRCTRLD	53h	W	Write CTRL display	1	MIPI/SPI/QSPI/DBI
RDCTRLD	54h	R	Read CTRL dsiplay	1	MIPI/SPI/QSPI/DBI
RDFCHKSUM	Aah	R	Read First Checksum	1	MIPI/SPI/QSPI/DBI
RDCCHKSUM	Afh	R	Read Continue Checksum	1	MIPI/SPI/QSPI/DBI
RDID1	Dah	R	Read ID1	1	MIPI/SPI/QSPI/DBI
RDID2	Dbh	R	Read ID2	1	MIPI/SPI/QSPI/DBI
RDID3	Dch	R	Read ID3	1	MIPI/SPI/QSPI/DBI
DSTB	90h	W	Enter Deep-Standby	4	MIPI/SPI/QSPI/DBI

Note: LPDT (Low Power Mode), HSDT (High Speed Mode)

4.2.2.1. POFF (10H): Power Off Command

8'H10	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
description			power off command(10) with no parameter is used to turn off power								

4.2.2.2. PON (11H): Power On Command

8'H11	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
description			power on command(11) with no parameter is used to turn on power								

4.2.2.3. NSI (20H): No Src_Inv Command

8'H20	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
description			no src_inv command(20) with no parameter is used to exit the invertion of black and white picture								

4.2.2.4. SI (21H): Src_Inv Command

8'H21	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
description			src_inv command(21) with no parameter is used to enter the invertion of black and white picture								

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4.2.2.5. DOFF (28H): Display Off Command

8'H28	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
description			display off command(28) with no parameter is used to turn off display								

4.2.2.6. DON (29H): Display On Command

8'H29	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
description			display on command(29) with no parameter is used to turn on display								

4.2.2.7. CWA (2AH): Column Windows Address Command

8'H2a	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
par0	↑	-						cr_2a_sc_src[10:8]			8'h00
par1	↑	-	cr_2a_sc_src[7:0]								8'h00
par2	↑	-						cr_2a_ec_src[10:8]			8'h00
par3	↑	-	cr_2a_ec_src[7:0]								8'h00
Description			When cr_win_en =1,2a, 2b window opening function is effective ; **cr_2a_sc_src:** represent row/column start/stop address in command mode display **cr_2a_ec_src:** represent row/column start/stop address in command mode display;								

4.2.2.8. RWA (2BH): Row Windows Address Command

8'H2b	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
par0	↑	-					cr_2b_sr_src[11:8]				8'h00
par1	↑	-	cr_2b_sr_src[7:0]								8'h00
par2	↑	-					cr_2b_er_src[11:8]				8'h00
par3	↑	-	cr_2b_er_src[7:0]								8'h00
Description			**cr_2b_sr_src:** represent row/column start/stop address in command mode display; **cr_2b_er_src:** represent row/column start/stop address in command mode display;								

4.2.2.9. WMS (2CH): write memory start

8'H2c	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
par0	↑	-	Pixel Data 0								8'h00
par1	↑	-	Pixel Data 1								8'h00
par2	↑	-	Pixel Data 2								8'h00
parN	↑	-	Pixel Data N								8'h00
Description			This command transfers image data from the host processor to the display module's frame memory starting at the pixel location specified by preceding set_column_address and set_page_address commands (Vsync) .								

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4.2.2.10.WMC (3CH): write memory continue

8'H3c	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
par0	↑	-	Pixel Data 0								8'h00
par1	↑	-	Pixel Data 1								8'h00
par2	↑	-	Pixel Data 2								8'h00
parN	↑	-	Pixel Data N								8'h00
Description			This command transfers image data from the host processor to the display module's frame memory continuing from the pixel location following the previous write_memory_continue or write_memory_start command（Hsync）.								

4.2.2.11.RMS (2EH): read memory continue

8'H2e	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
par0	-	↑	Pixel Data 0								8'h00
par1	-	↑	Pixel Data 1								8'h00
par2	-	↑	Pixel Data 2								8'h00
parN	-	↑	Pixel Data 3								8'h00
Description			his command transfers image data from the display module's frame memory to the host processor starting at the pixel location specified by preceding set_column_address and set_page_address commands.								

4.2.2.12.RMC (3EH): read memory continue

8'H3e	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
par0	-	↑	Pixel Data 0								8'h00
par1	-	↑	Pixel Data 1								8'h00
par2	-	↑	Pixel Data 2								8'h00
parN	-	↑	Pixel Data 3								8'h00
Description			This command transfers image data from the display module's frame memory to the host processor continuing from the location following the previous read_memory_continue or read_memory_start command								

4.2.2.13.ICI (04H): IC Information

8'H04	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
par0	-	↑	cr_manufacture_id								8'h00
par1	-	↑	cr_driver_version_id								8'h00
par2	-	↑	cr_driver_id								8'h00
par3	-	↑	cr_id_dummy								8'h00
Description			**cr_manufacture_id**：the manufacture_id of the IC.								

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	cr_driver_version_id：the version_id of the IC. **cr_driver_id**：the IC id. **cr_id_dummy**：is cr_id_dummy_rev0,the dummy id0 that reserved. The above registers look at the C0 command in detail.

4.2.2.14.RDNUMED(05H): Read Number of the Errors on DSI

8'H05	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
par0	-	↑	dsi_err_overflow	dsi_err_num							8'h00
description			The first parameter is telling a number of the errors on DSI. cr_ecc_en=1:Enable the mipi ecc function. cr_mipi_crc_en=1:Enable the mipi crc function. **dsi_err_num**：ecc error number +crc error num **dsi_err_overflow**：dsi_err_num——Overflow flag。								

4.2.2.15.RDDST (09H): Read Display Status

8'H09	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
par0	-	↑	booster_en	my	mx	mv	ml	cr_bgr	cr_ca	Cr_gs	8'h80
par1	-	↑		cr_itf_format			idle_mode	cr_partial_en	pwr_on	normal_dsp_en	8'h50
par2	-	↑	cr_vscroll_en		src_inv			dsp_on	tear_on	cr_ga_curve[2]	8'h00
par3	-	↑	cr_ga_curve[1:0]		cr_tear mode						8'h40
description			Read command(21/20/36/10/11/28/29/3a) **booster_en**：The charge pump boost function was enabled.（vgh/vgl/vsp/vsn）. **idle_mode:** 38/39h command flag. If the 39h command is sent, this bit is 1. If the 38h command is sent, this bit is 0. **cr_partial_en**：The enable flag is partially displayed. If the 12h command is sent, this bit is 1, and if the 13h command is sent, this bit is 0. **normal_dsp_en**：Contrary to cr_partial_en. **pwr_on**：If the 11 command is sent, the bit is 1. If the 10 command is sent, the bit is 0. cr_vscroll_en: 33/37h Indicates that the running horse light function is enabled. This bit is 1, indicating that the running horse light function is enabled. **src_inv**：Indicates the reverse flag bit of 0 and 1. If the flag bit is 1, the 21h command is sent. If the flag bit is 0, the 20 command is sent. **dsp_on**：If the command is sent 29, the bit is 1. If the command is sent 28, the bit is 0.									

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	tear_on：If the 35 command is sent, the bit is 1. If the 34 command is sent, the bit is 0. **cr_ga_curve**：gamma curve option. **cr_tear_mode**：1 indicates that TE is H-blanking+V-blanking, and 0 indicates that TE is V-blanking.

4.2.2.16.RDDMADCTL(0AH): Read Display MADCTL

8'H0A	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Par0	-	↑	booster_en	idle_mode	cr_partial_en	pwr_on	normal_dsp_en	dsp_on	-	-	8'h80
Description			**booster_en**: charge pump Enable/disable switch **idle_mode:** 38/39h command flag. If the 39h command is sent, this bit is 1. If the 38h command is sent, this bit is 0. **pwr_on**：If the 11 command is sent, the bit is 1. If the 10 command is sent, the bit is 0. **cr_partial_en**：The enable flag is partially displayed. If the 12h command is sent, this bit is 1, and if the 13h command is sent, this bit is 0. **normal_dsp_en**：Contrary to cr_partial_en. **dsp_on**：If the command is sent 29, the bit is 1. If the command is sent 28, the bit is 0.								

4.2.2.17.RDDMADCTL(0BH): Read Display MADCTL

8'H0B	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Par0	-	↑	MY	MX	MV	ML	RGB	MH	-	-	8'h00
Description			Read back the parameter of command word 36h.								

4.2.2.18.RDDCOLMOD(0CH): Read Display Pixel Format

8'H0C	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Par0	-	↑	0	cr_rgb_format			0	cr_itf_format			8'h55
Description			Read back the parameter of command word 3Ah. cr_rgb_format：RGB interface pixel format option. cr_itf_format：dbi、spi、qspi interface pixel format option.								

4.2.2.19.RDDMADCTL(0DH): Read Display MADCTL

8'H0D	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Par0	-	↑	cr_vscroll_en	pix_win_en	src_inv	wfull_fifo	rempty_fifo	cr_ga_curve_usr			8'h09

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Description	Read back the parameter of command word 2f、21/20、26h. **cr_vscroll_en:** 33/37h Indicates that the running horse light function is enabled. This bit is 1, indicating that the running horse light function is enabled. **pix_win_en**：2fh command enable flag, valid with 1. **src_inv**：Indicates the reverse flag bit of 0 and 1. If the flag bit is 1, the 21h command is sent. If the flag bit is 0, the 20 command is sent. **wfull_fifo:**22, 23, 24, 2fh Cache fifo full flag, the depth of the fifo is 8. **rempty_fifo:**22, 23, 24, 2fh Cache the fifo empty flag. **cr_ga_curve_usr**：The gamma curve option reads back the parameters of the ox26 command.

4.2.2.20.RDDSM (0Eh): Read Display Signal Mode

8'H0E	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Par0	-	↑	TEON	TEM	HS	VS	PixelClk	DataEn	0	ErrorDSI	8'h00

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
TEON	Tearing effect line on/off	'1' = ON, '0' = OFF,
TEM	Tearing effect line mode	'1' = mode2, '0' = mode1,
HS	Horizontal Sync (RGB interface)	'1' = ON, '0' = OFF,
VS	Vertical Sync (RGB interface)	'1' = ON, '0' = OFF,
PixelClk	Pixel Clock (DOTCLK, RGB interface)	'1' = ON, '0' = OFF,
DataEn	Data Enable (DE, RGB interface)	'1' = ON, '0' = OFF,
ErrorDSI	Error On DSI (MIPI Interface)	'1' = Error, '0' = No Error

4.2.2.21.RDDSDR (0Fh): Read Display Self-Diagnostic Result

8'H0F	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Par1	-	↑	otp_crc_done	ctn_crc_done	0					otp_crc_ok	8'h00

Description

This command indicates the current status of the display self-diagnostic result **after sleep out command** as described（detection function）below:

otp_crc_done:otp was loaded and crc test was completed.
ctn_crc_done: The host reconfigures the registers and the crc check ends.
otp_crc_ok: otp Checksums Comparison, '0' = Checksums are same ,'1' = Checksums are not same
See sections: "Read First Checksum (Aah)" and "Read Continue Checksum (Afh)"

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4.2.2.22.RDID1 (DAH): Read ID1

8'HDA	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
par0	-	↑	cr_da_dataid								8'h21
par1	-	↑	cr_da_par0								8'h40
par2	-	↑	cr_da_par1								8'h00
par3	-	↑	cr_da_ecc								8'h38
Description			**cr_da_dataid**: command da's data id; **cr_da_par0:** command da's parameter byte0; **cr_da_par1:** command da's parameter byte1; **cr_da_ecc**: command da's ecc; Note: mipi reads back four parameters. Other interfaces only read back cr_da_par0.								

4.2.2.23.RDID2 (DBH): Read ID2

8'HDB	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
par0	-	↑	cr_db_dataid								8'h21
par1	-	↑	cr_db_par0								8'h00
par2	-	↑	cr_db_par1								8'h00
par3	-	↑	cr_db_ecc								8'h12
Description			**cr_db_dataid**: command db's data id; **cr_db_par0**: command db's parameter byte0; **cr_db_par1**: command db's parameter byte1; **cr_db_ecc**: command db's ecc; Note: mipi reads back four parameters. Other interfaces only read back cr_da_par0.								

4.2.2.24.RDID3 (DCH): Read ID3

8'HDC	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
par0	-	↑	cr_dc_dataid								8'h21
par1	-	↑	cr_dc_par0								8'h03
par2	-	↑	cr_dc_par1								8'h00
par3	-	↑	cr_dc_ecc								8'h14
Description			**cr_dc_dataid**: command dc's data id; **cr_dc_par0**: command dc's parameter byte0; **cr_dc_par1**: command dc's parameter byte1; **cr_dc_ecc**: command dc's ecc; Note: mipi reads back four parameters. Other interfaces only read back								

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	cr_da_par0.

4.2.2.25.RBL (52H): Read Display Brightness Value

8'H52	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
par0	-	↑	cr_bl [7:0]								8'h80
Description			This command returns the brightness value of the display.								

4.2.2.26.RDCTRLD (54H): Read CTRL value Display

8'H54	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
par0	-	↑	-	-	BCTRL	-	DD	BL	-	-	8'h00
description			This command returns ambient light and brightness control values. Read back the parameter of command word 53h.								

4.2.2.27.GSCAN (45H): Get Scanline

8'H45	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
par0	-	↑	cr_44te_str[11:8]								8'h00
par1	-	↑	cr_44te_str[7:0]								8'h00
par2	-	↑	cr_44te_end[11:8]								8'h00
par3	-	↑	cr_44te_end[7:0]								8'h00
description			-The display module returns the current scanline ,N, used to update the display device. The total number of scanlines on a display device is defined as VSYNC+VBP+VACT+VFP. The first scanline is defined as the first line of V Sync and is denoted as Line 0. -When in sleep in mode, the value returned by get scanline is undefined. Note: that Set Tear Scan Line with N = 0 is equivalent to Tearing Effect Line ON with M = 0. Read back the parameter of command word 44h.								

4.2.2.28.RDFCS (AaH):Read First Checksum

8'HAa	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
par0	-	↑	fst_chk_sum[15:8]								8'hff
Par1	-	↑	fst_chk_sum[7:0]								8'hff
description			This command returns the **first checksum** what has been calculated from **User's area registers** and **the frame memory** after the write access to those registers and/or frame memory has been done.								

4.2.2.29.RDCFCS (AfH):Read Continue Checksum

8'HAf	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
par0	-	↑	ctn_chk_sum[15:8]								8'hff

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Par1	-	↑	ctn_chk_sum[7:0]	8'hff
description			This command returns the **continue checksum** what has been **calculated continuously** after the first checksum has calculated from User's area registers and the frame memory after the write access to those registers and/or frame memory has been done.	

4.2.2.30.SWRESET (01H): Software Reset

8'H01	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
description			The drv soft reset. cr_soft_rstn_tp_opt=0,TP soft reset can reset drv; cr_soft_rstn_tp_opt=1,TP soft reset cannot reset drv. If the TP register cr_soft_rstn_drv_opt=0, DRV soft reset can reset TP. If the TP register cr_soft_rstn_drv_opt=1, DRV soft reset cannot reset TP.								

4.2.2.31.SA (33H): Scroll Area Command

8'H33	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
par0	↑	-	cr_33_tfa[15:8]								8'h00
par1	↑	-	cr_33_tfa[7:0]								8'h00
par2	↑	-	cr_33_vsa[15:8]								8'h00
par3	↑	-	cr_33_vsa[7:0]								8'h00
par4	↑	-	cr_33_bfa[15:8]								8'h00
par5	↑	-	cr_33_bfa[7:0]								8'h00
Description			command table2 when cr_vscroll_en =1, the running horse light function is effective; **cr_33_tfa**：top fix area. **cr_33_vsa**：vertical scroll area. **cr_33_bfa**：bottom fix area.								

4.2.2.32.SS (37H): Scroll Start Command

8'H37	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
par0	↑	-	cr_37_vsp[15:8]								8'h00
par1	↑	-	cr_37_vsp[7:0]								8'h00
Description			**cr_37_vsp**：vertical scroll position.								

4.2.2.33. WRCTRLD (53H): Write CTRL Display

8'H53	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
par0	↑	-	-	-	BCTRL	-	DD	BL	-	-	8'hxx

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description	This command is used to control display brightness. **BCTRL**：Brightness Control Block On/Off,BCTRL=1 indicates that the backlight adjustment function is enabled. **DD**：Display Dimming On/Off,DD=1 indicates that the backlight climbing function is enabled. **BL**：Backlight Control On/Off,BL=1 indicates turning on the backlight. BL=0 indicates that the backlight is turned off immediately.

4.2.2.34.BL (51H): Back Light Command

8'H51	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
par0	↑	↑	cr_bl [7:0]								8'h80
Description			cr_bl：Adjust the backlight; cr_bl [7:0] is '0' when bit BCTRL of write CTRL display command (53h) is '0' cr_bl [7:0] is manual set brightness specified with write CTRL display command (53h) when bit BCTRL is '1'； This function is to adjust the duty cycle of PWM.								

4.2.2.35.COLMOD (3AH): Interface Pixel Format

8'H3A	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
par0	↑	-	-	D[6:4]			-	D[2:0]			8'h55

Description

This command is used to **define the format of RGB picture data**, which is to be transferred **via the MCU interface**.
When command table2 custom register cr_format_cmd3a_en =1, the pixel format is configured by the 3Ah command, otherwise it is determined by command table2, as shown in the following table.
For mipi format, cr_pix_sel is set to 1

D[6:4]: DPI Pixel Format Definition（RGB）
D[2:0]: DBI Pixel Format Definition

The formats are shown in the table:

Bit	Description	
D7	-	Set to '0'
D6	RGB interface color format	'101' = 16bit/pixel '110' = 18bit/pixel
D5		
D4		
D3	-	Set to '0'
D2	Control interface color format	'101' = 16bit/pixel '110' = 18bit/pixel '111' = 24 bit/pixel
D1		
D0		

Deault: 16bits/pixel

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Description **command table2**	

Interface	Register	Pix_format
SPI	cr_spi_format	0：565 1：888
DBI	cr_dbi_format[1:0]	00：565 10：666 01：666L 11：888
RGB	cr_ext_format[1:0]	00：565 10：666 01：666L 11：888
MIPI	1、cr_pix_otp[2:0] 2、decode from D0P/D0N	110：666L 111：888
QSPI	cr_qspis_datamode[2:0]	000（mipi111）：888 001（101）：565 010（010）：332 011（001）、111 100（000）：gray_mode
	IC requirements	565 666

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4.2.2.36.DCTR (36H): Display Control Command

8’H36	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
par0	↑	↑	MY	MX	MV	ML	BGR	MH	cr_ca	cr_gs	8’h00

Description

cr_gs: gip scan direction setting.

cr_gs	cr_fv	result
0	0	FW, select D7 and D8 register groups
0	1	BW, select D9 and DD register groups
1	0	FW, select D7 and D8 register groups
1	1	BW, select D9 and DD register groups

cr_ca: the data invert option for data_shift block.

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dsh_shr = cr_dsh_shr ^ cr_ca ^ cr_mx ^ cr_mh

(when dsh_shr = 0, invert; when dsh_shr = 1, don't invert).

cr_dsh_shr	cr_ca	cr_mx =MX^ cr_36_opt[1]	cr_mh =MH^ cr_36_opt[4]	result
0	0	0	0	Left and right mirror
0	0	0	1	Normal
0	0	1	0	Normal
0	0	1	1	Left and right mirror
0	1	0	0	Normal
0	1	0	1	Left and right mirror
0	1	1	0	Left and right mirror
0	1	1	1	Normal
1（default）	0（default）	0（default）	0（default）	Normal
1	0	0	1	Left and right mirror
1	0	1	0	Left and right mirror
1	0	1	1	Normal
1	1	0	0	Left and right mirror
1	1	0	1	Normal
1	1	1	0	Normal
1	1	1	1	Left and right mirror

MY：Up and down the mirror

MY	cr_36_opt[0]	ML	cr_36_opt[31]	result
0（default）	0（default）	0（default）	0（default）	Normal
0	0	0	1	Up and down mirror
0	0	1	0	Up and down mirror
0	0	1	1	Normal
0	1	0	0	Up and down mirror
0	1	0	1	Normal
0	1	1	0	Normal
0	1	1	1	Up and down mirror
1	0	0	0	Up and down mirror
1	0	0	1	Normal
1	0	1	0	Normal
1	0	1	1	Up and down mirror
1	1	0	0	Normal
1	1	0	1	Up and down mirror
1	1	1	0	Up and down mirror
1	1	1	1	Normal

MX：Left and right mirror.

MV：Transpose, with up and down mirroring or left and right mirroring to get a 90 degree rotation.

MV	cr_36_opt[2]	result
0	0	normal
0	1	transposition
1	0	transposition
1	1	normal

ML: Up and down the mirror

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MH：Left and right mirror.

BGR：sub_pixel order of one pixel data setting，

cr_bgr_en	BGR	cr_bgr_opt	result
0	0	0	RGB（default）
0	0	1	BGR
0	1	0	BGR
0	1	1	RGB
1	0	0	RGB
1	0	1	RGB
1	1	0	RGB
1	1	1	RGB

Bit	NAME	DESCRIPTION
MY	Row Address Order	These 3bits controls MCU to memory write/read direction.
MX	Column Address Order	
MV	Row/Column Exchange	
ML	Vertical Refresh Order	LCD vertical refresh direction control '0' = LCD vertical refresh Top to Bottom '1' = LCD vertical refresh Bottom to Top
RGB	RGB-BGR ORDER	Color selector switch control '0' =RGB color filter panel, '1' =BGR color filter panel
MH	Horizontal Refresh Order	Horizontal direction '0' = Left to Right '1' = Right to Left

4.2.2.37.GAMSET (26h): Gamma curve set

8'H26	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Par0	-	↑						cr_ga_curve_usr			8'h01

Description

This command selects the desired gamma curve for the display device. Four fixed gamma curves are defined in section 5.2. A curve is selected by setting the appropriate bit in the parameter as described in the following table.
When the command table2 custom register cr_ga_cur_usren =1, the GAMMAM curve is configured by the 26h command, otherwise it is determined by the cr_ga_curve of command table2.

Table 7 Gamma Curves

GC[7:0]	Parameter	Curve Selected
00h	None	No curve selected
01h	GC0	Gamma Curve 1
02h	GC1	Gamma Curve 2
04h	GC2	Gamma Curve 3
08h	GC3	Gamma Curve 4

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4.2.2.38.PTLON (12H): Partial Display Mode On

8'H12	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
description			Enable the partial display function, that is, cr_partial_en =1. The upper and lower boundary of the local display area is determined by the 30H command word. The left and right boundary of the local display area is determined by 31H command word. Local display area (within the boundary position) displays normal picture content; The non-local display area (outside the boundary position) is configured by the register. （cr_partial_value_r，cr_partial_value_g，cr_partial_value_b）。								

4.2.2.39.NORON (13H): Normal Display Mode On（Partial mode off）

8'H13	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
description			Disable the partial display function and switch to the normal display mode, that is, cr_partial_en =0.								

4.2.2.40.PTLAR (30H):set_partial_rows

8'H30	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
par0	↑	-	PSL[15:8]								8'h00
par1	↑	-	PSL[7:0]								8'h00
par2	↑	-	PEL[15:8]								8'h00
Par3	↑	-	PEL[7:0]								8'h00
description			PSL[15:0]: local display of the starting line; PEL[15:0]: local display end line;								

4.2.2.41.PTLAR (31H):set_partial_columns

8'H31	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
par0	↑	-	PSC[15:8]								8'h00
par1	↑	-	PSC[7:0]								8'h00
par2	↑	-	PEC[15:8]								8'h00
Par3	↑	-	PEC[7:0]								8'h00
description			PSC[15:0]: Locally displays the starting column; PEC[15:0]: local display end column;								

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4.2.2.42.TEOFF (34H): Tearing Effect Line OFF

8'H34	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
description			Disables Tearing Effect output signal from TE signal line, i.e. tear_on = 0.								

4.2.2.43.TEON (35H): Tearing Effect Line On

8'H35	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
par0	↑	-								TEM	8'hxx
description			Send 35h, that is, tear_on = 1, Tearing Effect Line On. TEM determines the Tearing Effect Output Line mode. 1、TEM =0: The Tearing Effect output line consists of **V-Blanking** information only。 2、TEM =1: The Tearing Effect output Line consists of both **V-Blanking** and **H-Blanking** information。 The TE of H-blanking is determined by C5 of command table2: cr_te_gsps: start column position; cr_te_gspf: end column position.								

4.2.2.44.STE (44H): Set Tear Scanline

8'H44	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
par0	↑	-	cr_44te_str[11:8]								8'h00
Par1	↑	-	cr_44te_str[7:0]								8'h00
par2	↑	-	cr_44te_end[11:8]								8'h00
Par3	↑	-	cr_44te_end[7:0]								8'h00
description			-This command turns on the display module's Tearing Effect output signal on the TE signal line when the display module reaches line N. The TE signal is not affected by changing MV. -The tearing effect line on has one parameter that describes the tearing effect output line mode. -The tearing effect output line consist of V-blanking information only. Note that set tear scanline with N=0 is equivalent to tearing effect line on with TEM=0. The tearing effect output line shall be active low when the display module is in sleep mode。 cr_44te_str: start line; cr_44te_end: indicates the end line When the command table2 custom register cr_te_44en =1, the TE position is configured by the 44h command, otherwise it is determined by the cr_te_str and cr_te_end of command table2.								

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4.2.2.45. IDMON (39H): Idle mode on

8'H39	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default

description			Enter Idle mode, that is, the eight-color mode.
			The register configuration is as follows :
			vedio mode: cr_idle_mode_en = 1
			The command mode:
			cr_idle_mode_en=1;
			cr_corr_col_en = 0;
			cr_gray_high = 'h80.								

4.2.2.46.IDMOFF (38H): Idle Mode Off

8'H38	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
description			Exit Idle mode.								

4.2.2.47.ALLPOFF (22H): All Pixels off

8'H22	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
description			In the display state, send this command and fill **the black data** with GRAM to clear the entire screen to black. Used to quickly clear the full screen.								

4.2.2.48.ALLPON (23H): All Pixels on

8'H23	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
description			In the display state, send this command and fill GRAM with **white data** to clear the entire screen to white. Used to quickly clear the full screen.								

4.2.2.49.ALLPFILL (24H): All Pixels fill given color

8'H24	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
par0	↑	-	cr_24_datar								8'h00
Par1	↑	-	cr_24_datag								8'h00
par2	↑	-	cr_24_datab								8'h00
description			In the display state, the instruction is sent and **the specified color data** is filled with GRAM to clear the whole screen to the given color, as specified by the parameter of the instruction.								

4.2.2.50.RAWFILL (2FH): Memory fill given color

8'H2f	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
par0	↑	-	cr_2f_datar								8'h00
Par1	↑	-	cr_2f_datag								8'h00

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par2	↑	-	cr_2f_datab	8'h00
description			1, send 2A, 2B to specify the Gram area, and then send 2F instruction, the specified Gram area is clear to the given color, the specified color is specified by the parameter of the instruction. For quick monochromatic filling areas. 2, 22, 23, 24, 2fh can be cached through the fifo, so that the host can do other things when the burst has finished issuing these instructions. 3. This instruction can be used to achieve fast rectangular filling functions, such as drawing rectangles, drawing lines and so on. It can speed up and save data transmission power consumption.	

4.2.2.51.DSTB (90H): Enter deep standby

8'H90	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
par0	↑	-	8'hA5								8'h00
Par1	↑	-	8'h5A								8'h00
par2	↑	-	8'h15								8'h00
par3	↑	-	8'h23								8'h00
description			With the 90 command, you can say A5,5A,15,23 to form a sequence, Method 1: When scan reg cr_vdd_off_soft_en (scan reg 0x1E bit7) =1 and cr_dstb_det_int_en (scan reg 0x19 bit6) =1, interrupt is triggered. ext_int4, As the interrupt of MCU (the interrupt is enabled as cr_dstb_det_int_en and the interrupt flag bit is bit7 of SFR REG 0xBC). MCU issues DSTB command (with scan reg's cr_vdd_off_trig (0x8A) to generate 0xAA 0x55 sequence) to measure VDD_OFF_TRIG_CLK_DTA(.ts_in05) (16 cycle clock (1MHz)). It is used to enter deep sleep mode and be awakened by RSTN_PIN; Method 2: When scan reg's cr_vdd_off_soft_en=0, measure VDD_OFF_TRIG_CLK_DTA (16-cycle clock (1MHz)), and send the clock to the analog. After receiving the clock signal, the analog will shut down the entire digital power supply VDD and enter the very low power mode. That is, the hardware shuts down vdd directly and RSTN_PIN wakes up.									

4.3. QSPI/SPI/MCU read ID function

4.3.1.1. Description

If we want to realise the QSPI/SPI/MCU read-id function, we can operate in the same procedure as normal registers read. The read-id commands include cr_rdid_index, cr_rdid_index2. They can be configured by register command C2/C5 /CA/CB/CC.

4.3.1.2. MCU/SPI/QSPI Read ID Number Configure

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Index	Read number	Package content
cr_rdid_index	22 bytes	C2

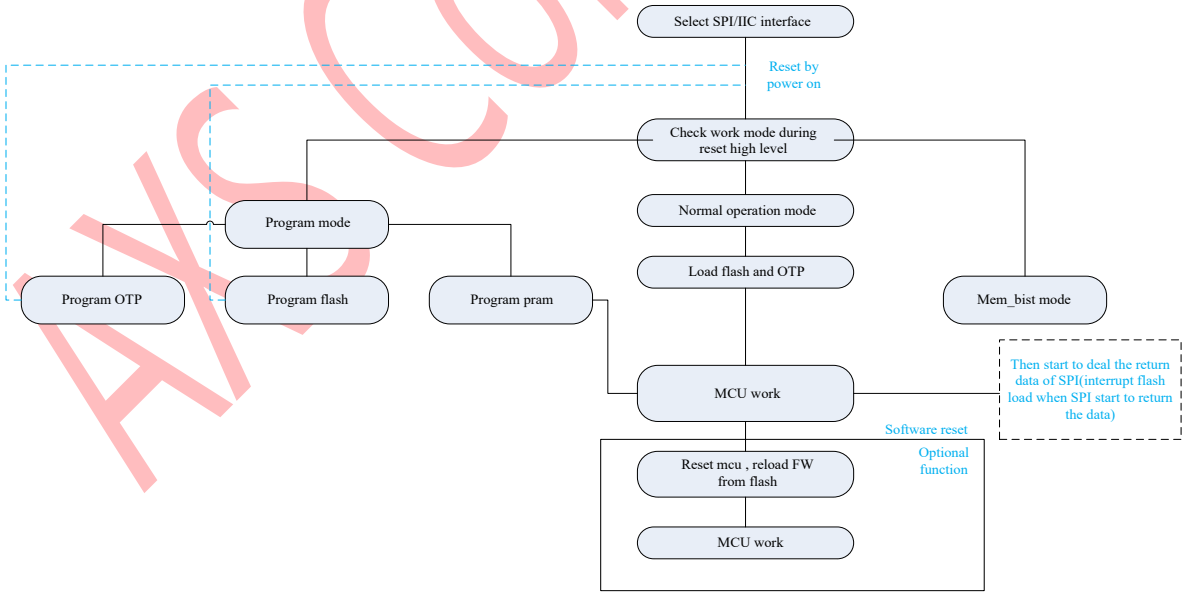
Index	Read number	Package content
cr_rdid_index2	9 bytes	cr_da_par0(CA) cr_db_par0(CB) cr_dc_par0(CC) cr_id_crc0(C5) cr_id_crc1(C5) cr_rd_sel_d0(C5) cr_rd_sel_d1(C5) cr_rd_sel_d2(C5) cr_rd_sel_d3(C5)

5. FUNCTIONS

5.1. Touch

5.1.1. TP work flow

First, select the SPI or I2C interface to work through the work mode PIN. Then Write program into flash or pram with a different interface; Finally, please reset if writing program into flash or otp, and directly enter into MCU work mode if writing program into pram.



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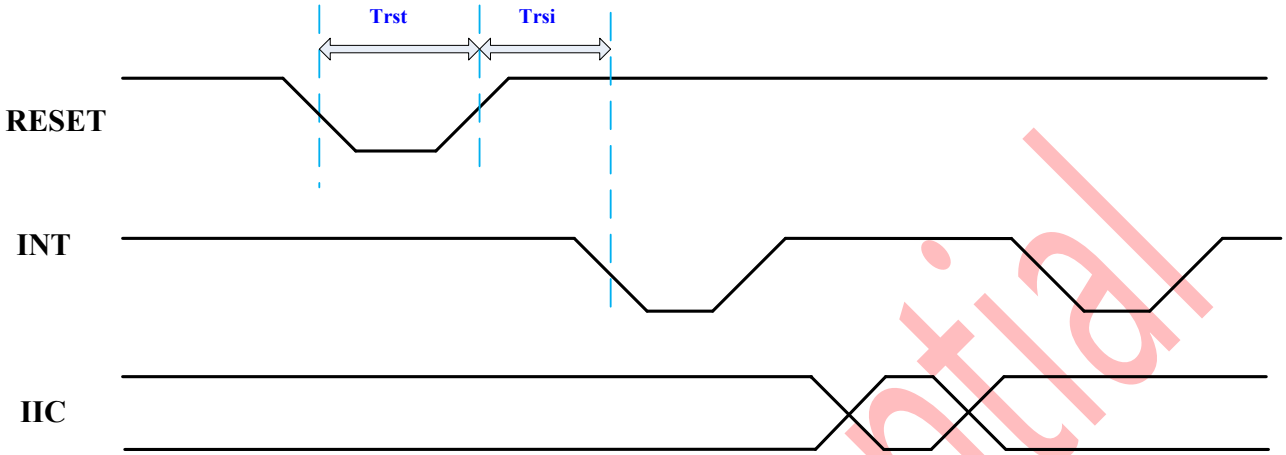
5.1.2. Touch Reset (RSTN) input timing

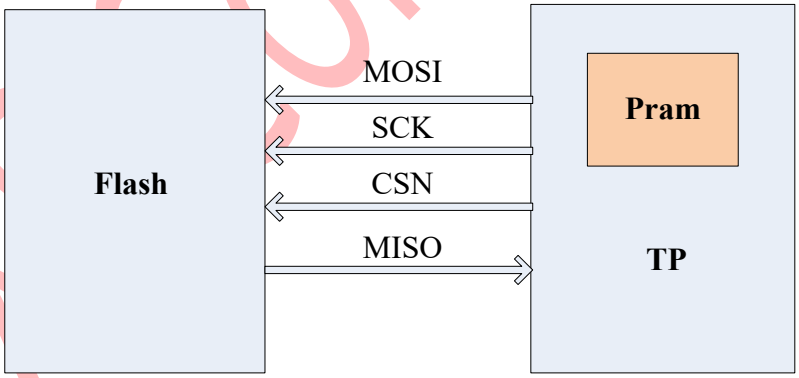
Reset time must be enough to guarantee reliable reset.



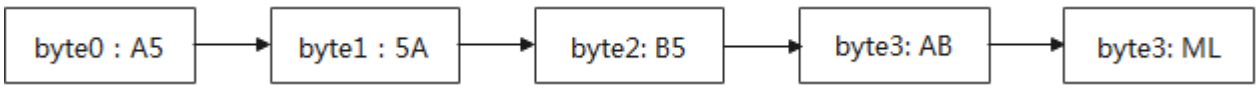
Parameter	Descrlption	Min	Max	Units
Trsi	Time of starting to report point after resetting	200	--	ms
Trst	Reset time	5	--	ms

5.1.3. Firmware booting

Touch firmware can boot from external flash or from AP optional, default is from external flash. Boot block diagram as follows.



Touch controller can also boot firmware from AP through I2C or SPI interface. booting firmware protocol as follows,



byte0~byte3 is character string, it means enable booting. and ML is mode flag. when ML=1, select boot firmware from the host. it is an optional to select I2C or SPI interface through WORK_MODE pin. When WORK_MODE = 1, I2C active, otherwise, SPI active.

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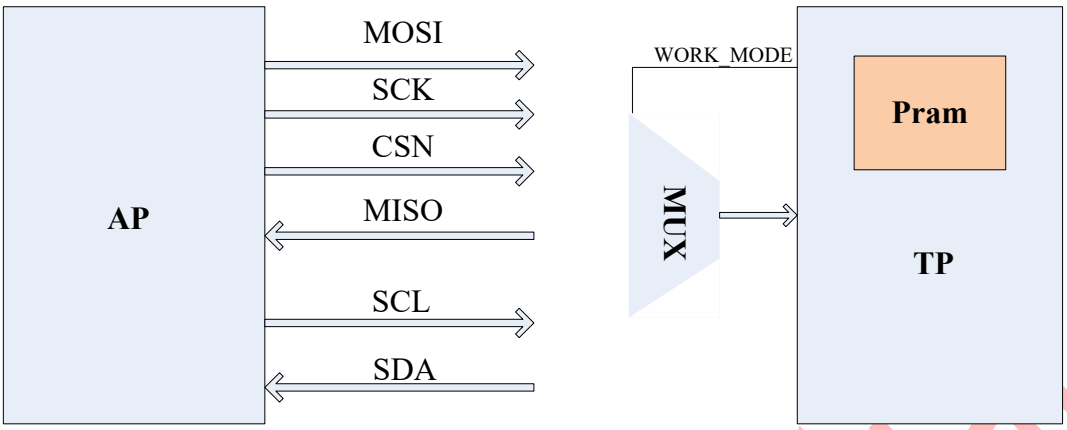


5.2. MIPI-DSI Interface

5.2.1. General description

The communication can be separated into two different levels between the host and the display module:

– Interface Level: Low level communication, low power
– Packet level: High level communication, high speed

5.2.2. Interface level communication

5.2.2.1. General

The display module uses data and clock lane differential pairs for DSI. Both clock lane and data lane can be driven in Low Power (LP) or High Speed (HS) mode.

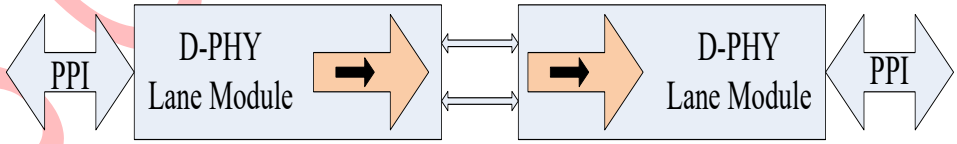
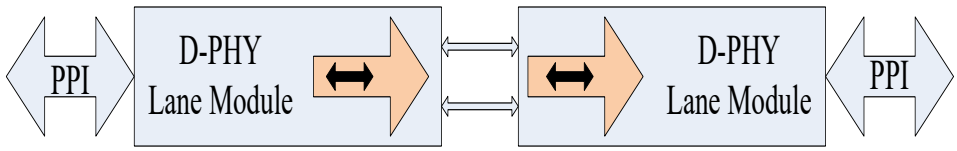
-	Lane support mode	MPU(Host) AXS15231E(Slave)
Clock Lane	Unidirectional lane •High-Speed Clock only •SimplifiedEscape Mode (ULPS Only)	
Data Lane	Bi-directional lane • Forward high-speed only •Bi-directional Escape Mode •Bi-direction LPDT	

Table: Lane types and support mode

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Low Power mode means that each line of the differential pair is used in single end mode and a differential receiver is disabled (The termination resistor of the receiver is disable) and it can be driven into a low power mode.

High Speed mode means that differential pairs (The termination resistor of the receiver is enabled) are not used in the single end mode.

There are different modes and protocols in each mode when transferring information from the HOST to the display module and vice versa.

The State Codes of the High Speed (HS) and Low Power (LP) lane pair are defined below.

Lane Pair State Code	Line DC Voltage Levels		High Speed (HS)	Low-Power (LP)	
	Dn+ Line	Dn- Line	Burst Mode	Control Mode	Escape Mode
HS-0	Low (HS)	High (HS)	Differential-0	Note 1	Note 1
HS-1	High (HS)	Low (HS)	Differential-1	Note 1	Note 1
LP-00	Low (LP)	Low (LP)	Not Defined	Bridge	Space
LP-01	Low (LP)	High (LP)	Not Defined	HS-Request	Mark-0
LP-10	High (LP)	Low (LP)	Not Defined	LP-Request	Mark-1
LP-11	High (LP)	High (LP)	Not Defined	Stop	Note 2

Table: High Speed and Low-Power Lane Pair State Descriptions

5.2.2.2. DSI-CLK lanes

DSI-CLK+/- lanes can be driven into three different power modes: Low Power Mode (LPM LP-11), Ultra Low Power Mode (ULPM) or High Speed Clock Mode (HSCM).

Clock lanes are in a single end mode (LP = Low Power) when there is entering or leaving Low Power Mode(LPM) or Ultra Low Power Mode (ULPM).

Clock lanes are in the single end mode (LP = Low Power) when there is entering in or leaving out High Speed Clock Mode (HSCM).

These entering and leaving protocols are using clock lanes in the single end mode to generate an entering or leaving sequences.

The principal flow chart of the different clock lanes power modes is illustrated below.

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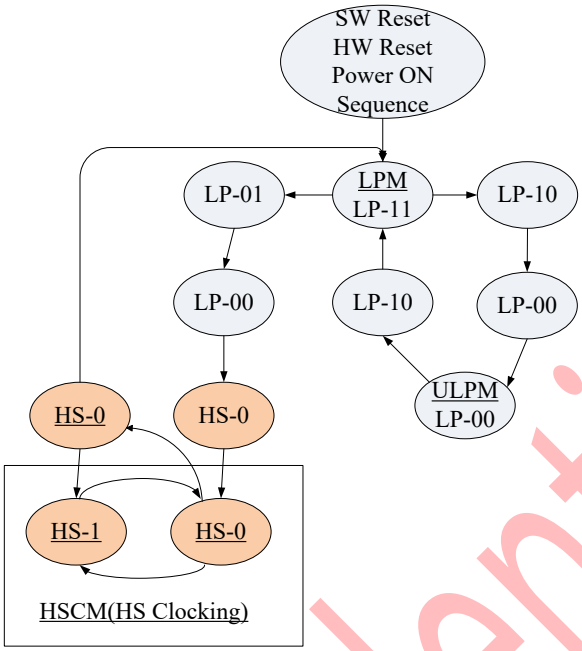

Figure: Clock Lanes Power Modes

Notes:

1. Low-Power Receivers (LP-Rx) of the lane pair are checking the LP-00 state code, when the Lane Pair is in the High Speed (HS) mode.

2. If Low-Power Receivers (LP-Rx) of the lane pair recognizes LP-11 state code, the lane pair returns to LP-11 of the Control Mode.

Low Power Mode (LPM)

DSI-CLK+/- lanes can be driven to the Low Power Mode (LPM), when DSI-CLK lanes are entering the LP-11 State Code, in three different ways:

1) After SW Reset, HW Reset or Power On Sequence =>LP-11

2) After DSI-CLK+/- lanes are leaving Ultra Low Power Mode (ULPM, LP-00 State Code) =>LP-10 =>LP-11 (LPM). This sequence is illustrated below.

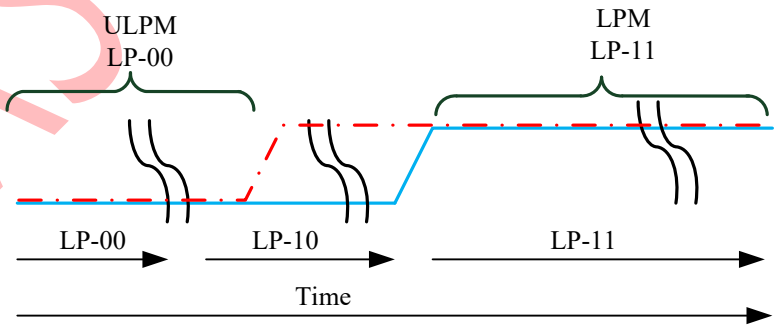

Figure:From ULPM to LPM

After DSI-CLK+/- lanes are leaving High Speed Clock Mode (HSCM, HS-0 or HS-1 State Code) =>HS-0 =>LP-11 (LPM). This sequence is illustrated below.

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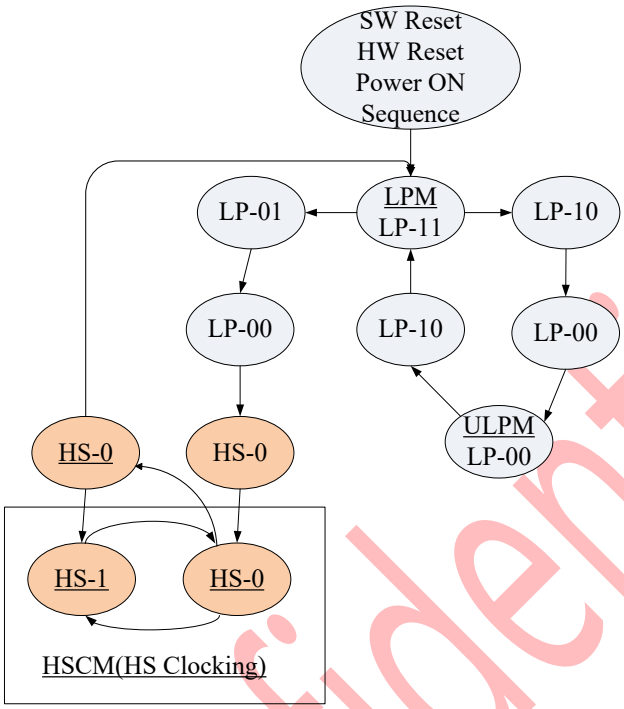

Figure: From HSCM to LPM

All three mode changes are illustrated a flow chart below.

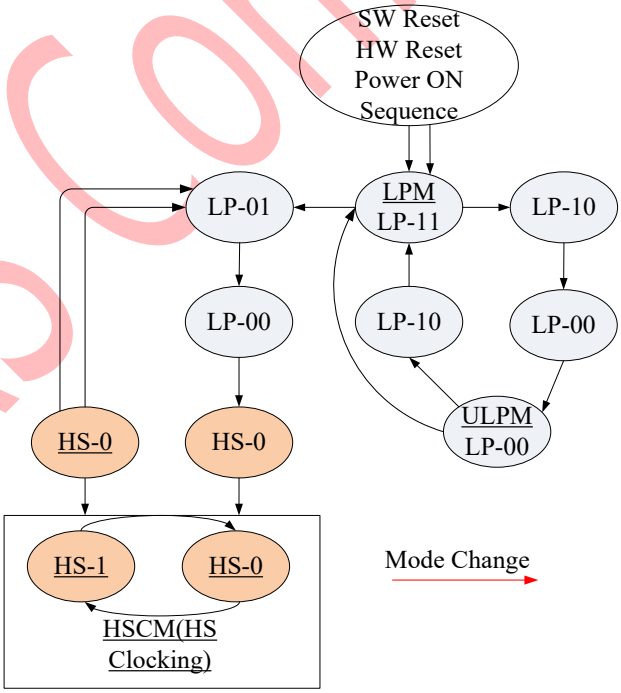

Figure: All three mode changes to LPM

Ultra Low Power Mode (ULPM)

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DSI-CLK+/- lanes can be driven to the High Speed Clock Mode (HSCM), when DSI-CLK lanes are starting to work between HS-0 and HS-1 State Codes.

The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) =>LP-01 =>LP-00 =>HS-0 =>HS-0/1 (HSCM). This sequence is illustrated below.

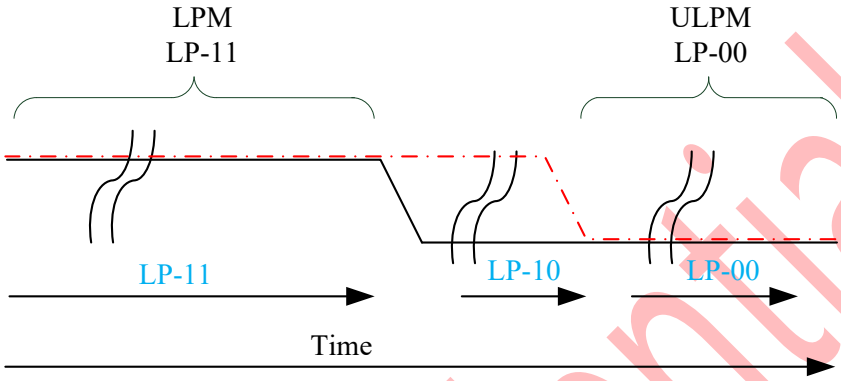

Figure: From LPM to UPLM

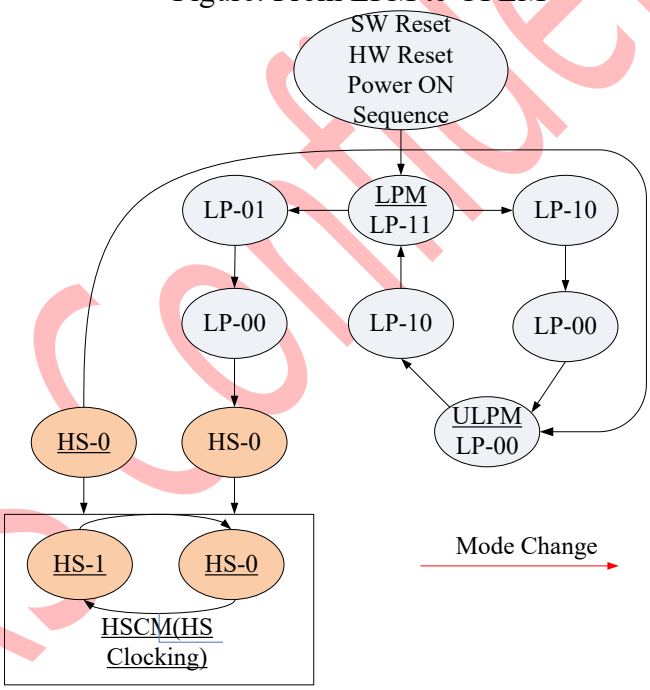

Figure:The mode change from LPM to UPLM

High-speed Clock Mode (HSCM)

DSI-CLK+/- lanes can be driven to the High Speed Clock Mode (HSCM), when DSI-CLK lanes are starting to work between HS-0 and HS-1 State Codes.

The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) =>LP-01 =>LP-00 =>HS-0 =>HS-0/1 (HSCM). This sequence is illustrated below.

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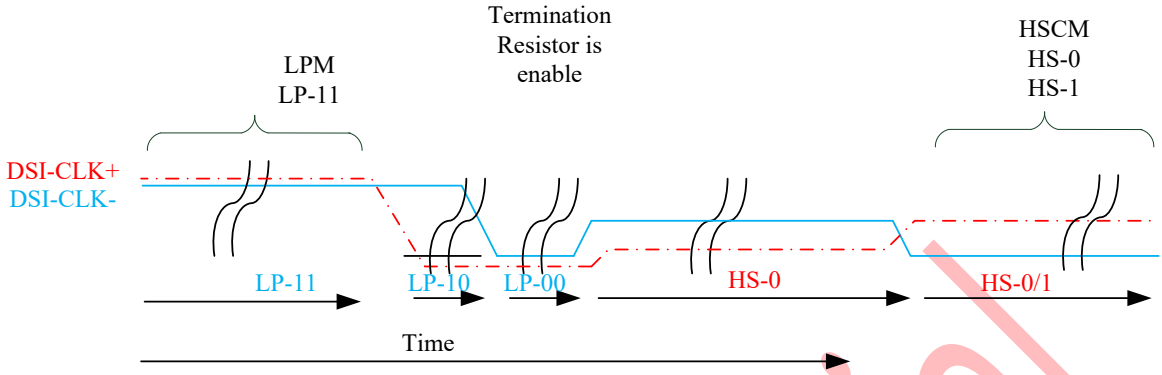

Figure: From LPM to HSCM

The mode change is also illustrated below:

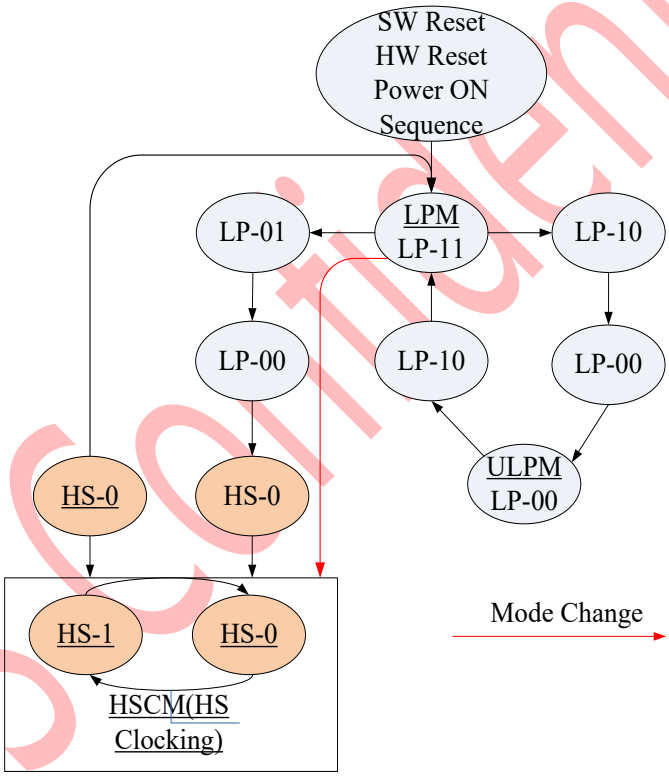

Figure:Mode change from LPM to HSCM

The high speed clock (DSI-CLK+/-) is started before high speed data is sent via DSI-Dn+/- lanes. The high speed clock continues clocking after the high speed data sending has been stopped

The burst of the high speed clock consists of:

– Even the number of transitions
– Start state is HS-0
– End state is HS-0

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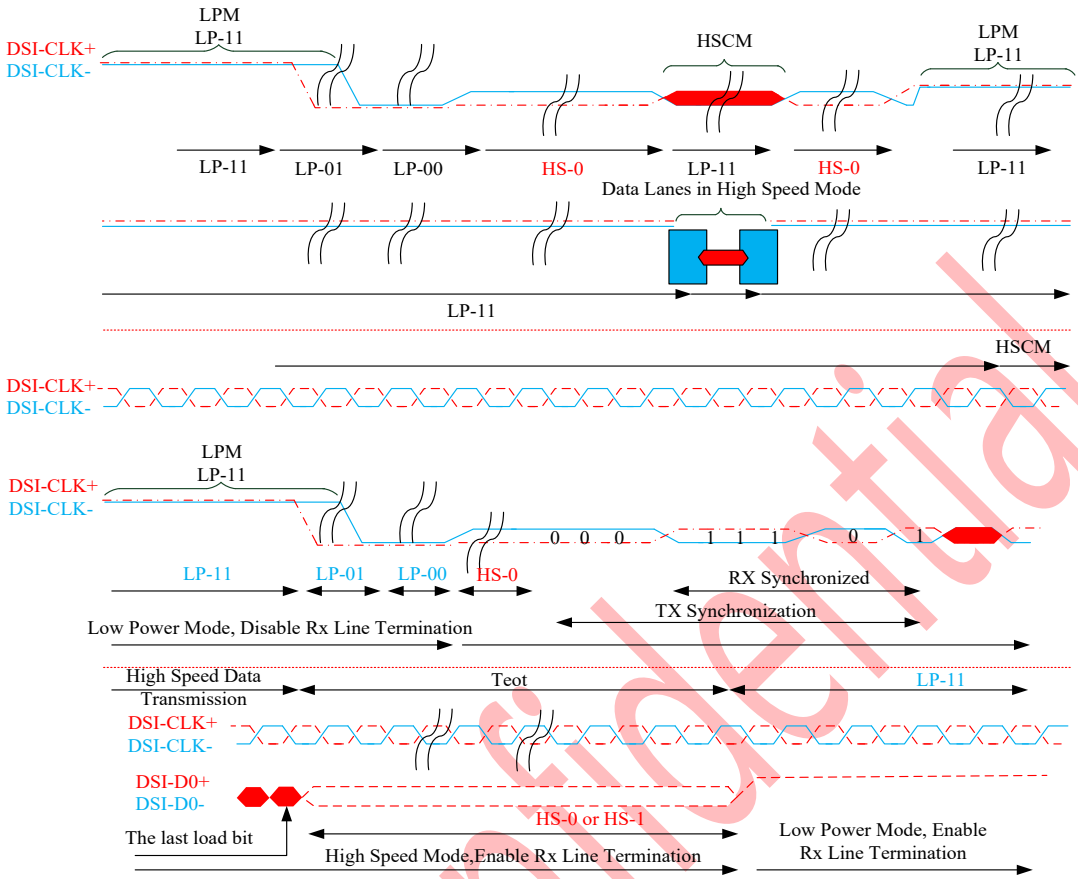

Figure: High speed clock burst

5.2.3. DSI data lanes

5.2.3.1. General

DSI-Dn+/- Data Lanes can be driven in different modes which are:
– Escape Mode (only support DSI_D0 data lane pair)
– High-Speed Data Transmission (support all data lane pairs)
– Bus Turnaround Request (only support DSI_D0 data lane pair)
These modes and their entering codes are defined in the following table.

Mode	Entering Mode Sequence	Leaving Mode Sequence
Escape Mode	LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00	L P-00 =>LP-10 =>LP-11 (Mark-1)
High-Speed Data Transmission	LP-11 =>LP-01 =>LP-00 =>HS-0	(HS-0 or HS-1) =>LP-11
Bus Turnaround Request	LP-11 =>LP-10 =>LP-00 =>LP-10 =>LP-00	High-Z, Note

Table: Entering and leaving sequences

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5.2.3.2. Escape modes

Escape mode is a special mode of operation for Data Lanes using Low-Power states. With this mode, some additional functionality becomes available. Escape mode operation shall be supported in the Forward direction and Reverse direction.

The basic sequence of the Escape Mode is as follows

• Start: LP-11.

• Escape Mode Entry: LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00.

• Escape Command, which is coded, when one of the data lanes is changing from low-to-high-to-low, then this changed data lane is presenting a value of the current data bit.

• A payload stream if it is needed.

• Exit Escape (Mark-1) LP-00 =>LP-10 =>LP-11.

• End: LP-11.

For Data Lane0, once Escape mode is entered, the transmitter shall send an 8-bit entry command to indicate the requested action. All currently available Escape mode commands and actions are listed below.

• Send or receive “Low-Power Data Transmission” (LPDT).

• Driver data lanes to “Ultra-Low Power State” (ULPS).

• Indicate “Remote Application Reset” (RAR), which is resetting the display module (same as S/W Reset function).

• Indicate “Tearing Effect” (TEE), which is used for a TE line event from the display module to the HOST.

• Indicate “Acknowledge” (ACK), which is used for a non-error event from the display module to the HOST.

The Stop state shall be used to exit Escape mode and cannot occur during Escape mode operation because of the Spaced-One-Hot encoding. Stop state immediately returns the Lane to Control mode. If the entry command doesn’t match a supported command, that particular Escape mode action shall be ignored and the receive side waits until the transmit side returns to the Stop state. For Data Lane1 and 2, only support ULPS Escape mode commands.

• Driver data lanes to “Ultra-Low Power State” (ULPS).

The basic construction is illustrated below:

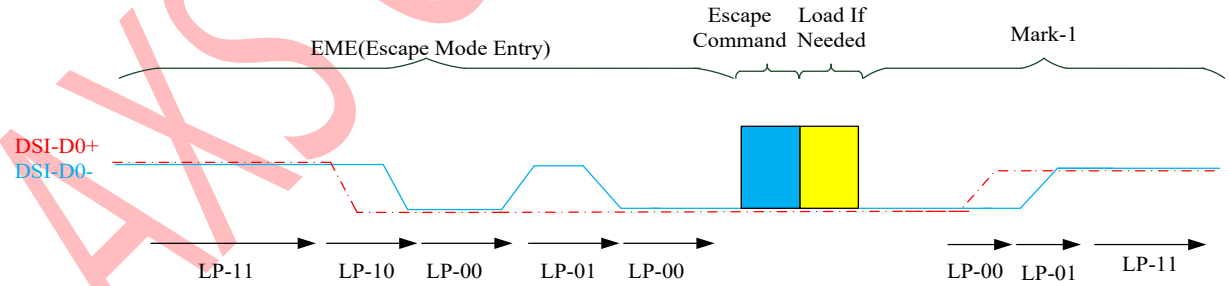

Figure: General Escape mode sequence

The number of the different Escape Commands is eight. These eight different Escape Commands can be divided to 2 different groups: Mode or Trigger. Escape command and groups are defined below.

Escape Command	Command Type	Entry Command Pattern

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	Mode/Trigger	(First Bit => Last Bit Transmitted)
Low-Power Data Transmission	Mode	1110 0001bin
Ultra-Low Power Mode	Mode	0001 1110bin
Remote Application Reset	Trigger	0110 0010 bin
Tearing Effect	Trigger	0101 1101 bin
Acknowledge	Trigger	0010 0001 bin

Table: Escape commands

The HOST is inform the display module that it is controlling data lanes (DSI-D0+/-) with the Mode e.g. The HOST can inform the display module that it can put data lanes in the low power mode.

The HOST is waiting from the display module event information, which has been set by the HOST , with the Trigger e.g. when the display module reaches a new V-synch, the display module sent the HOST a TE trigger (TEE), if the HOST has been requested it.

Low-Power Data Transmission (LPDT)

The HOST can send data to the display module in Low-Power Data Transmission (LPDT) mode when data lanes are entering in Escape Mode and Low-Power Data Transmission (LPDT) command has been sent to the display module. The display module is also using the same sequence when it is sending data to the HOST .

The Low Power Data Transmission (LPDT) is using a following sequence:

• Start: LP-11

• Escape Mode Entry : LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00

• Low-Power Data Transmission (LPDT) command in Escape Mode: 1110 0001 (First to Last bit)

• Payload (Data):

- One or more bytes
- Data lanes are in pause mode when data lanes are stopped (Both lanes are low) between bytes

• Mark-1: LP-00 =>LP-10 =>LP-11

• End: LP-11

This sequence is illustrated for reference purposes below:

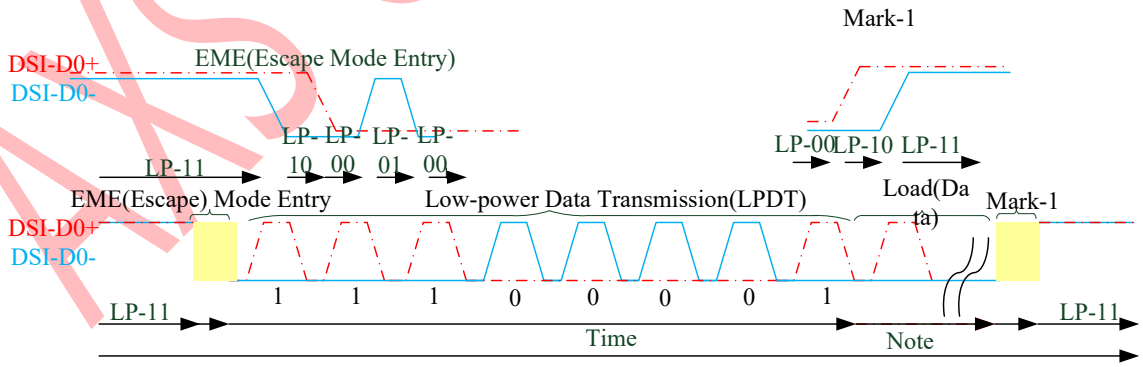

Figure: Low-power data transmission

Note: Load(Data) is presenting the first bit is logical “1” in this example

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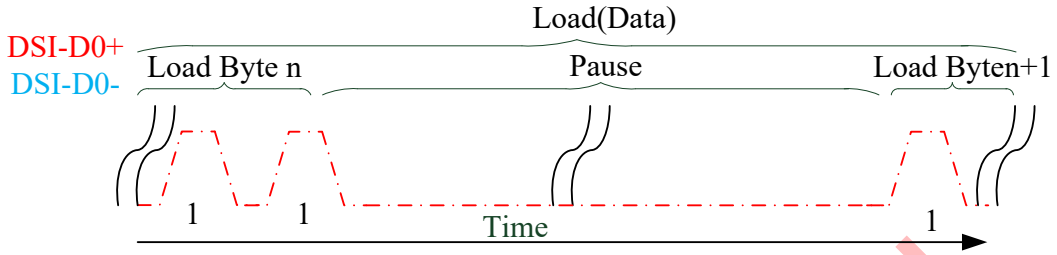

Figure: Pause (example)

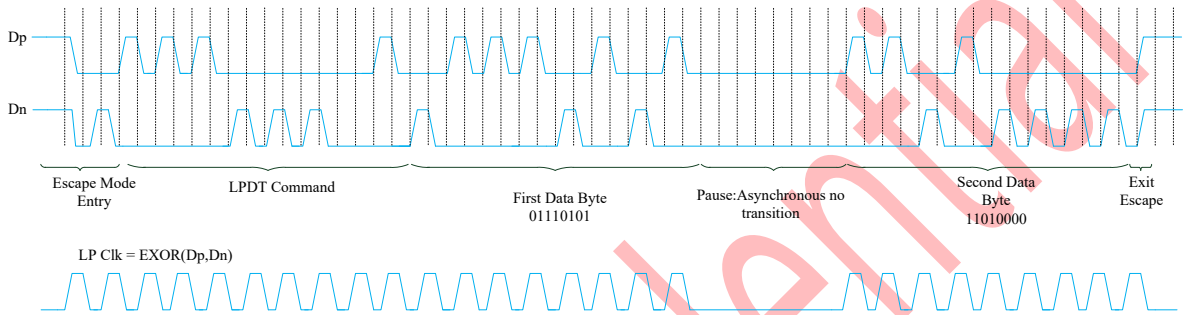

Figure: Two Data Byte Low-Power Data Transmission Example

Ultra-Low Power State (ULPS)

The HOST can force data lanes in Ultra-Low Power State (ULPS) mode when data lanes are entering in Escape Mode.

The Ultra-Low Power State (ULPS)used/uses(?) the following sequence:

- Start: LP-11
- Escape Mode Entry : LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Ultra-Low Power State (ULPS) command in Escape Mode: 0001 1110 (First to Last bit)
- Ultra-Low Power State (ULPS) when the HOST is keeping data lanes low
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

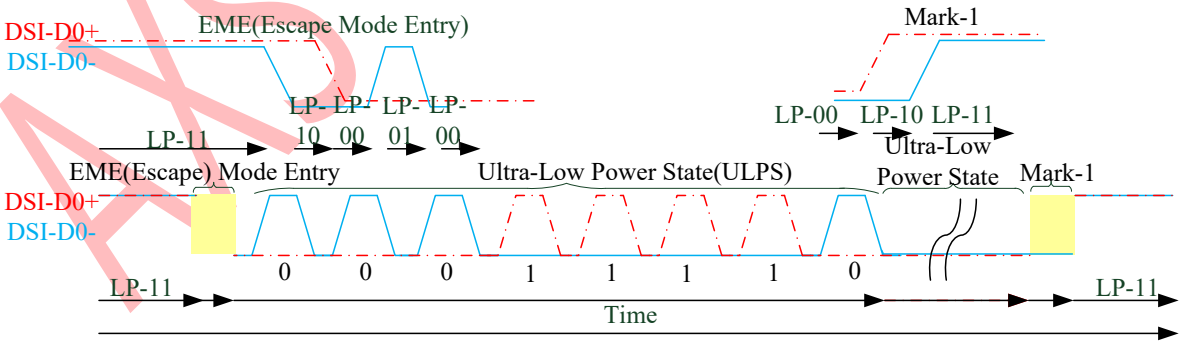

Figure: Ultra-low power state (ULPS)

Remote Application Reset (RAR)

The HOST can inform the display module that it should be reseted in Remote Application Reset (RAR) trigger when data lanes are entering in Escape Mode. The Remote Application Reset using

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the following sequence:

- Start: LP-11
- Escape Mode Entry : LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Remote Application Reset (RAR) command in Escape Mode: 0110 0010 (First to Last bit)
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

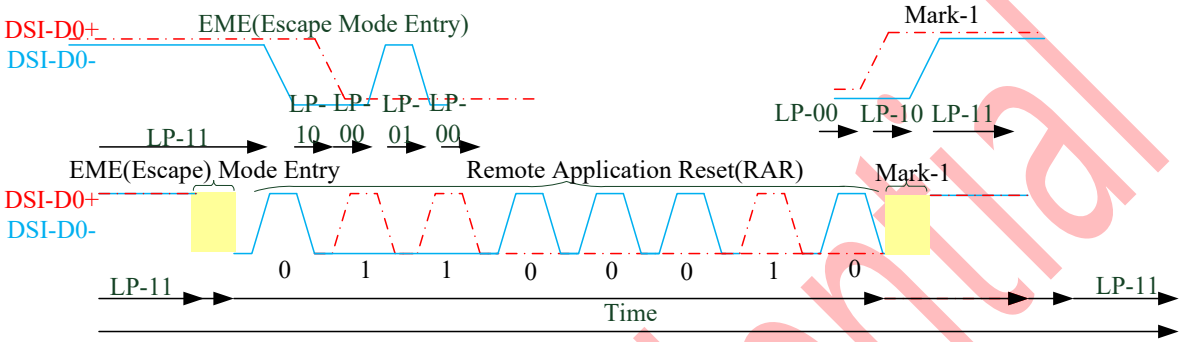

Figure: Remote Application Reset (RAR)

Tearing Effect (TEE)

The display module can inform the HOST when a tearing effect event (New V-synch) has been happen on the display module by Tearing Effect (TEE).

The Tearing Effect (TEE) is using a following sequence:

- Start: LP-11
- Escape Mode Entry: LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Tearing Effect (TEE) trigger in Escape Mode: 0101 1101 (First to Last bit)
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

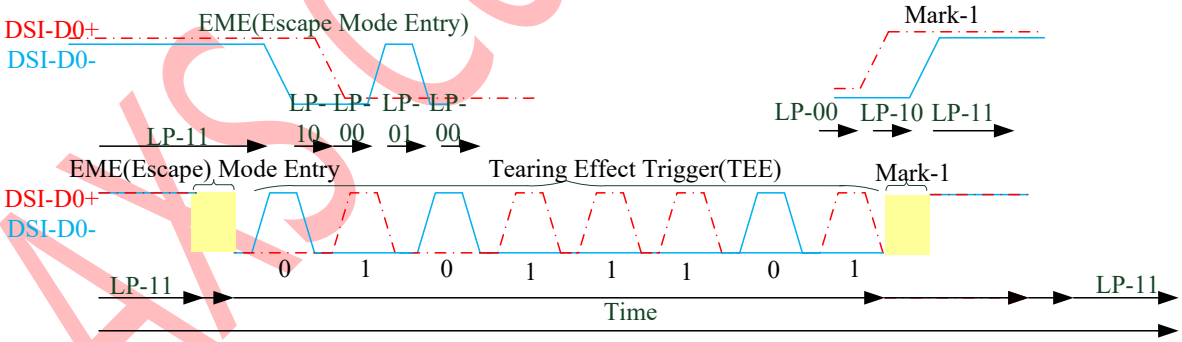

Figure: Tearing effect(TEE)

Acknowledgement (ACK)

The display module can inform the HOST when an error has not recognized on it by Acknowledge (ACK).

The Acknowledge (ACK) used/uses(?) the following sequence:

- Start: LP-11
- Escape Mode Entry: LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Acknowledge (ACK) command in Escape Mode: 0010 0001 (First to Last bit)

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• Mark-1: LP-00 =>LP-10 =>LP-11
• End: LP-11

This sequence is illustrated for reference purposes below:

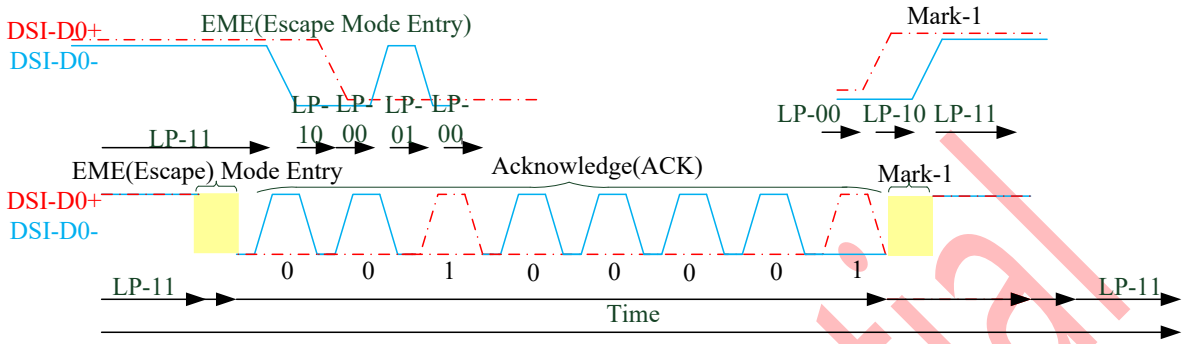

Figure: Acknowledgement (ACK)

5.2.3.3. High-Speed Data Transmission (HSDT)

Entering High-Speed Data Transmission (Tsot of HSDT)

The display module is entering High-Speed Data Transmission (HSDT) when Clock lanes DSI-CLK+/- have already been entered in the HighSpeed Clock Mode (HSCM) by the HOST. See more information on chapter "High-Speed Clock Mode (HSCM)".

Data lanes DSI-D0+/- of the display module are entering (TSOT) in the High-Speed Data Transmission(HSDT) as follow

• Start: LP-11
• HS-Request: LP-01
• HS-Settle: LP-00 => HS-0 (Rx: Lane Termination Enable)
• Rx Synchronization: 011101 (Tx (= HOST) Synchronization: 0001 1101)
• End: High-Speed Data Transmission (HSDT) – Ready to receive High-Speed Data Load

This same entering High-Speed Data Transmission (TSOT of HSDT) sequence is illustrated below.

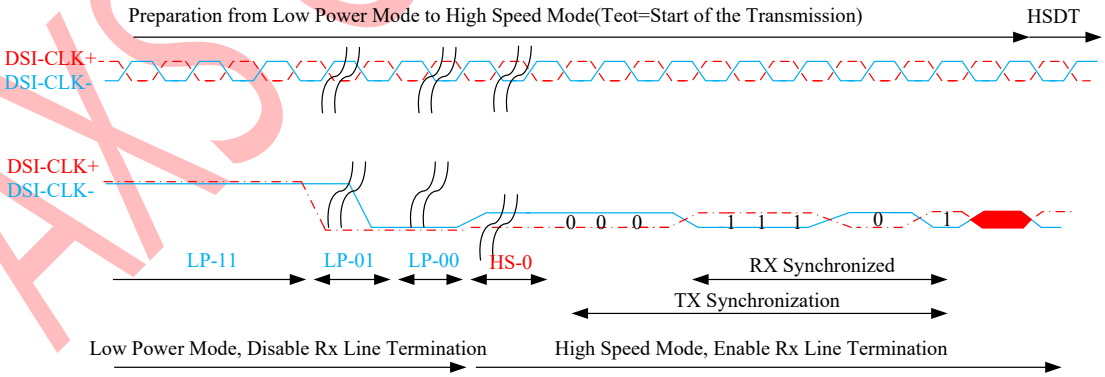

Figure: Tsot of HSDT

Leaving High-Speed Data Transmission (TEOT of HSDT)

The display module is leaving the High-Speed Data Transmission (TEOT of HSDT) when Clock lanes DSI- CLK+/- are in the High-Speed Clock Mode (HSCM) by the HOST and this HSCM is kept until data lanes DSI-D0+/- are in LP-11 mode. See more information on chapter "7.2.2 High-

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Speed Clock Mode (HSCM)". Data lanes DSI-D0+/- of the display module are leaving from the High-Speed Data Transmission (TEOT of HSDT) as follow

- Start: High-Speed Data Transmission (HSDT)
- Stops High-Speed Data Transmission

-HOST changes to HS-1, if the last load bit is HS-0

-HOST changes to HS-0, if the last load bit is HS-1

- End: LP-11 (Rx: Lane Termination Disable)

The same leaving High-Speed Data Transmission (TEOT of HSDT) sequence is illustrated below

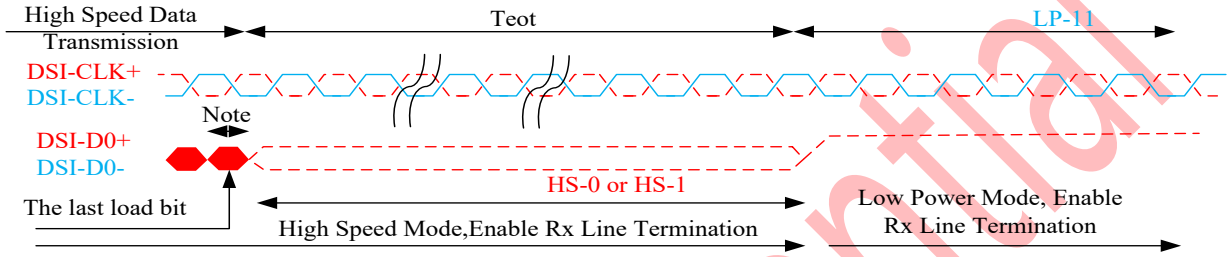

Figure: TEOT of HSDT

Note:

If the last load bit is HS0, the transmitter changes from HS0 to HS-1.

If the last load bit is HS1, the transmitter changes from HS1 to HS-0.

Burst of the High-Speed Data Transmission (HSDT)

The burst of the high-speed data transmission (HSDT) can consist of one data packet or several data packets. These data packets can be Long (LPa) or Short (SPa) packets. These packets are defined on chapter "Short Packet (SPa) and Long Packet (LPa) Structures". These different burst of the High-Speed Data Transmission (HSDT) cases are illustrated for reference purposes below.

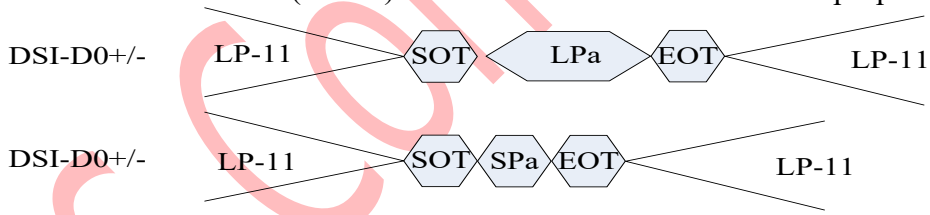

Figure: Single packet in HSDT

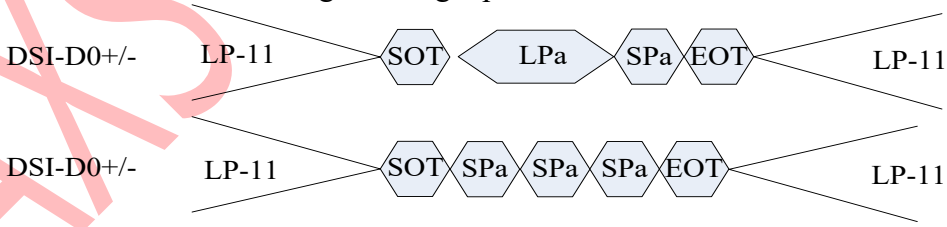

Figure: Multiple packets in HSDT

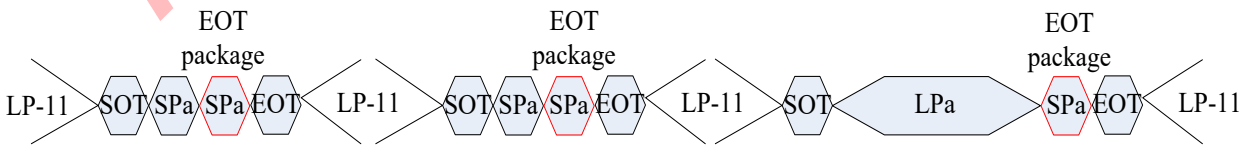

Figure: Packets with EoT package in HSDT

Abbreviation	Explanation

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LP-11	Low Power Mode, Data lanes are '1's (Stop Mode)
SOT	Start of the Transmission
LPa	Long Packet
SPa	Short Packet
EOT	End of the Transmission

Table: Abbreviations

5.2.3.4. Bus Turnaround (BTA)

The HOST or display module, which is controlling DSI-D0+/- Data Lanes, can start a bus turnaround procedure when it wants information to a receiver.

The HOST and display module can use the same sequence when this bus turnaround procedure is used.

This sequence is described for reference purposes, when the HOST wants to do the bus turnaround procedure to the display module, as follows.

• Start (HOST): LP-11

• Turnaround Request (HOST): LP-11 =>LP-10 =>LP-00

• The HOST waits until the display module is starting to control DSI-D0+/- data lanes and the HOST stops to control DSI-D0+/- data lanes (= High-Z)

• The display module changes to the stop mode: LP-00 =>LP-10 =>LP-11

The same bus turnaround procedure (From the HOST to the display module) is illustrated below.

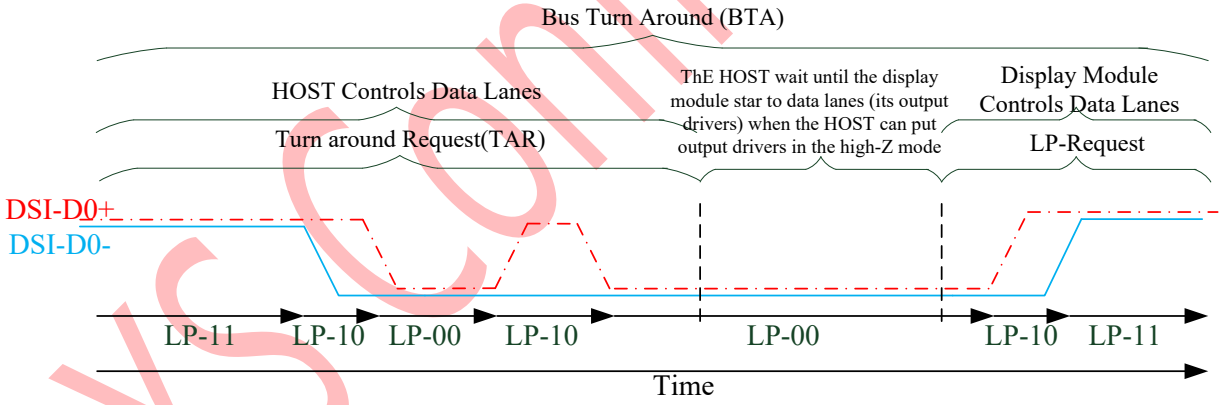

Figure: Bus turnaround procedure

5.2.4. Packet level communication

5.2.4.1. Short Packet (SPa) and Long Packet (LPa) structures

Short Packet (SPa) and Long Packet (LPa) are always used when data transmission is done in Low Power Data Transmission (LPDT) or High-Speed Data Transmission (HSDT) modes.

The lengths of the packets are

- Short Packet (SPa): 4 bytes
- Long Packet (LPa): From 6 to 65,541 bytes

The type (SPa or LPa) of the packet can be recognized from their package headers (PH).

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Data Identifier(DI):
Contains the virtual Channel Identifier and the daTa type information data type denotes the format/content of the application specific payload data used by the application layer.

Package Data:
Length is fixed at two bytes, there are no value restrictions on data words.

8-bit Error Correction Code (ECC)for the packet Header:
8-Bit ECC for the packet header, Allows one-bit errors within the packet header to be corrected and two-bit errors to be detected.

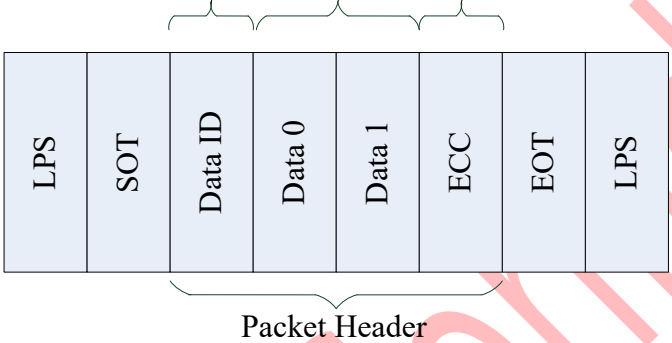

Figure: Short packet structure

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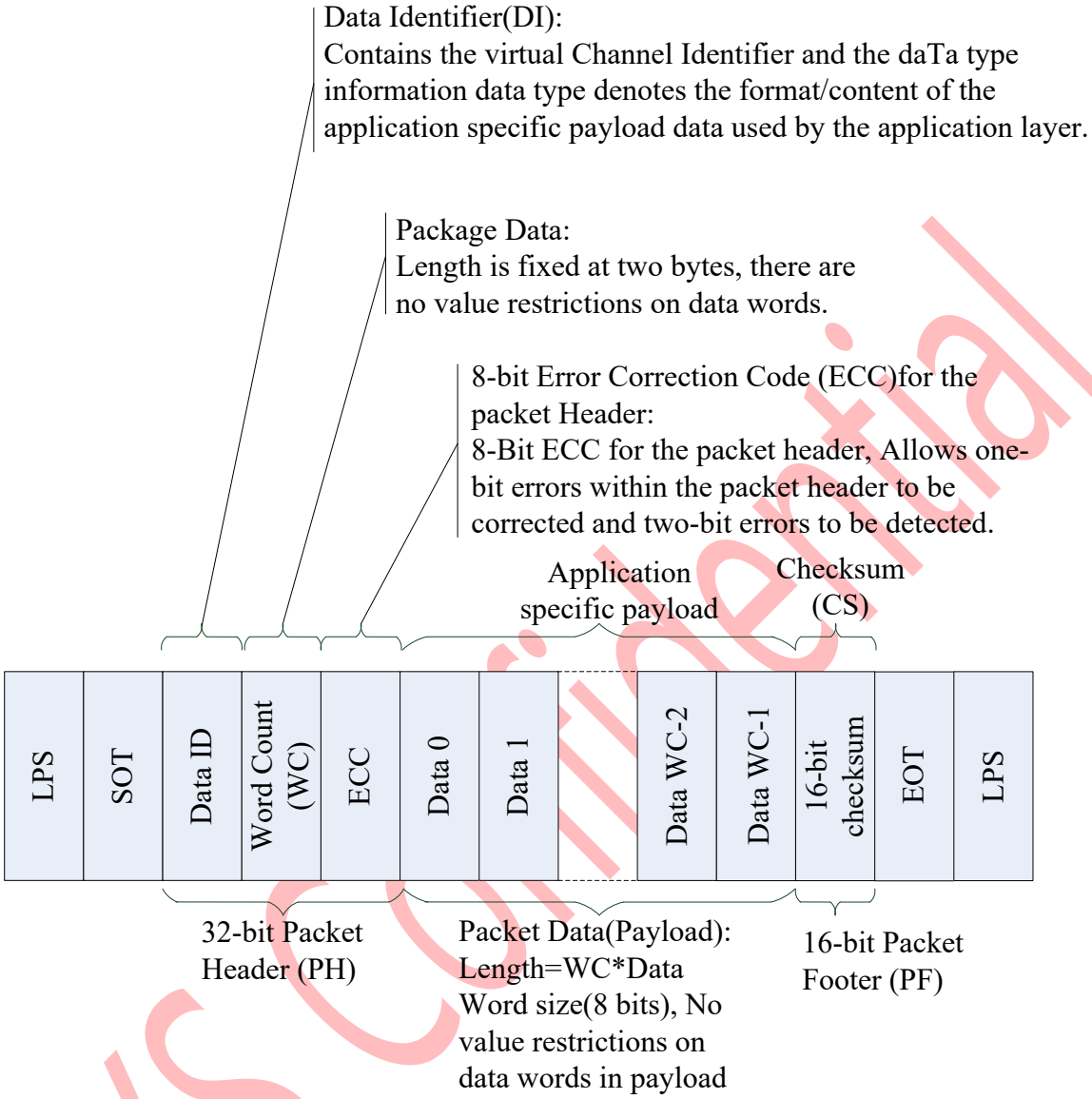

Figure:. Long packet structure

Note: Short Packet (SPa) Structure" and Long Packet (LPa) Structure" are presenting a single packet sending (= Includes LP-11, SoT and EoT for each packet sending).

The other possibility is that there is not needed SoT, EoT and LP-11 between packets if packets have sent in multiple packet format. e.g.:

- LP-11 =>SoT =>SPa =>LPa =>SPa =>SPa =>EoT =>LP-11
- LP-11 =>SoT =>SPa =>SPa =>SPa =>EoT =>LP-11
- LP-11 =>SoT =>LPa =>LPa =>LPa =>EoT =>LP-11

Bit Order of the Byte on Packets

A byte is the smallest transmission unit of a packet. Sequentially, a transmitter shall send data LSB first, MSB last. For packets with multi-byte fields, the least significant byte shall be transmitted first unless otherwise specified. Figure below shows a complete Long packet data transmission. Note, the figure shows the byte values in standard positional notation, i.e. MSB on the left and LSB on the right, while the bits are shown in chronological order with the LSB on the left, the MSB on the right

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and time increasing left to right.

DI								WC(Least Significant Byte)								ECC								Data								CRC(LS Byte)								CRC(MS Byte)							
39hex								01hex								15hex								01hex								0Ehex								1Ehex							
1	0	0	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	1	1	1	1	0	0	0
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Figure: Bit order of the byte on packets

Byte Order of the Multiple Byte Information on Packets

Byte order of the multiple bytes information, what is used on packets, is that the Least Significant (LS) Byte of the information is sent in the first and the Most Significant (MS) Byte of the information is sent in the last. e.g. Word Count (WC) consists of 2 bytes (16 bits) when the LS byte is sent in the first and the MS byte is sent in the last.

This same order is illustrated for reference purposes below.

WC(Least Significant Byte)								WC(Most Significant Byte)							
01hex								00hex							
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12	B13	B14	B15
LSB							MSB	LSB							MSB

Figure: Byte order of the multiple byte information on packets

Packet Head (PH)

The packet header is always consisting of 4 bytes. The content of these 4 bytes are different when it is used to Short Packet (SPa) or Long Packet (LPa).

Short Packet (SPa):

- 1st byte: Data Identification (DI) => Identification that this is Short Packet (SPa)
- 2nd and 3rd bytes: Packet Data (PD), Data 0 and 1
- 4th byte: Error Correction Code (ECC)

DI								Data 0								Data 1								ECC							
15hex								3Ahex								07hex								18hex							
1	0	1	0	1	0	0	0	0	1	0	1	1	1	0	0	1	1	1	0	0	0	0	0	0	0	0	1	1	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12	B13	B14	B15	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Figure: Packet head on short packet

Long Packet (LPa):

- 1st byte: Data Identification (DI) => Identification that this is Long Packet (LPa)

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- 2nd and 3rd bytes: Word Count (WC)
- 4th byte: Error Correction Code (ECC)

DI								WC(Least Significant Byte)								WC(Most Significant Byte)								ECC							
39hex								01hex								00hex								15hex							
1	0	0	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12	B13	B14	B15	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Figure: Packet head on long packet

Data Identification

Data Identification (DI) is a part of Packet Header (PH) and it consists of 2 parts:

- Virtual Channel (VC), 2 bits, DI[7...6]
- Data Type (DT), 6 bits, DI[5…0]

The Data Identification (DI) structure is illustrated on a table below.

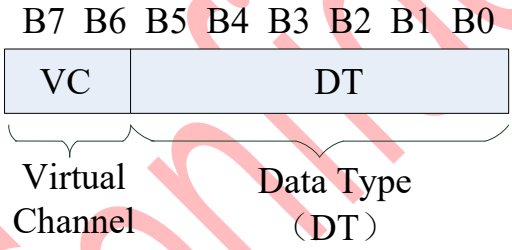

Table: Data identification structure

Data Identification (DI) is illustrated on Packet Header (PH) for reference purposes below.

DI								WC(Least Significant Byte)								WC(Most Significant Byte)								ECC							
39hex								01hex								00hex								15hex							
1	0	0	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12	B13	B14	B15	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Figure: Data identification of the packet head

Virtual Channel (VC)

A processor may service up to four peripherals with tagged commands or blocks of data, using the Virtual Channel ID field of the header for packets targeted at different peripherals.

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Virtual Channel (VC) is a part of Data Identification (DI[7…6]) structure and it is used to address where a packet is wanted to send from the MCU. Bits of the Virtual Channel (VC) are illustrated for reference purposes below.

AXS15231E only support VC code=00, package with other VC code(01/10/11) will be filter out.

DI								WC(Least Significant Byte)								WC(Most Significant Byte)								ECC							
39hex								01hex								00hex								15hex							
1	0	0	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12	B13	B14	B15	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Figure: Virtual channel on the packet head

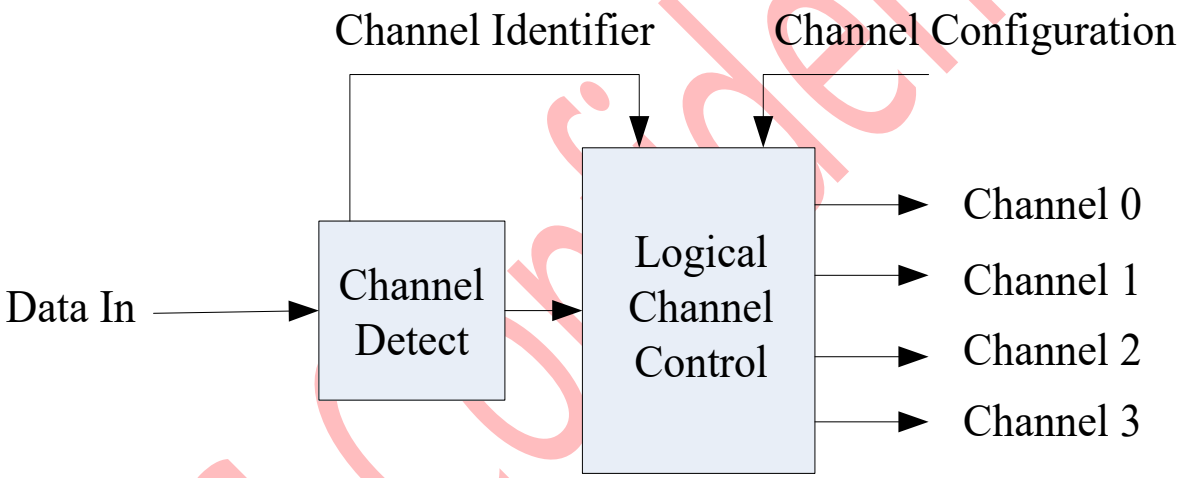

Figure: Virtual channel block diagram (receiver case)

Data Type (DT)

Data Type (DT) is a part of Data Identification (DI[5…0]) structure and it is used to define a type of the used data on a packet.

Bits of the Data Type (DT) are illustrated for reference purposes below.

DI								WC(Least Significant Byte)								WC(Most Significant Byte)								ECC							
39hex								01hex								00hex								15hex							
1	0	0	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12	B13	B14	B15	B0	B1	B2	B3	B4	B5	B6	B7
LS							MS	LS							MS	LS							MSB	LS							MS

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B		B	B		B	B			B		B

Figure: Data type on the packet head

This Data Type (DT) also defines what the used packet is: Short Packet (SPa) or Long Packet (LPa). Data Types (DT) are different from the MCU to the display module (or other devices) and vice versa. These Data Type (DT) are defined on tables below.

From the MCU to the Display module		
Data Type(HEX)	Data Type(Binary)	Description
01h	00 0001	Sync Event, V Sync Start
11h	01 0001	Sync Event, V Sync End
21h	10 0001	Sync Event, H Sync Start
31h	11 0001	Sync Event, H Sync End
08h	00 1000	End of Transmission (EoT)packet
03h	00 0011	Generic Short WRITE, no parameters
13h	01 0011	Generic Short WRITE, 1 parameters
23h	10 0011	Generic Short WRITE, 2 parameters
04h	00 0100	Generic READ, no parameters
14h	01 0100	Generic READ, 1 parameters
24h	10 0100	Generic READ, 2 parameters
05h	00 0101	DCS WRITE, no parameters
15h	01 0101	DCS WRITE, 1 parameters
06h	00 0110	DCS READ, no parameters
37h	11 0111	Set Maximum Return Packet Size
09h	00 1001	Null Packet, no data
19h	01 1001	Blanking Packet, no data
29h	10 1001	Generic Long Write
39h	11 1001	DCS Long Write/Write_LUT Command packet
3Eh	11 1110	Packet Pixel Streem, 24-bit RGB, 8-8-8 Format
0Eh	001110	Packed Pixel Stream,16-bit RGB,5-6-5 Format
1Eh	011110	Packed Pixel Stream,18-bit RGB,6-6-6 Format
2Eh	101110	Loosely Packed Pixel Stream,18-bit RGB,6-6-6 Format

Table: Data type from the MCU to the display module

From the Display module to the MCU		
Data Type(HEX)	Data Type(Binary)	Description

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1Ch	01 1100	DCS Long Read Response
21h	10 0001	DCS Short Read Response, 1 Byte returned
22h	10 0010	DCS Short Read Response, 2 Byte returned
1Ah	011010	Genaric Long READ Response
11h	01 0001	Generic Short Read Response, 1 Byte returned
12h	01 0010	Generic Short Read Response, 2 Byte returned

Table: Data type from the display module to the MCU

The receiver will ignore other Data Type (DT) if they are not defined on tables above. Host send "Generic Read" data type, AXS15231E will return Generic Read package to Host.

Packet data on the short packet

Packet Data (PD) of the Short Packet (SPa) is defined after Data Type (DT) of the Data Identification (DI) has indicated that Short Packet (SPa) is wanted to send. Packet Data (PD) of the Short Packet (SPa) consists of 2 data bytes: Data 0 and Data 1. Packet Data (PD) sending order is that Data 0 is sent in the first and the Data 1 is sent in the last. Bits of Data 1 are set to 00h, if the information length is 1 byte. Packet Data (PD) of the Short Packet (SPa), when the length of the information is 1 or 2 bytes are illustrated for reference purposes below.

DI								Data 0								Data 1								ECC							
15hex								35hex								01hex								1Ehex							
1	0	1	0	1	0	0	0	1	0	1	0	1	1	0	0	1	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12	B13	B14	B15	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Figure: Packet data on the short packet, 2 bytes information

Packet Data (PD) information:

- Data 0: 10hex
- Data 1: 00hex (Null)

DI								Data 0								Data 1								ECC							
05hex								10hex								00hex								2Chex							
1	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12	B13	B14	B15	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Figure: Packet data on the short packet, 1 bytes information

Word count on the long packet

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Word Count (WC) of the Long Packet (LPa) is defined after Data Type (DT) of the Data Identification (DI)has indicated that Long Packet (LPa) is wanted to send. Word Count (WC) indicates a number of the data bytes of the Packet Data (PD) what is wanted to send after Packet Header (PH) versus Packet Data (PD) of the Short Packet (SPa) is placed in the Packet Header (PH). Word Count (WC) of the Long Packet (LPa) consists of 2 bytes.

These 2 bytes of the Word Count (WC) sending order is that the Least Significant (LS) Byte is sent in the first and the Most Significant (MS) Byte is sent in the last.

Word Count (WC) of the Long Packet (LPa) is illustrated for reference purposes below.

DI								WC(Least Significant Byte)								WC(Most Significant Byte)								ECC							
39hex								01hex								00hex								15hex							
1	0	0	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12	B13	B14	B15	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Figure: Word count on the long packet

Error Correction Code (ECC)

Error Correction Code (ECC) is a part of Packet Header (PH) and its purpose is to identify an error or errors:

- Short Packet (SPa): Data Identification (DI) and Packet Data (PD) bytes (24 bits: D[23…0])
- Long Packet (LPa): Data Identification (DI) and Word Count (WC) bytes (24 bits: D[23…0])

D[23…0] is illustrated for reference purposes below.

DI								Data 0								Data 1								ECC							
05hex								10hex								00hex								2Chex							
1	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0
D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D16	D17	D18	D19	D20	D21	D22	D23	P0	P1	P2	P3	P4	P5	P6	P7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Figure: D[23:0] and P[7:0] on the short packet

DI								WC(Least Significant Byte)								WC(Most Significant Byte)								ECC							
39hex								01hex								00hex								15hex							
1	0	0	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0
D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D1	D1	D1	D1	D1	D1	D1	D1	D1	D1	D2	D2	D2	D2	P0	P1	P2	P3	P4	P5	P6	P7

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										0	1	2	3	4	5	6	7	8	9	0	1	2	3								
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Figure: D[23:0] and P[7:0] on the long packet

Error Correction Code (ECC) can recognize one error or several errors and makes correction in one bit error case.

Bits (P[7…0]) of the Error Correction Code (ECC) are defined, where the symbol '^' is presenting XOR function (Pn is '1' if there is odd number of '1's and Pn is '0' if there is even number of '1's), as follows.

ecc_parity = {P7,P6,P5,P4,P3,P2,P1,P0};

- P7 = 0
- P6 = 0
- P5 = D10^D11^D12^D13^D14^D15^D16^D17^D18^D19^D21^D22^D23
- P4 = D4^D5^D6^D7^D8^D9^D16^D17^D18^D19^D20^D22^D23
- P3 = D1^D2^D3^D7^D8^D9^D13^D14^D15^D19^D20^D21^D23
- P2 = D0^D2^D3^D5^D6^D9^D11^D12^D15^D18^D20^D21^D22
- P1 = D0^D1^D3^D4^D6^D8^D10^D12^D14^D17^D20^D21^D22^D23
- P0 = D0^D1^D2^D4^D5^D7^D10^D11^D13^D16^D20^D21^D22^D23

P7 and P6 are set to '0' because Error Correction Code (ECC) is based on 64 bit value ([D63…0]), but this implementation is based on 24 bit value (D[23…0]). Therefore, there is only needed 6 bits (P[5…0]) for Error Correction Code (ECC).

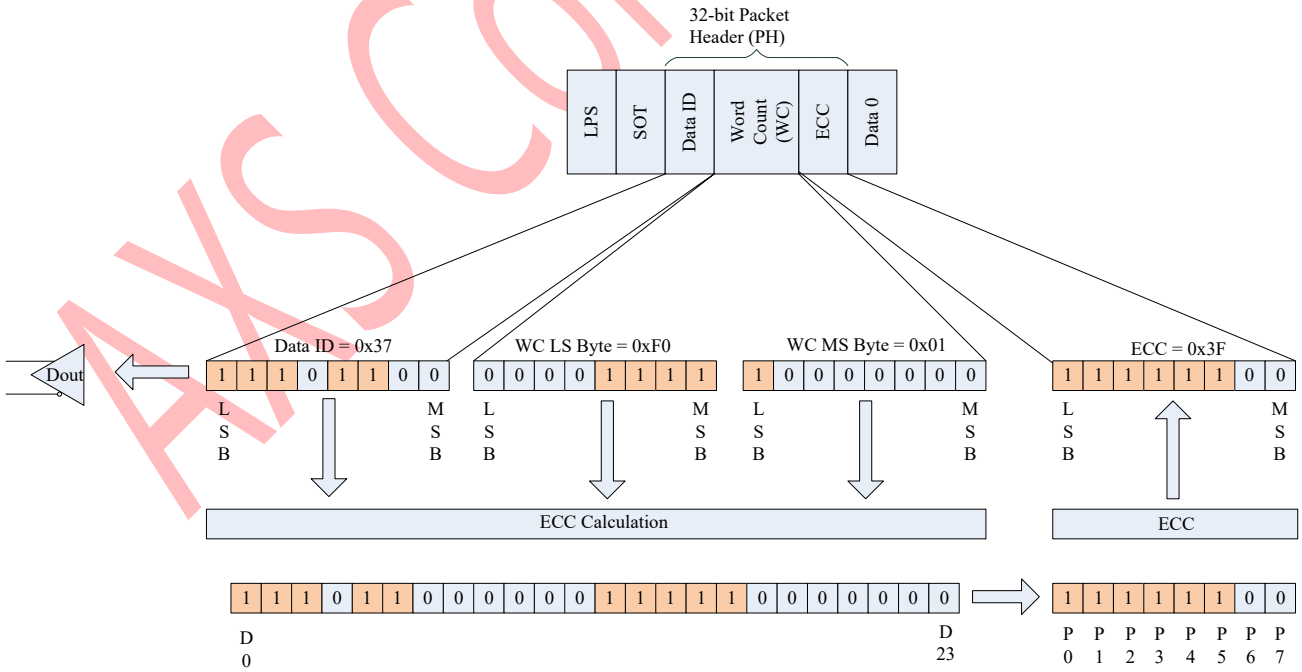

Figure: 24-bit ECC generation on TX side (Example)

Packet footer on the long packet

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Packet Footer (PF) of the Long Packet (LPa) is defined after the Packet Data (PD) of the Long Packet (LPa). The Packet Footer (PF) is a checksum value what is calculated from the Packet Data of the Long Packet (LPa).

The checksum is using a 16-bit Cyclic Redundancy Check (CRC) value which is generated with a polynomial X16+X12+X5+X0 as it is illustrated below.

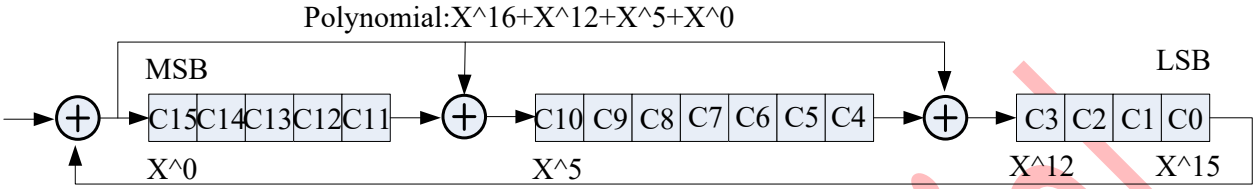

Figure: 16-bit cyclic redundancy check (CRC) calculation

The 16-bit Cyclic Redundancy Check (CRC) generator is initialized to FFFFh before calculations. The Most Significant Bit (MSB) of the data byte of the Packet Data (PD) is the first bit what is inputted into the 16-bit Cyclic Redundancy Check (CRC). The receiver is calculated own checksum value from received Packet Data (PD). The receiver compares own checksum and the Packet Footer (PF) what the transmitter has sent. The received Packet Data (PD) and Packet Footer (PF) are correct if the own checksum of the receiver and Packet Footer (PF) are equal and vice versa the received Packet Data (PD) and Packet Footer (PF) are not correct if the own checksum of the receiver and Packet Footer (PF) are not equal.

5.2.4.2. Packet transmissions

Packet from the MCU to the display module

Display Command Set (DCS), which is defined on chapter “Instructions” is used from the MCU to the display module. This Display Command Set (DCS) is always defined on the Data 0 of the Packet Data (PD), which is included in Short Packet (SPa) and Long packet (LPa) as these are illustrated below.

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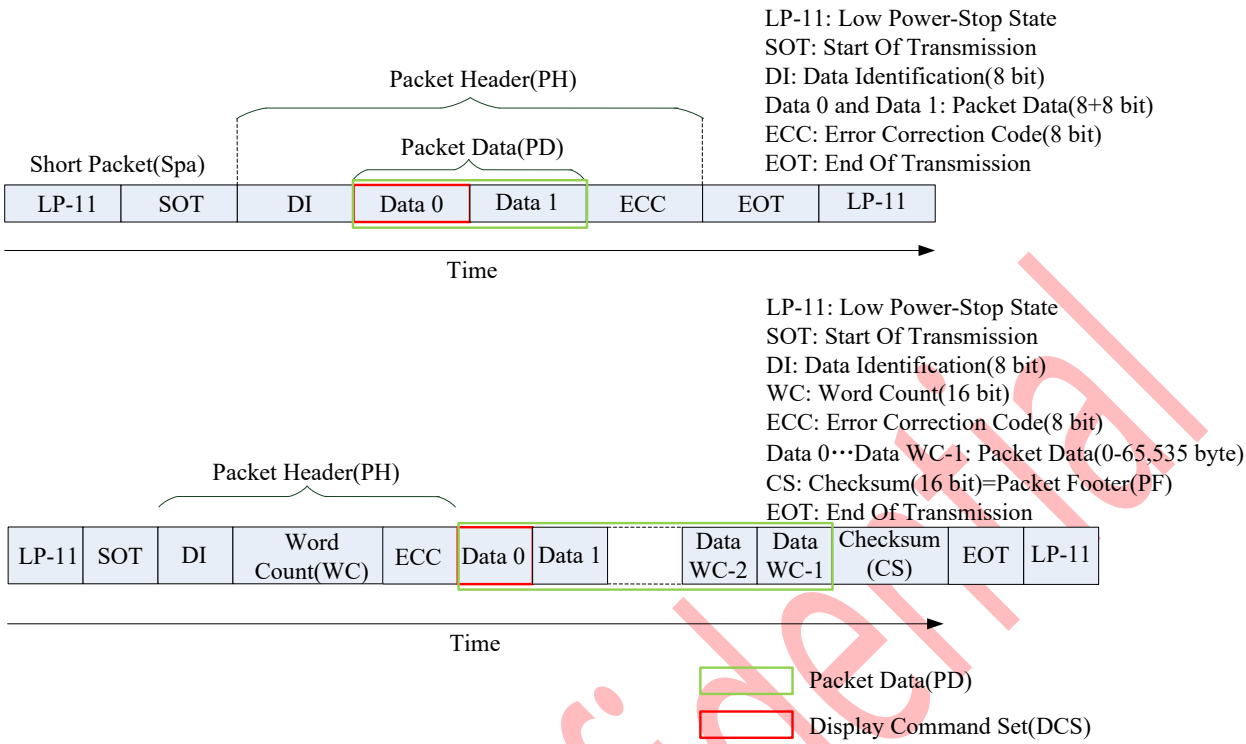

Figure: DCS on the short packet and long packet

Packet from the display module to the MCU
Used packet types

The display module is always using Short Packet (SPa) or Long Packet (LPa), when it is returning information to the MCU after the MCU has requested information from the Display Module. This information can be a response of the Display Command Set (DCS).

The used packet type is defined on Data Type (DT).

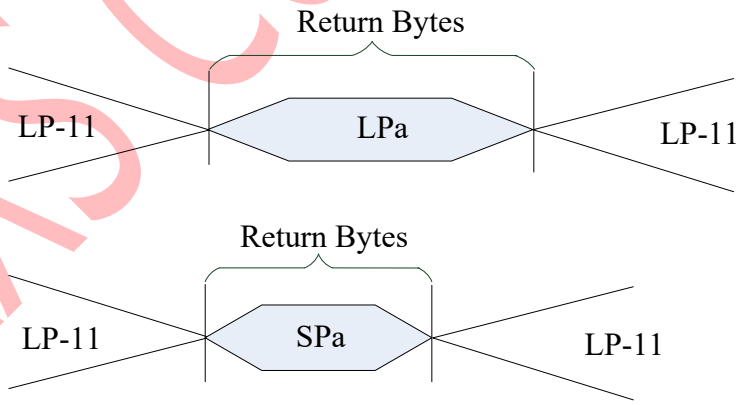

Figure: Return bytes on single packet

5.2.5. Customer-defined generic read data type format

The short packet of Data Type 14h (Generic READ, 1 parameters) specifies the register content for read and the Nth parameter that will begin reading. After Data Type 14h is received, BTA is

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executed. Then, the Nth parameter becomes the first data, and the number of data of WC (word count) value is output.

Packet Structure(processor → peripheral)

		P 0	P 1		
	Data Type 24h	Manufacturer Command	Start Parameter N	ECC	

Low Power Data Transfer(peripheral → processor)

					Data 0	Data 1		Data WC-1			
	Data Type 1Ah	WC 0	WC 1	WC 2	1th Parameter	2th Parameter		Nth Parameter	CRC 0	CRC 1	

Figure: Generic read data type format

5.2.6. MIPI video parameter

In the MIPI video mode, the frame is transmitted from the host processor to a display module as a sequence of pixels, with each horizontal line of the image data sent as a group of consecutive pixels.

Vsync (VS) indicates the beginning of each frame of the displayed image.

Hsync (HS) signals the beginning of each horizontal line of pixels.

Each pixel value (16-, 18-, or 24-bit data) is transferred from the host processor to the display module during one pixel period. The rising edge of PCLK is used by the display module to capture pixel data. Since PCLK runs continuously, control signal DE is required to indicate when valid pixel data is being transmitted on the pixel data signals.

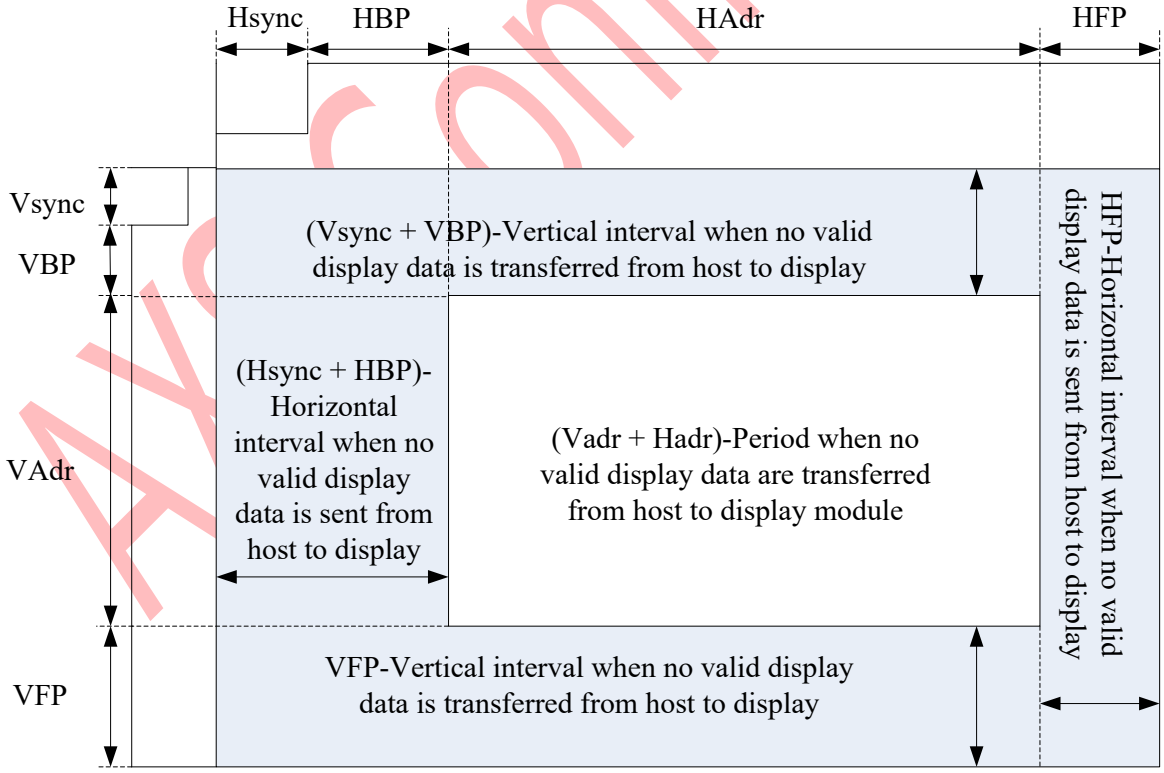

Figure:Define timing parameter for MIPI video operation

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(Resolution for 320 horizontal x 480 vertical display with Frame-Rate of 60 Hz)

Parameters	Symbols	Min.	Typ	Max.	Unit
Horizontal Synchronization	Hsync	2	2	-	PCLK
Horizontal Back Porch	HBP	2	60	-	PCLK
Horizontal Front Porch	HFP	2	60	-	PCLK
Hsync+ HBP+ HFP	-	6	122	-	PCLK
Horizontal Address (Display area)	HAdr	-	320	-	PCLK

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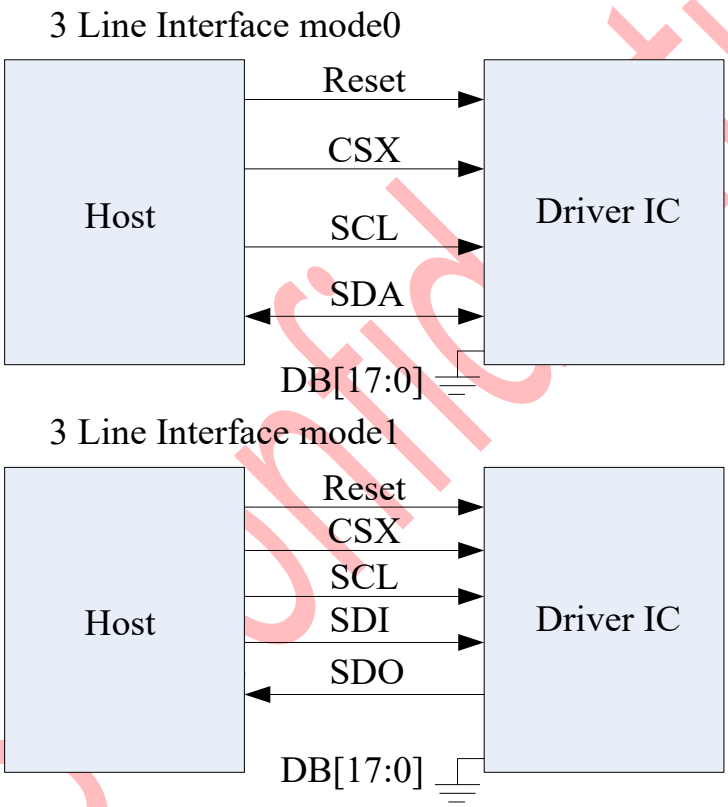
5.3. Serial Interface (SPI)

5.3.1. 3-Line Interface

The Serial Peripheral Interface (SPI) is selected by setting the IM[3:0] pins as “0011” level. The chip select pin (CSX), the serial transfer clock pin (SCL), the serial data input /output pin (SDA or SDI/SDO) are used in SPI mode. The ID pin sets the least significant bit of the identification code. The DB[17:0] pins, which are not used, must be tied to GND



5.3.1.1. Write Sequence.

In the write mode of 3-line serial interface contains a D/CX (data/command) select bit and a transmission byte. If the D/CX bit is “0”, the transmission byte is interpreted as a command byte. If the D/CX bit is “1”, the transmission byte is display data, or stored in the command register as parameter data.

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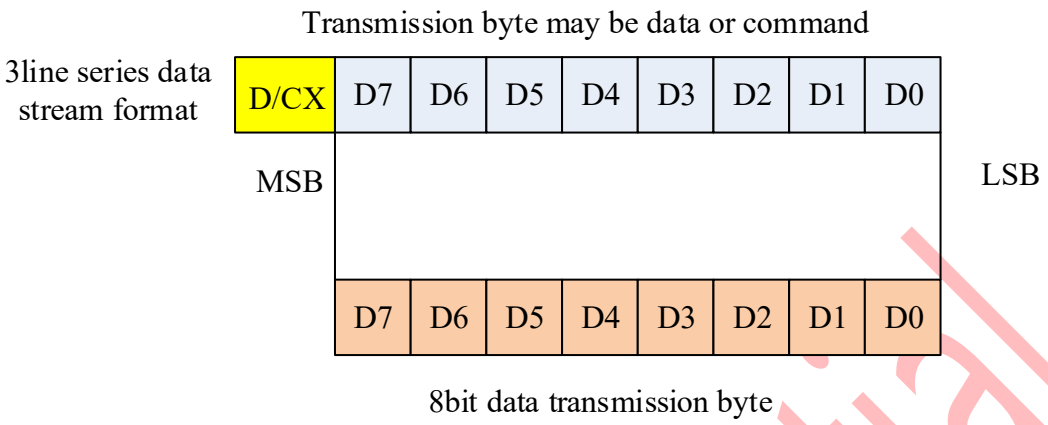
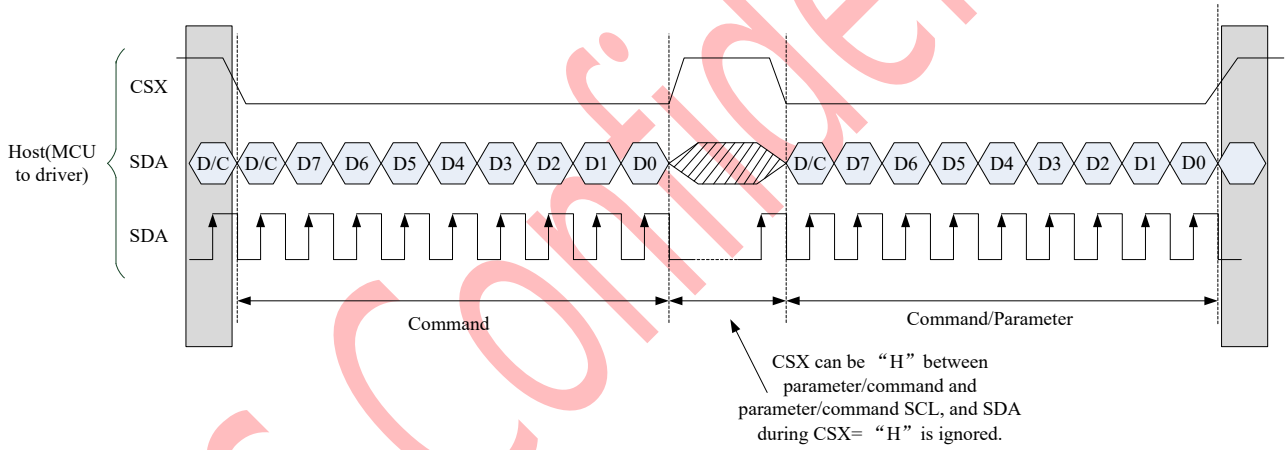


The instruction of AXS15231E can be sent in any order, and the MSB is transmitted first. The 3-line serial interface is initialized when the CSX keeps high level. In this state, the SCL clock pulse and SDA data have no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission.



5.3.1.2. Read Sequence

In the read mode of the interface, the host reads the register value from the AXS15231E. The host sends out a command (Read ID or register command), then a byte is (bytes are) transmitted in the opposite direction. The AXS15231E samples the SDA (input data) at the rising edges of the SCL (serial clock), and shifts to SDO (output data) at the falling edges of the SCL (serial clock). The read mode has three types of transmitted command data (8-/24-/32-bit) according to the command code.

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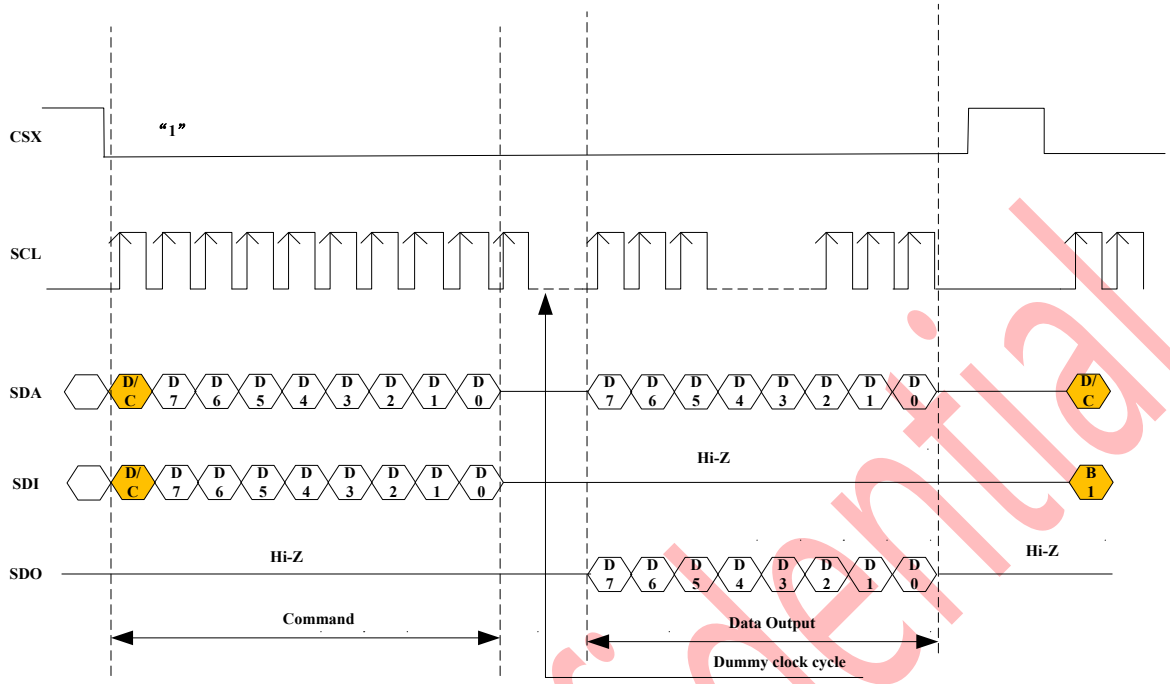
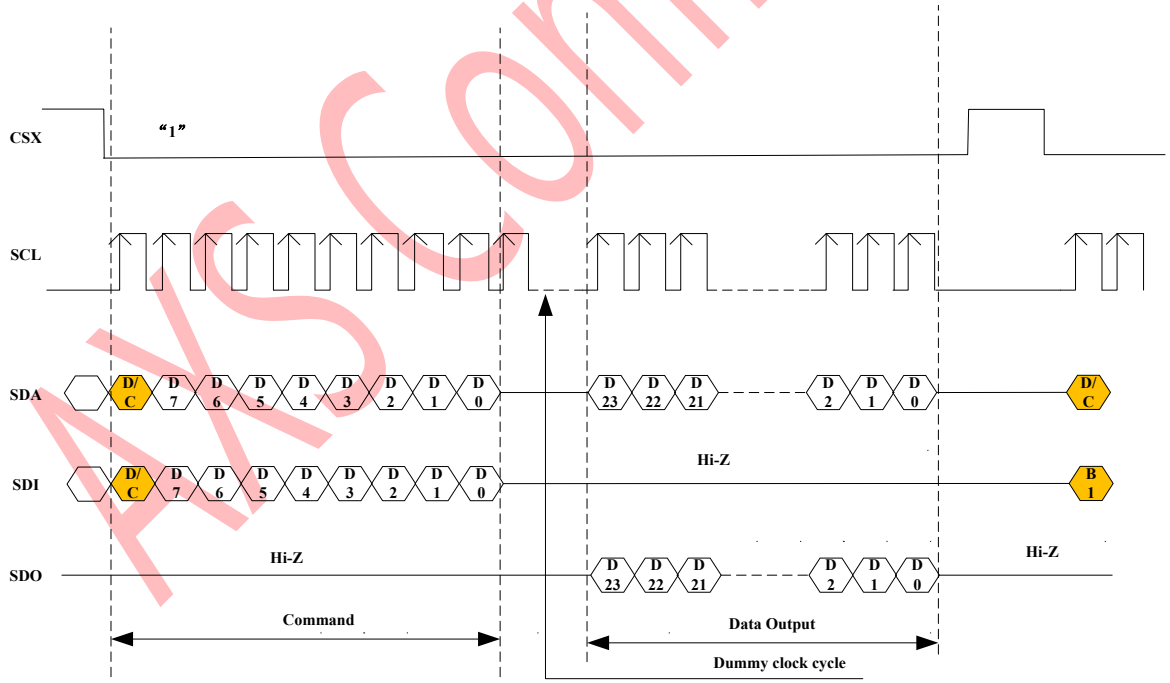
5.3.1.2.1. 3-line serial protocol (for RDDST command: 8-bit read, cr_spi_rd_en=1)



5.3.1.2.2. 3-line serial protocol (for RDDST command: 24-bit read, cr_spi_rd_en=1)



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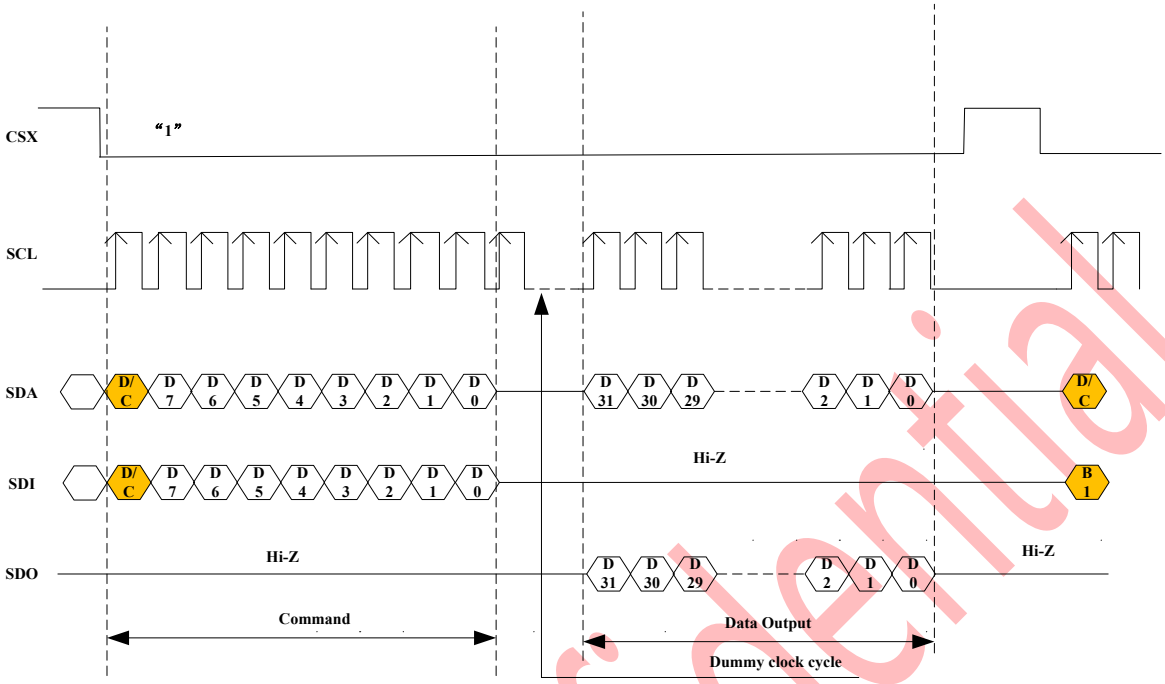
5.3.1.2.3. 3-line serial protocol (for RDDST command: 32-bit read, cr_spi_rd_en=1)



5.3.1.3. 3-SPI Color format

Different display data formats are available for three colors depth supported by the LCM listed below. :

65k colors, RGB 5-6-5-bit input
262k colors, RGB 6-6-6-bit input
16.7M colors, RGB 8-8-8-bit input

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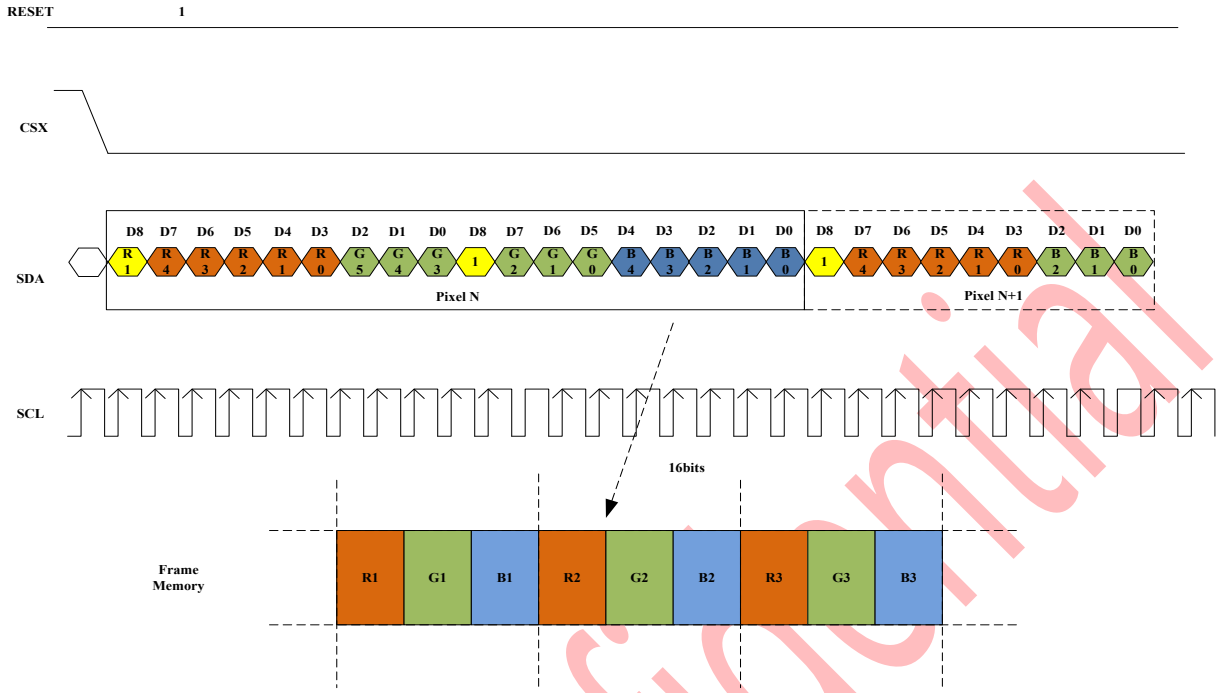
5.3.1.3.1. Write data for 16-bit/pixel (RGB 5-6-5-bit input), 65K-Colors, cr_spi_format=0



5.3.1.3.2. Write data for 18-bit/pixel (RGB 6-6-6L-bit input), 262K-Colors, cr_spi_format=1

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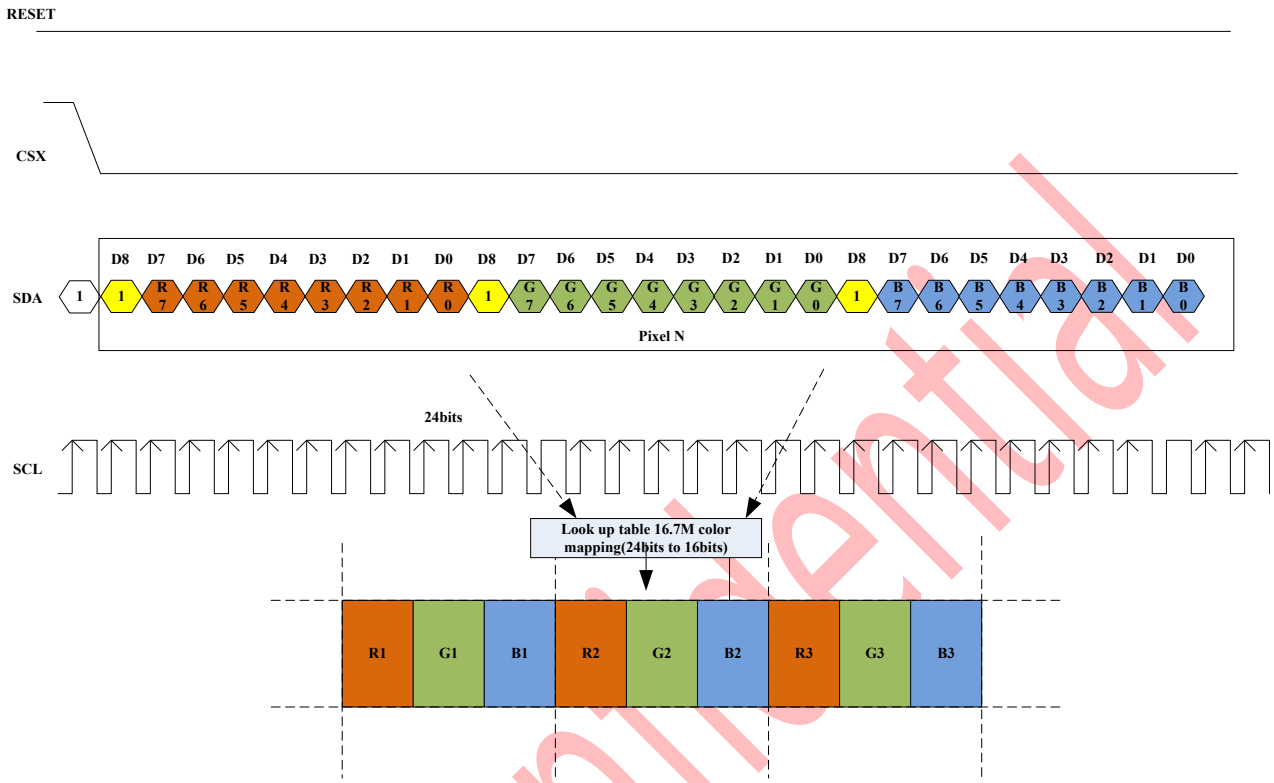
5.3.1.3.3. Write data for 24-bit/pixel (RGB 8-8-8-bit input), 16.7M-Colors, cr_spi_format=1



5.3.2. 4-Line Interface

The Serial Peripheral Interface (SPI) is selected by setting the IM[3:0] pins as “0010” level. The chip select pin (CSX), the serial transfer clock pin (SCL), the display data/command selection (D/CX), the serial data input/output pin (SDA or SDI/SDO) are used in SPI mode. The ID pin sets the least significant bit of the identification code. The DB[17:0] pins, which are not used, must be tied to GND

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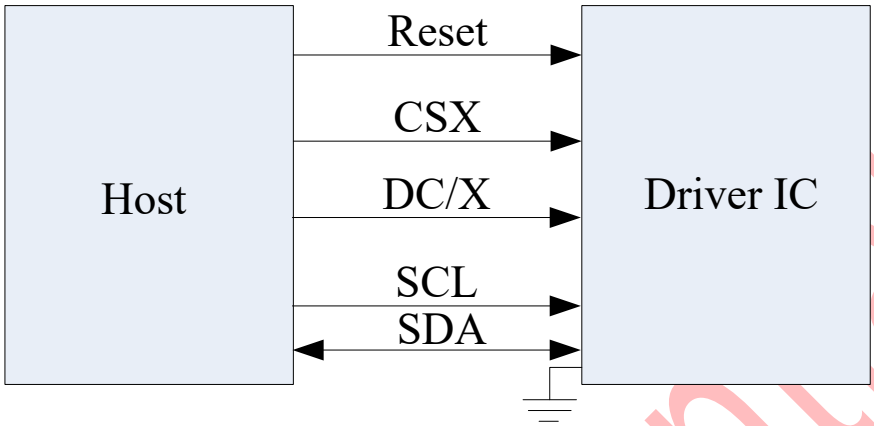
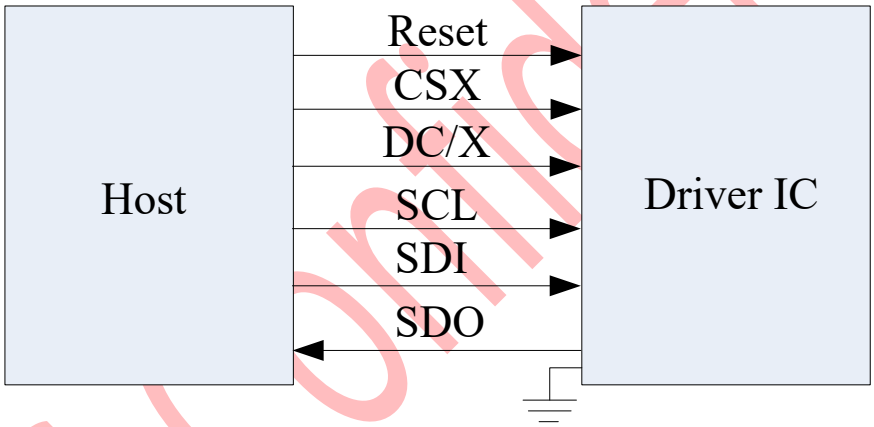
4 Line Interface mode0



4 Line Interface mode1



5.3.2.1. Write Sequence

The write mode of the interface means the host writes commands and data to AXS15231E. The 4-lines serial data packet contains a data/command and a transmission byte. If D/CX is “low”, the transmission byte is interpreted as a command byte. If D/CX is “high”, the transmission byte is stored in the display data RAM (Memory write command), or command register as parameter.

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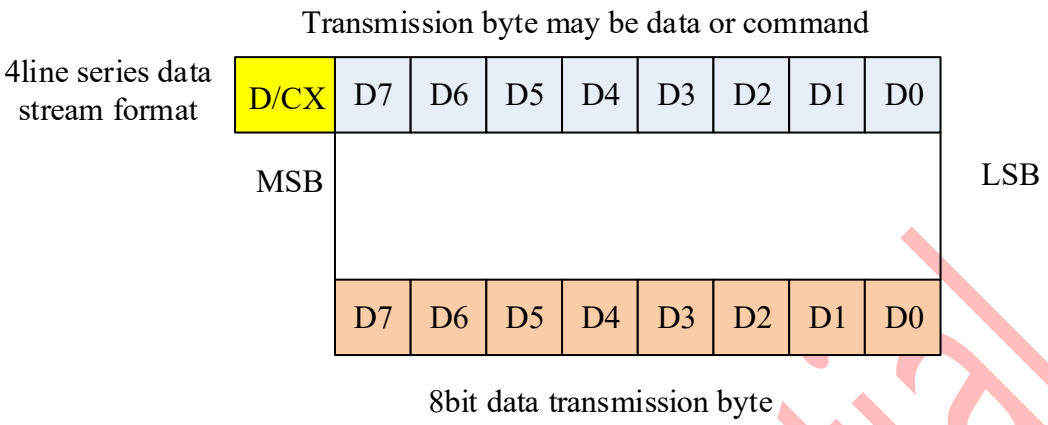
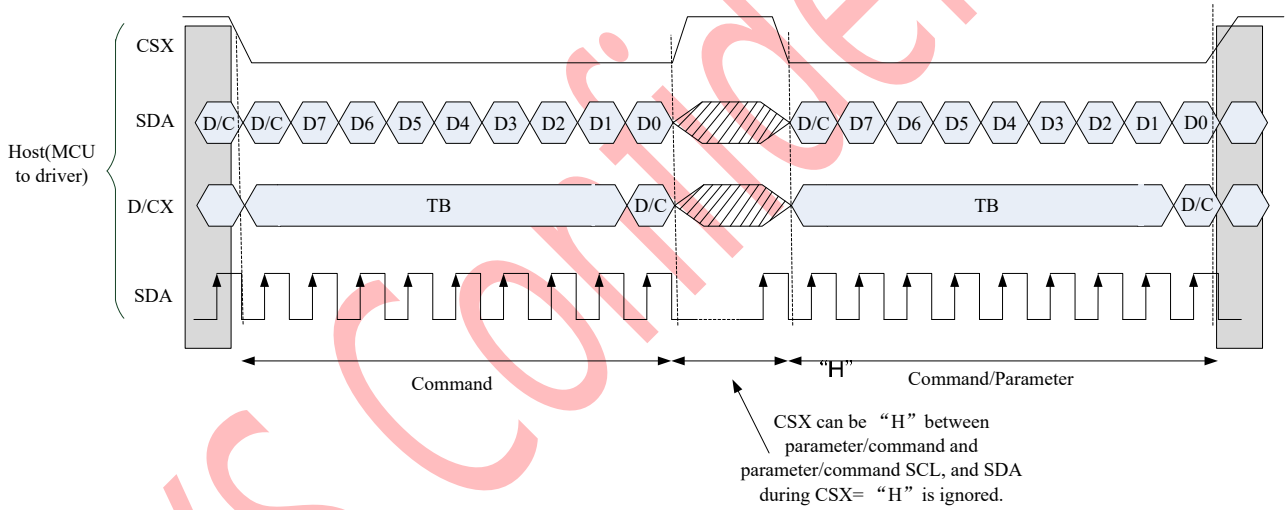


The host drives the CSX pin to low and the MSB data bit (D7) is set on SDA by the host. On the next falling edge of SCL the next bit (D6) is set on SDA. If the optional D/CX signal is used, a byte is eight read cycle long. The 4-line serial interface writes sequence described in the Figure as below.



5.3.2.2. Read Sequence

The read mode of the interface means that the micro controller reads register value from the driver. To achieve read function, the micro controller first has to send a command (read ID or register command) and then the following byte is transmitted in the opposite direction. After that CSX is required to go to high before a new command is send (see the below figure). The driver samples the SDA (input data) at rising edge of SCL, but shifts SDA (output data) at the falling edge of SCL. Thus the micro controller is supported to read at the rising edge of SCL.

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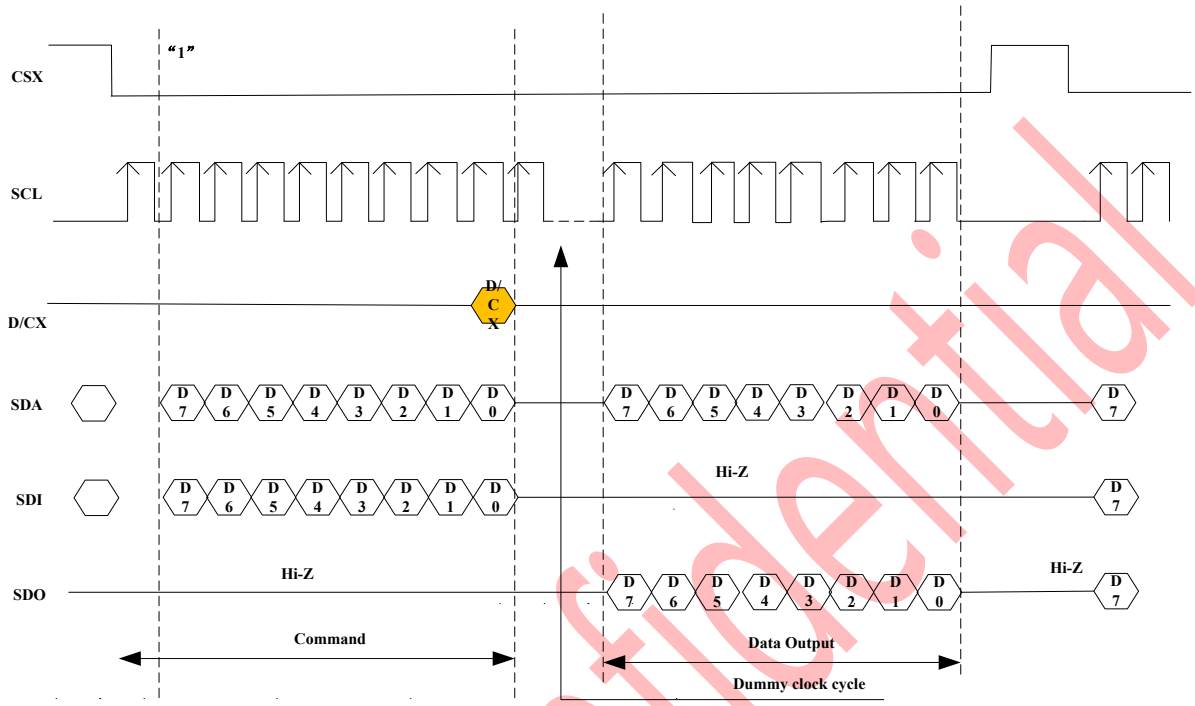
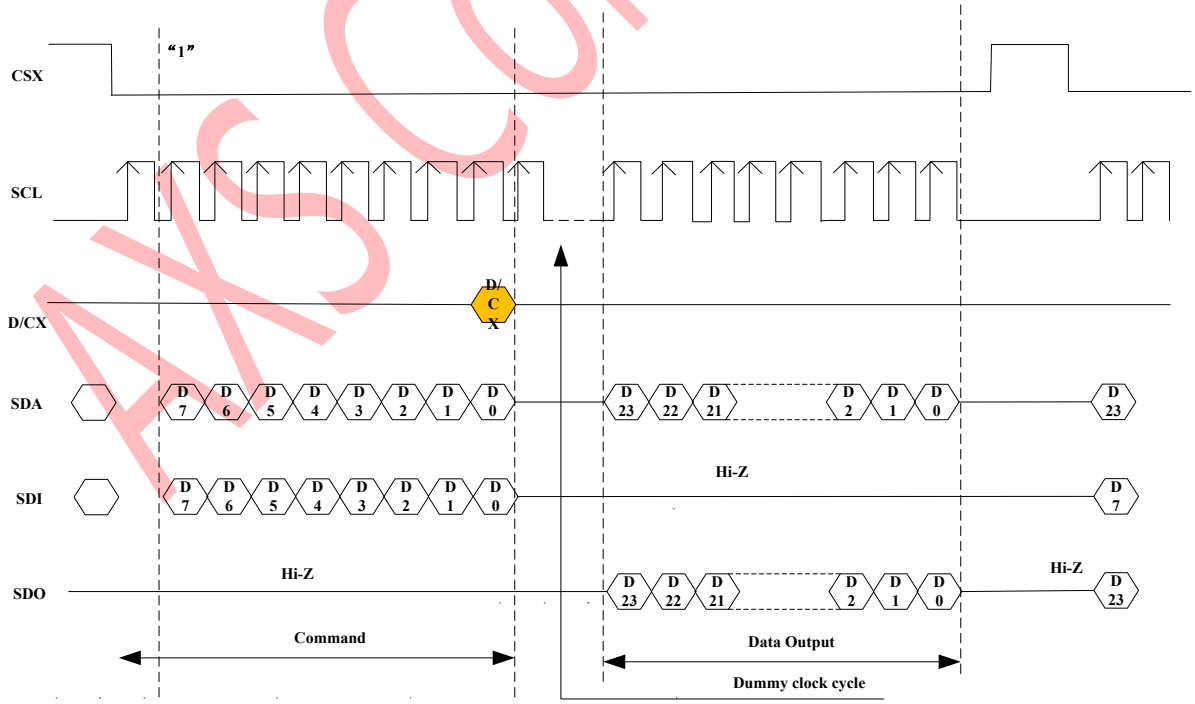
5.3.2.2.1. 4-line serial protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read, cr_spi_rd_en=1):



5.3.2.2.2. 4-line serial protocol (for RDDID command: 24-bit read,cr_spi_rd_en=1)



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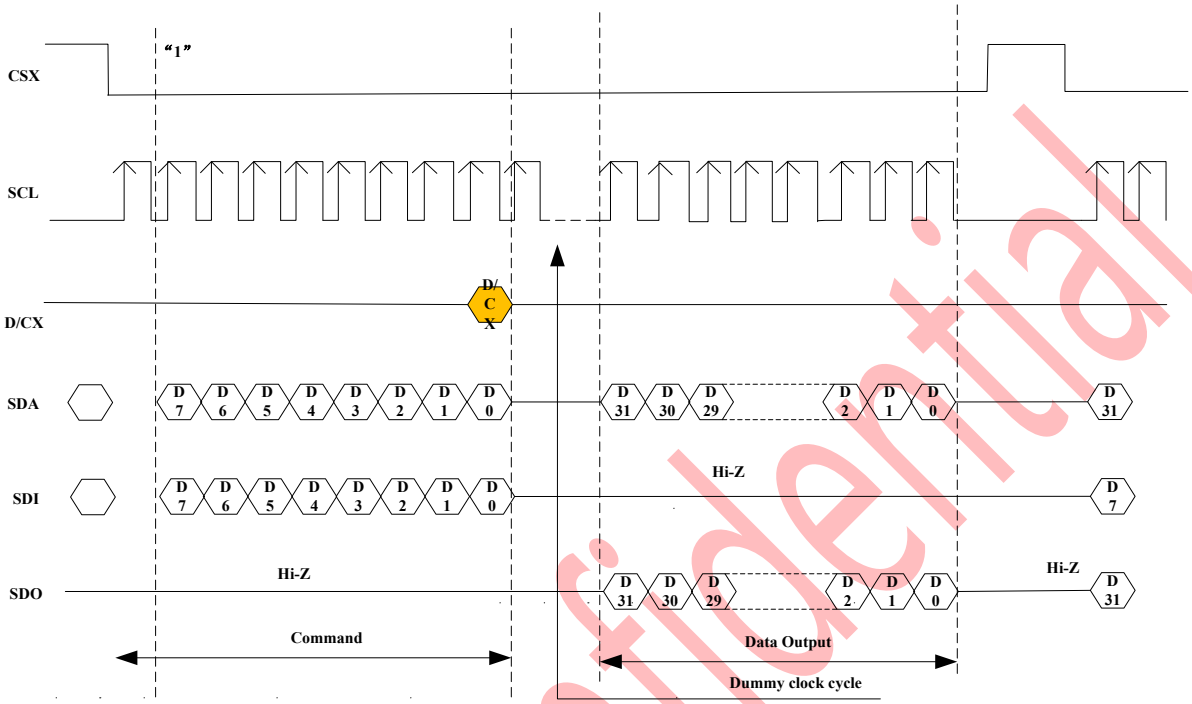
5.3.2.2.3. 4-line serial protocol (for RDDST command: 32-bit read,cr_spi_rd_en=1)



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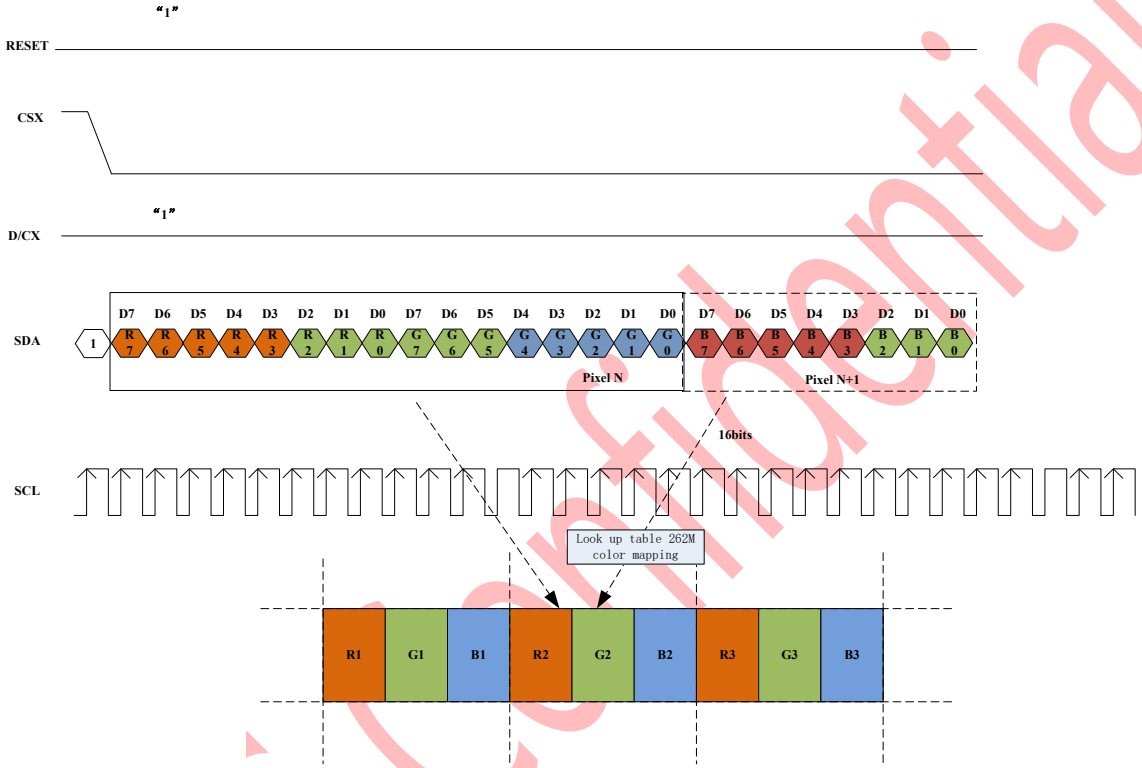
5.3.2.3. 4-SPI Color format

Different display data formats are available for three colors depth supported by the LCM listed below. 65k colors, RGB 5-6-5-bit input
262k colors, RGB 6-6-6-bit input
16.7M colors, RGB 8-8-8-bit input

5.3.2.3.1. Write data for 16-bit/pixel (RGB-5-6-5-bit input), 65K-Colors, cr_spi_format=0



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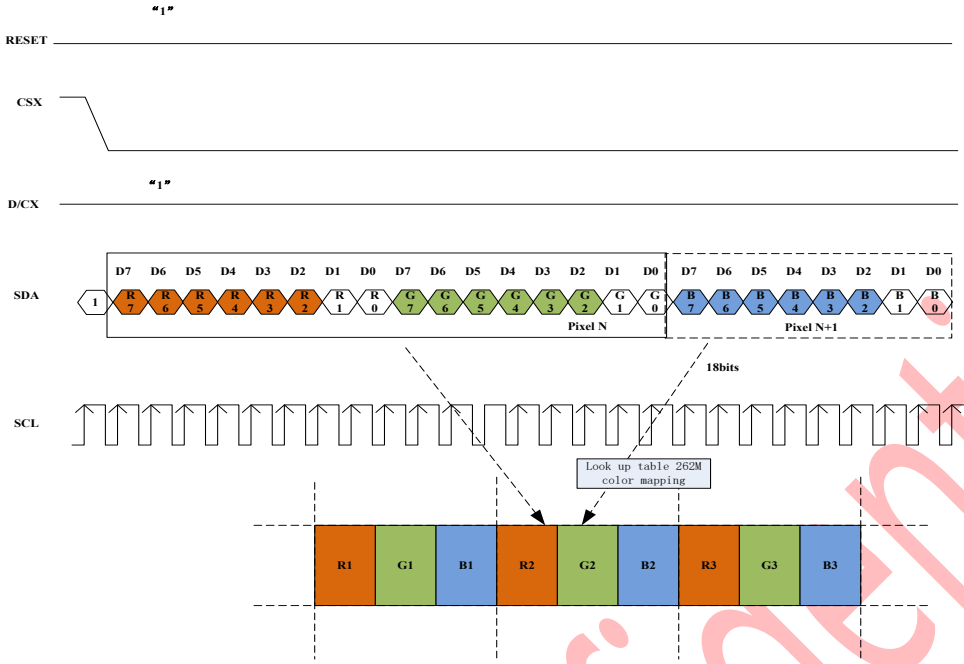
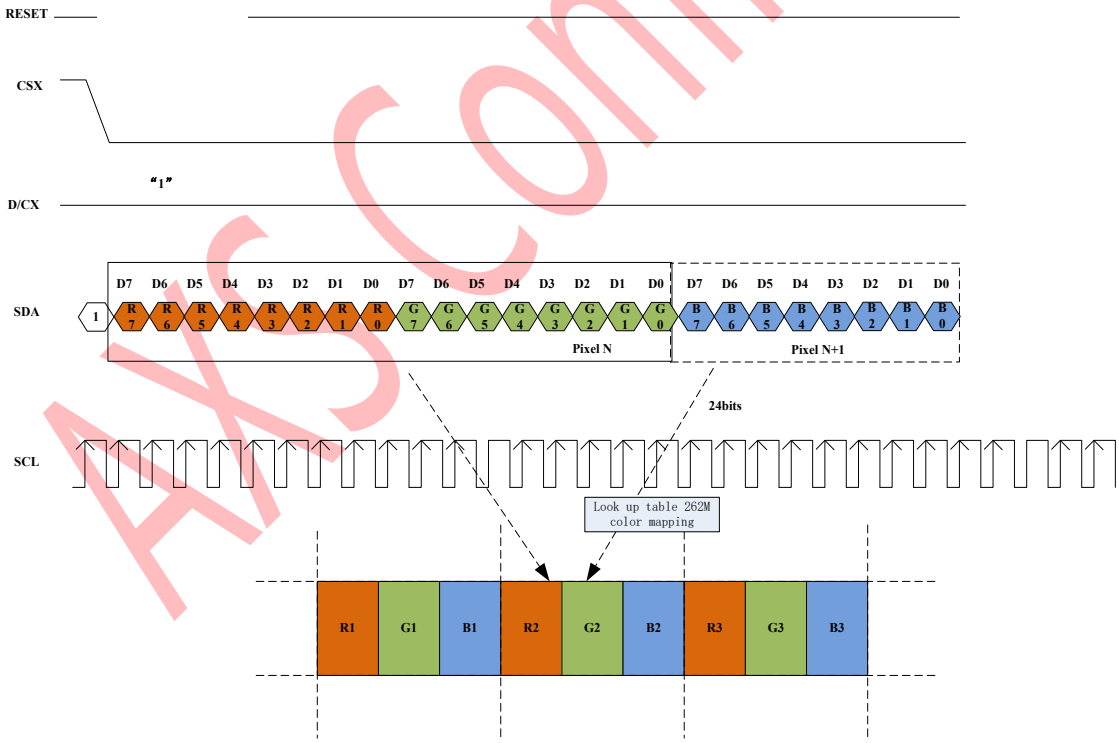
5.3.2.3.2. Write data for 18-bit/pixel (RGB-6-6-6L-bit input), 262K-Colors, cr_spi_format=1



5.3.2.3.3. Write data for 24-bit/pixel (RGB-8-8-8-bit input), 16.7M-Colors, cr_spi_format=1



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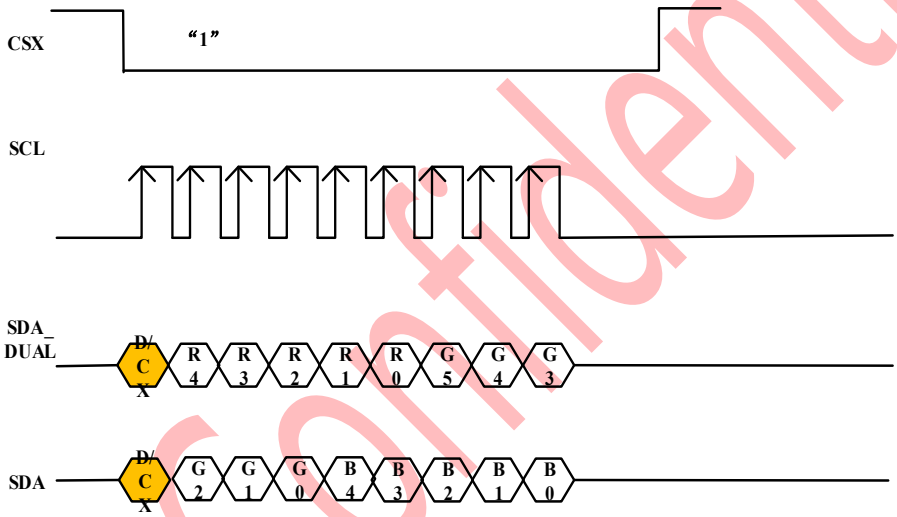
5.3.3. 2-data-line mode

This mode is active when 2data_en set to “1” in 3-wire. Only frame pixel data write transitions are sent in 2-data-line mode, register write/read is still sent in 3-wire.
The chip-select CSX (active low) enables and disables the serial interface. SCL is the serial data clock. SDA and SDA_DUAL are serial data lines.

Serial data must be input to SDA in the sequence D/CX, D23 to D12 and SDA_DUAL in the sequence D/CX, D11 to D0. The AXS15231E reads the data at the rising edge of SCL signal. The first bit of serial data D/CX is data/command flag. It must be set to "1", D23 to D0 bits are display RAM data.

5.3.3.1.1. 3-line write data for 16-bit/pixel (RGB-5-6-5-bit input), 65K-Colors, cr_spi_format=0



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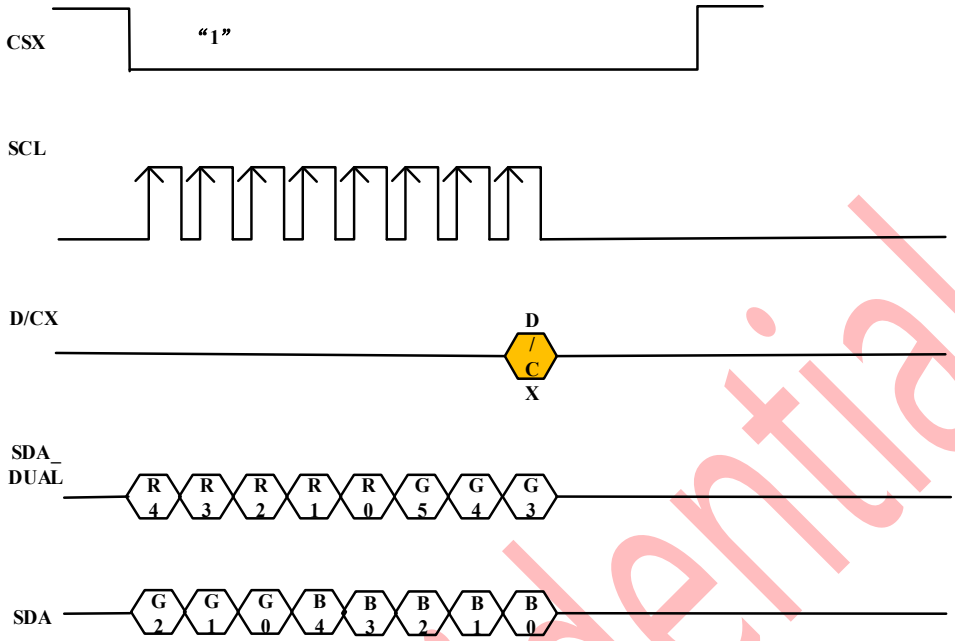
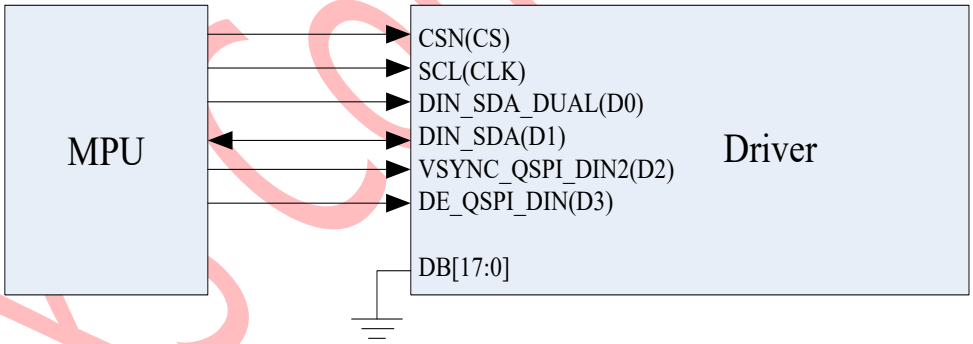
5.3.3.1.2. 4-line write data for 16-bit/pixel (RGB-5-6-5-bit input), 65K-Colors, cr_spi_format=0



5.4. Quad Serial Peripheral Interface

The Quad Serial Peripheral Interface of AXS15231 can be selected by setting hardware pin IM [3:0] to "1010". The following shown figure is the example of interface with Quad Serial Peripheral Interface.



5.4.1. Write Cycle Sequence

The AXS15231 reads the data at the rising edge of SCL signal. The timing of Write Cycle Sequence is shown as below CMD_WR only use SDA, first byte=0x02

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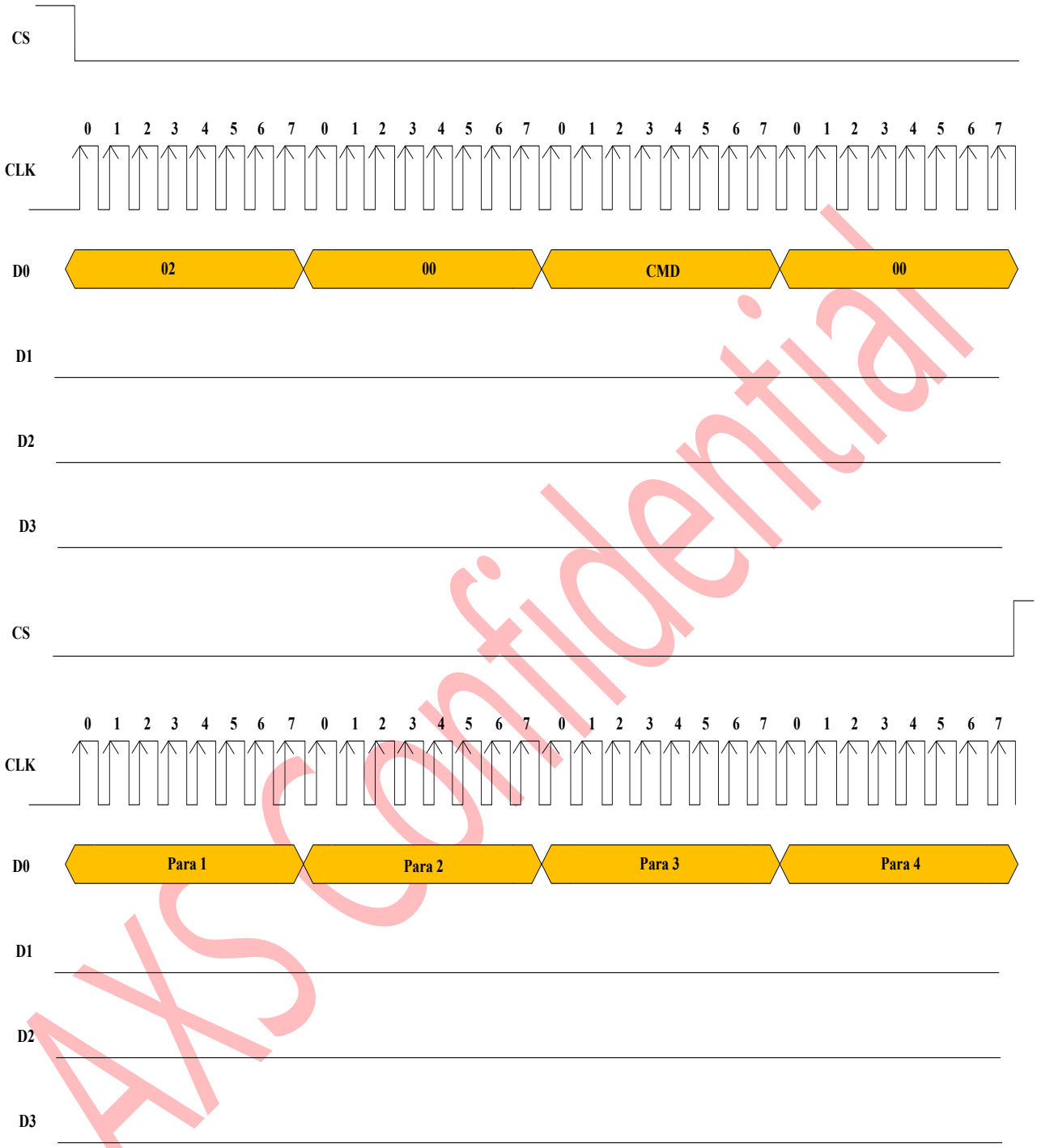

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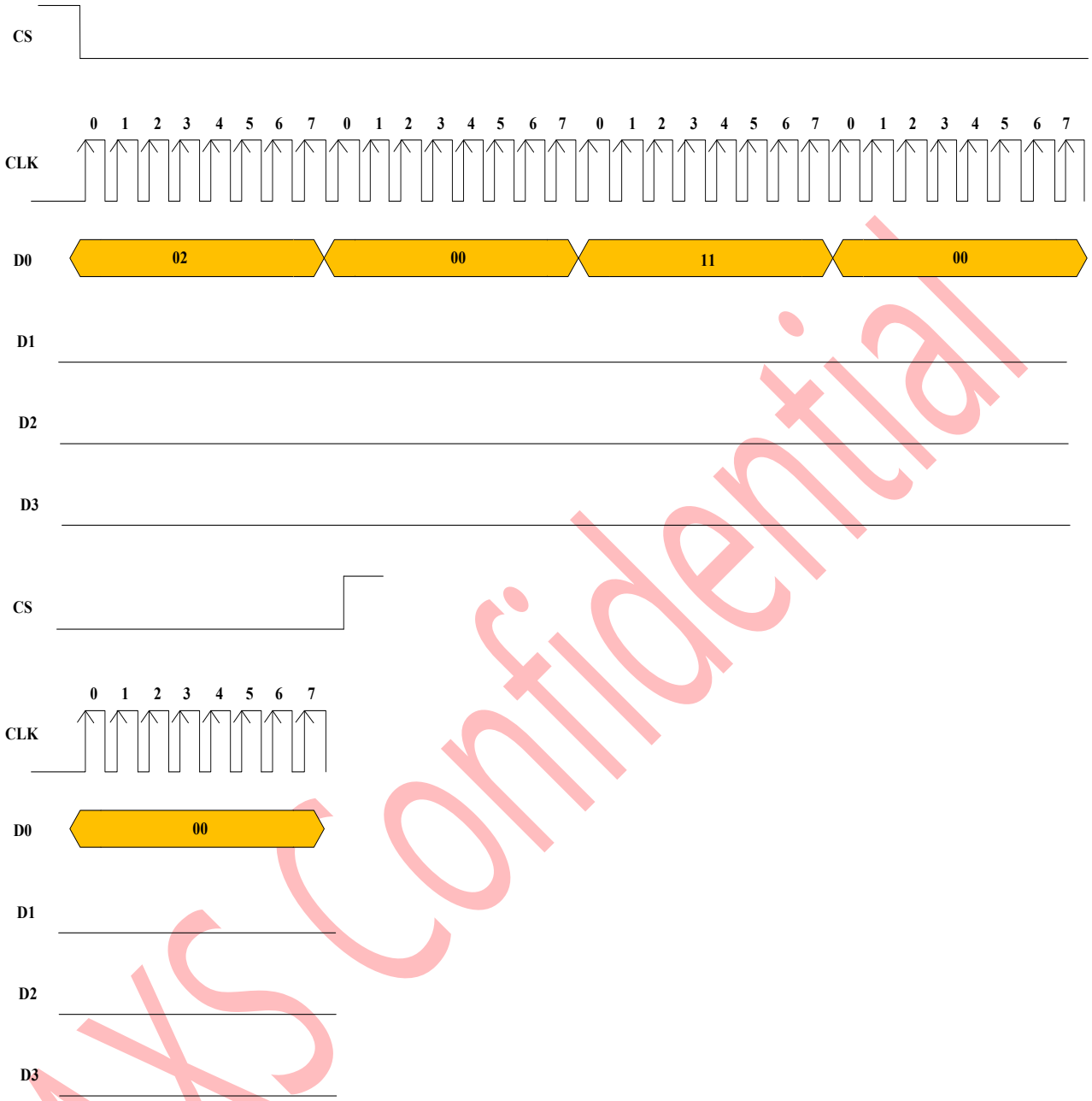

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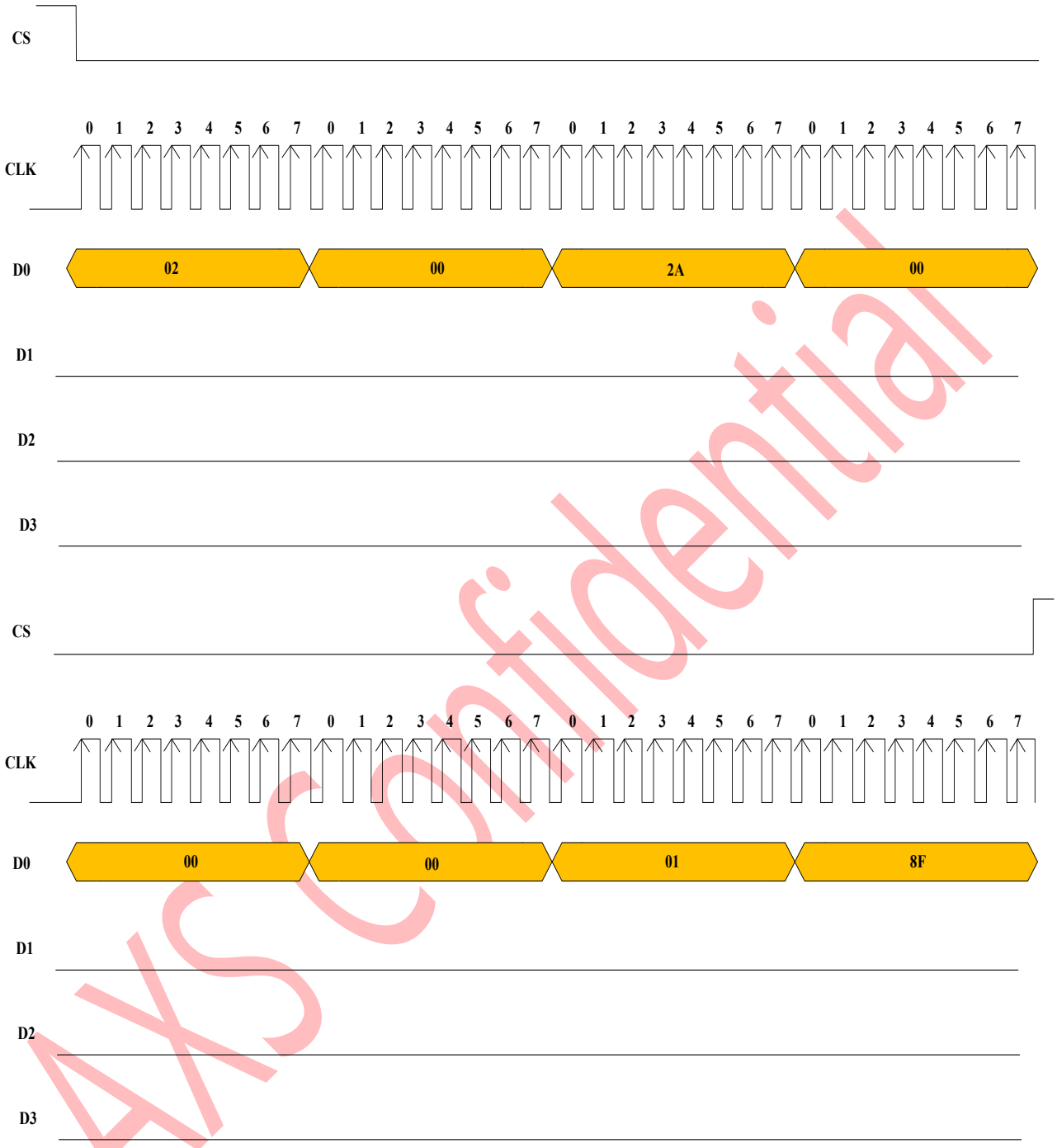

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5.4.2. Read Cycle Sequence

The timing of Read Cycle Sequence is shown as below CMD_RD: Only Use SDA0, First Byte=0x03

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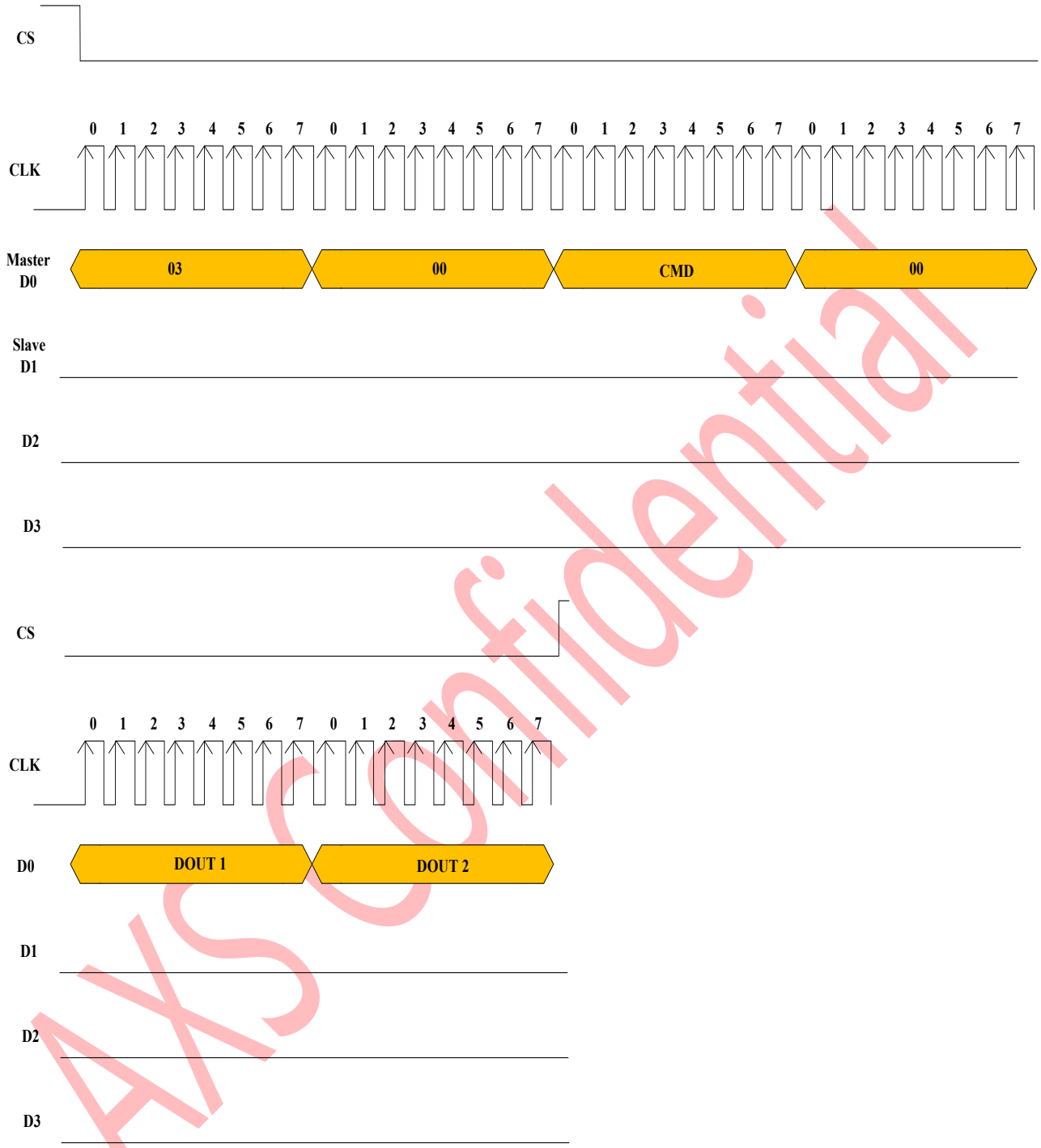

5.4.3. QSPI Color Format

In quad serial Peripheral interface, different display data format is available for five color depths

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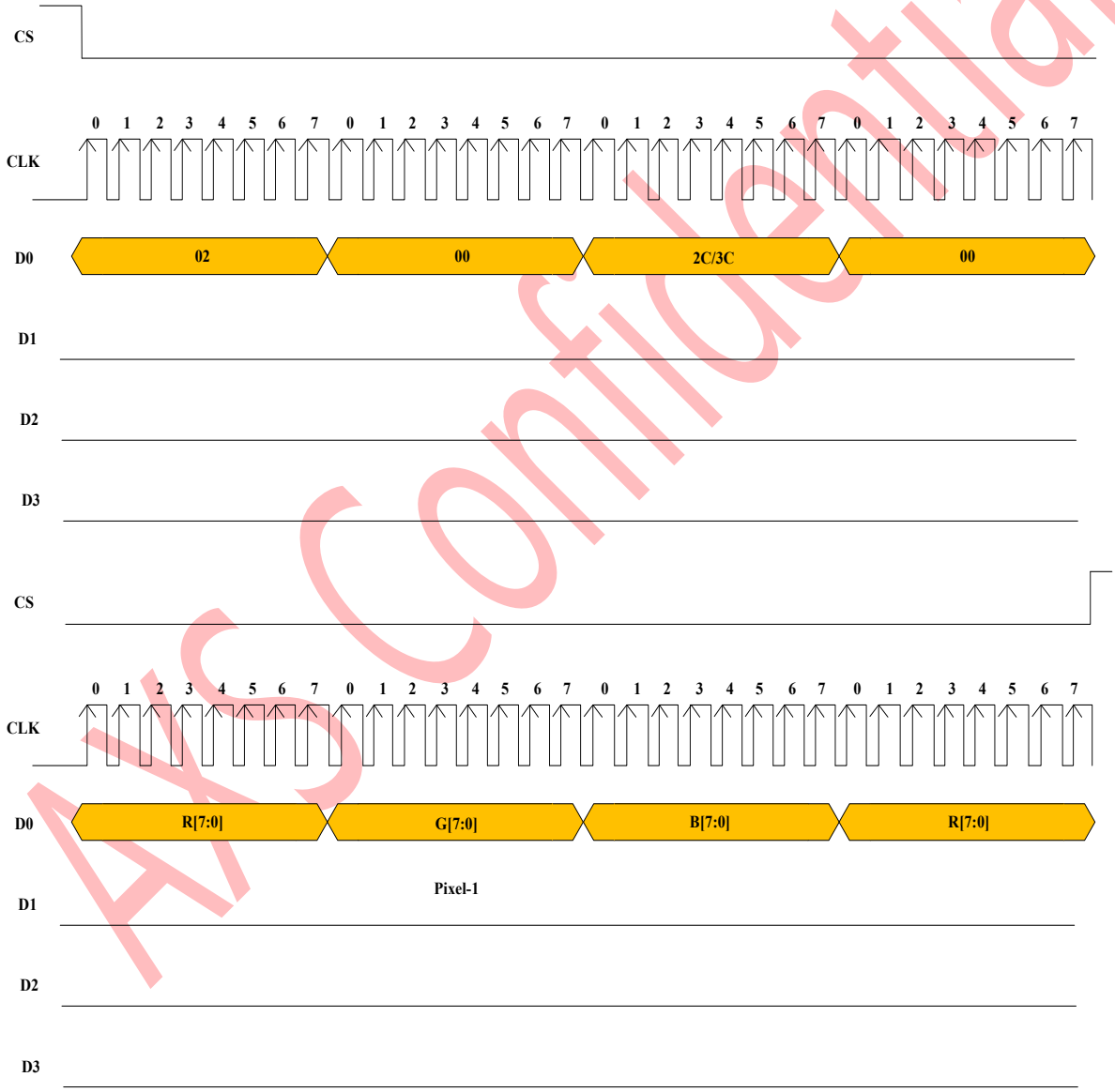
supported by the LCM listed below.
-16.7M colors RGB 8, 8, 8-bits input
-262k colors, RGB 6, 6, 6 -bits input.
-65k colors, RGB 5, 6, 5 -bits input
-256 colors, RGB 3, 3, 2 -bits input
-8 colors，RGB 1, 1, 1-bits input
-256 gray，data：00000000~11111111

5.4.3.1. 1wire data: only use SDA, first byte=0x02

5.4.3.1.1. 16.7M-Colors:24-bit/pixel (RGB 8, 8, 8 -bits input, Cr_qspis_datamode=3'b000)



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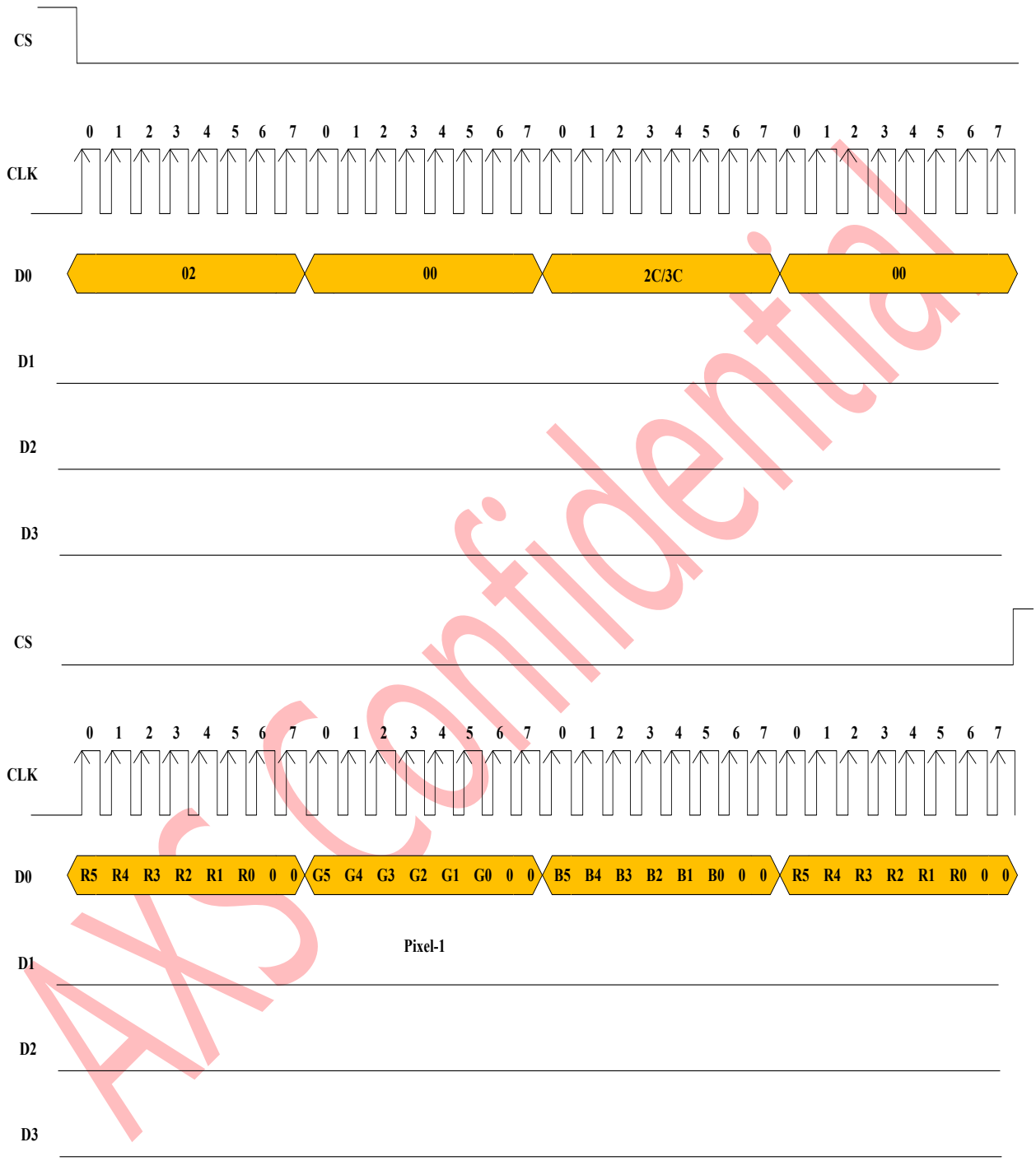
5.4.3.1.2. 262k-Colors:18-bit/pixel (RGB 6, 6, 6L-bits input, Cr_qspis_datamode=3'b000)



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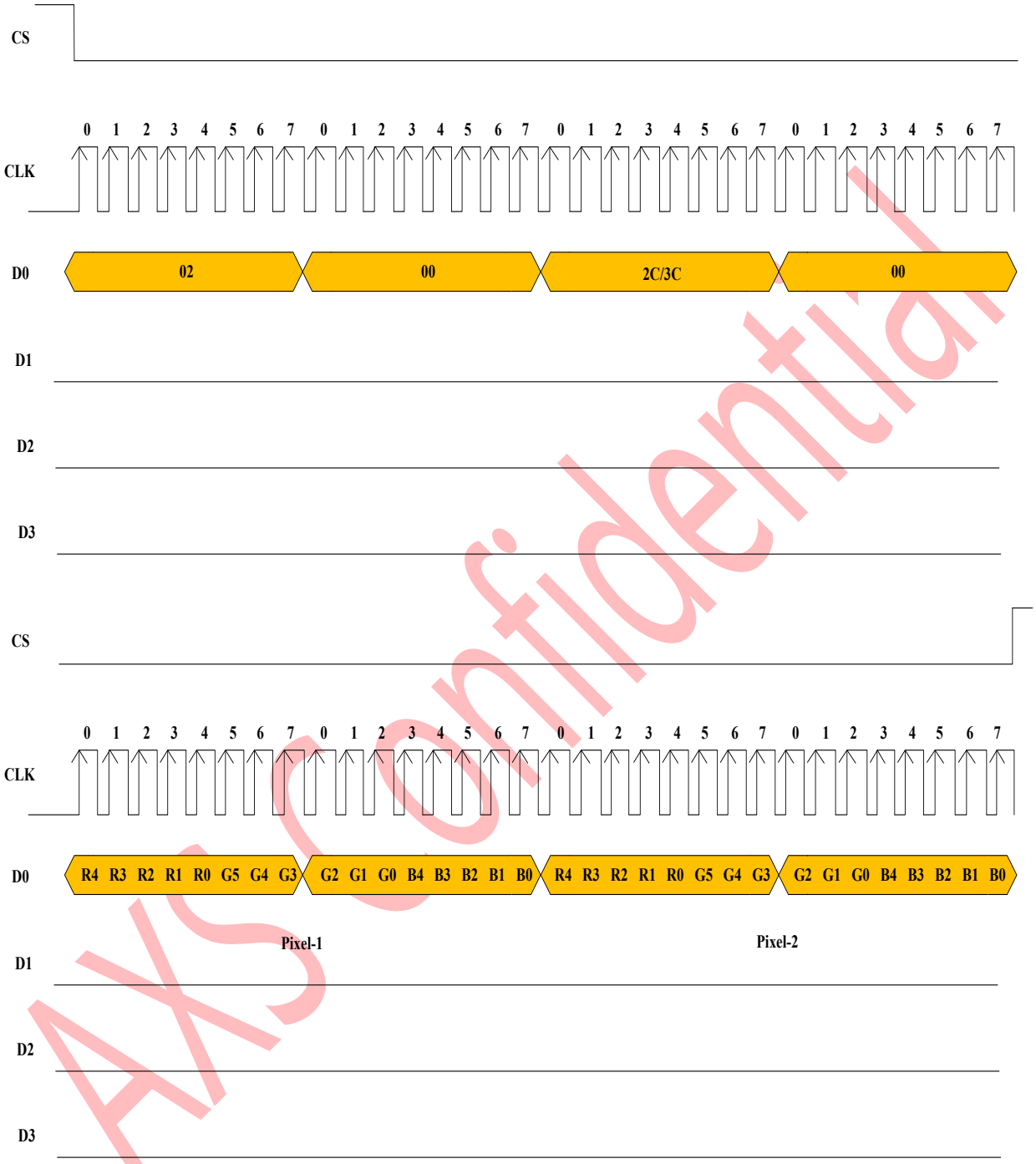
5.4.3.1.3. 65k-Colors:16-bit/pixel (RGB 5, 6,5 -bits input, Cr_qspis_datamode=3'b001)



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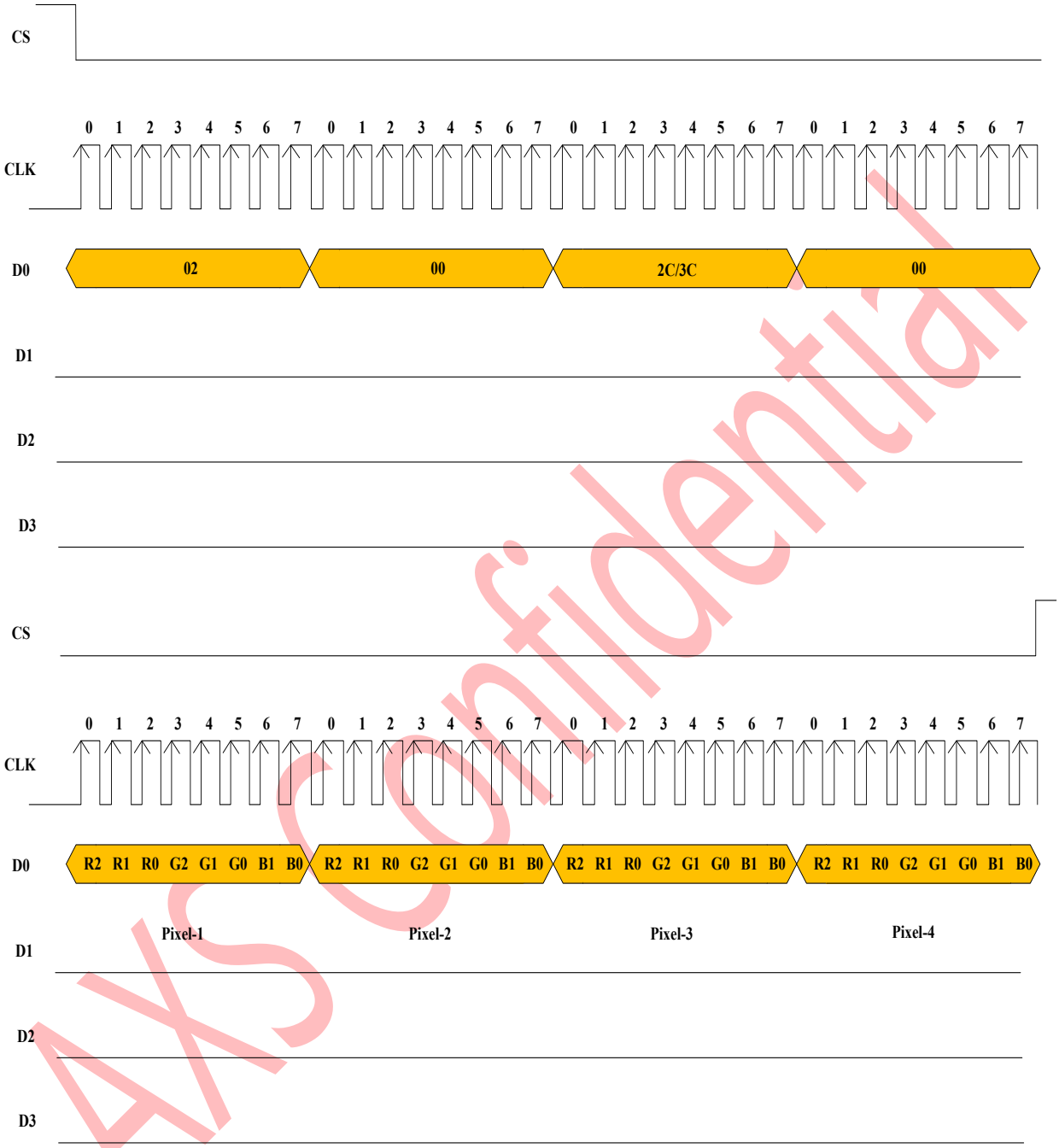
5.4.3.1.4. 256-Colors:8-bit/pixel (RGB 3, 3,2 -bits input, Cr_qspis_datamode=3'b010)



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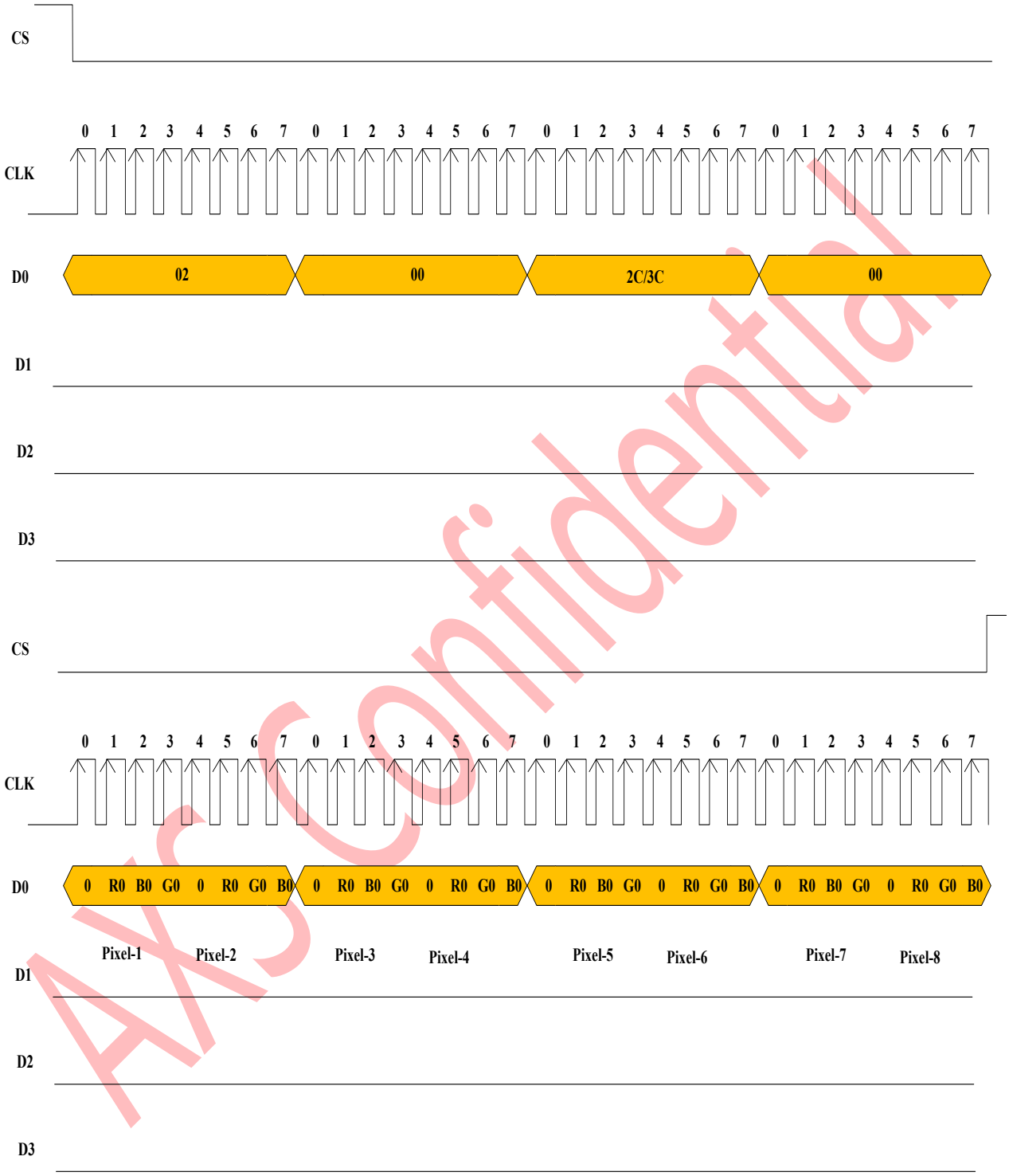
5.4.3.1.5. 8-Colors:3-bit/pixel (RGB 1, 1,1 -bits input, Cr_qspis_datamode=3'b011)



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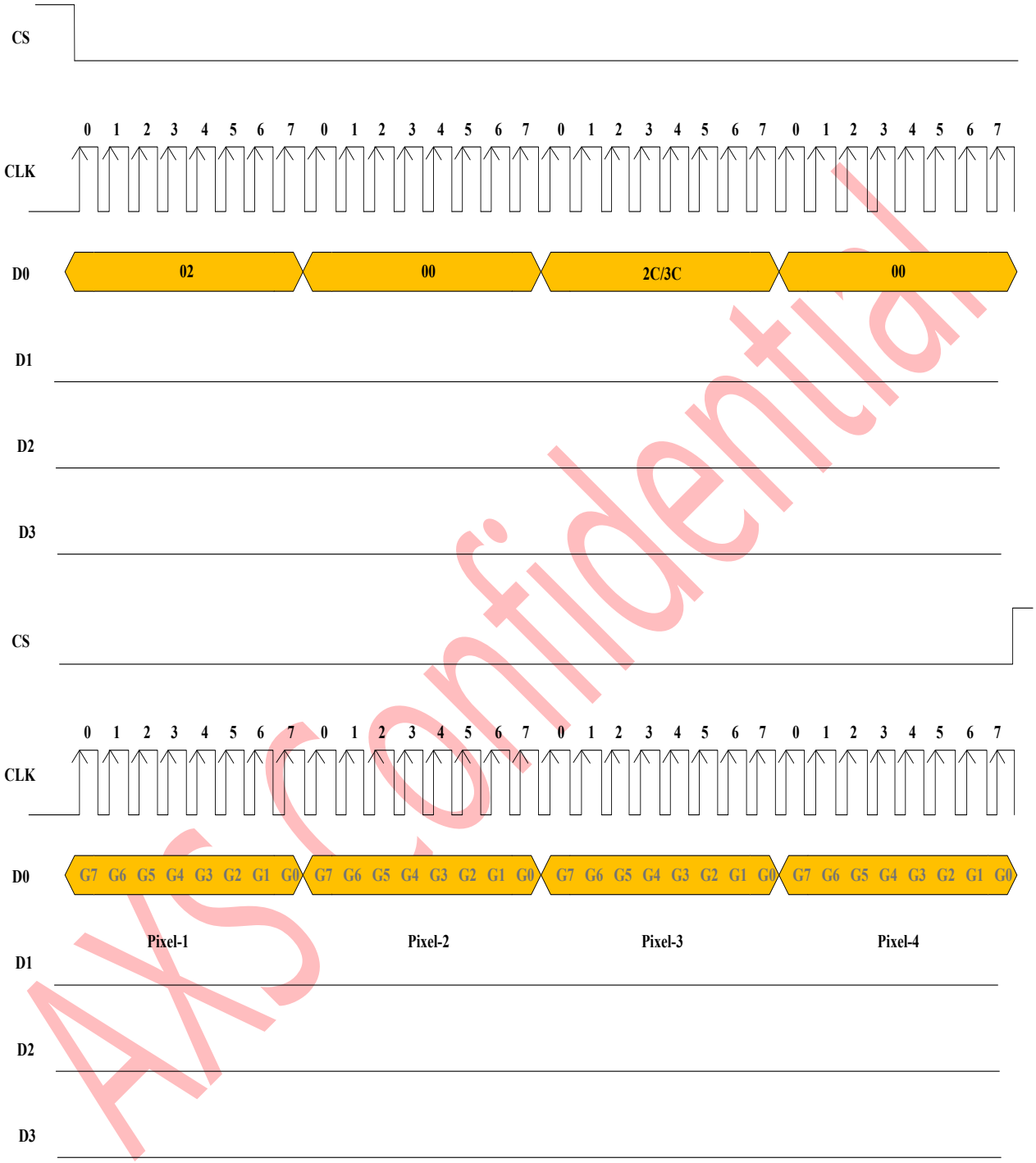
5.4.3.1.6. 256GRAY(data:bin0~bin11111111, Cr_qspis_datamode=3'b100)



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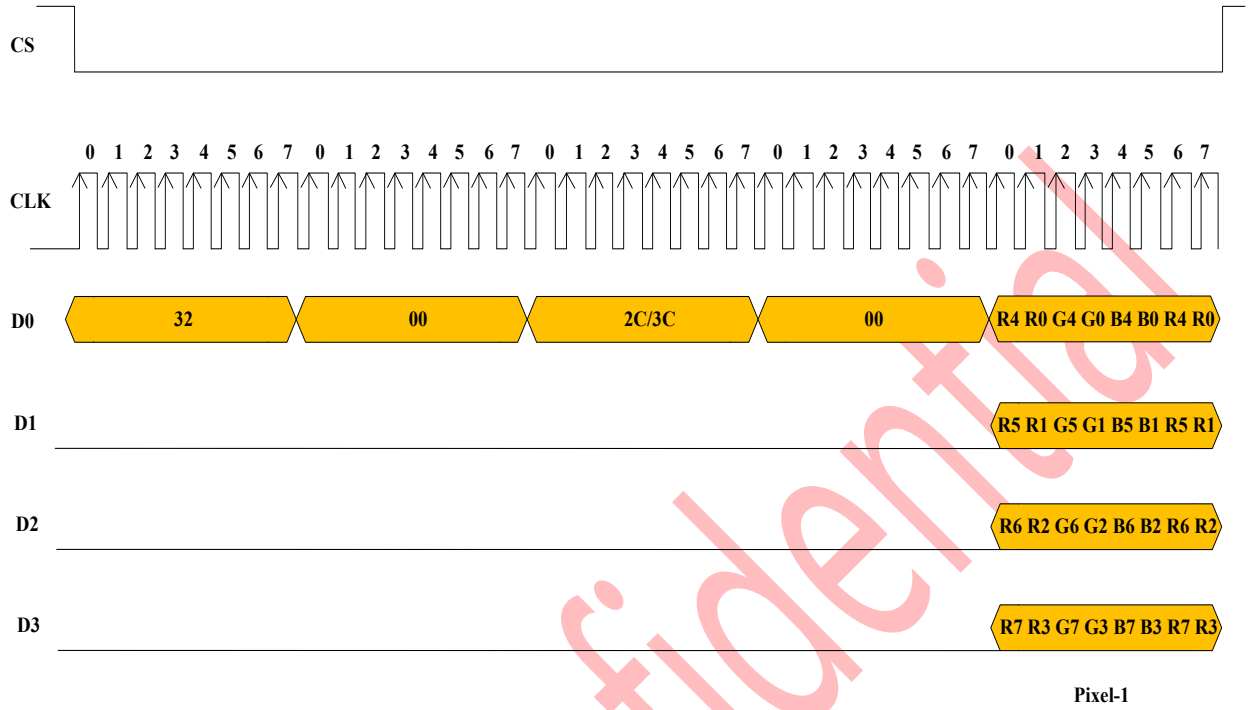
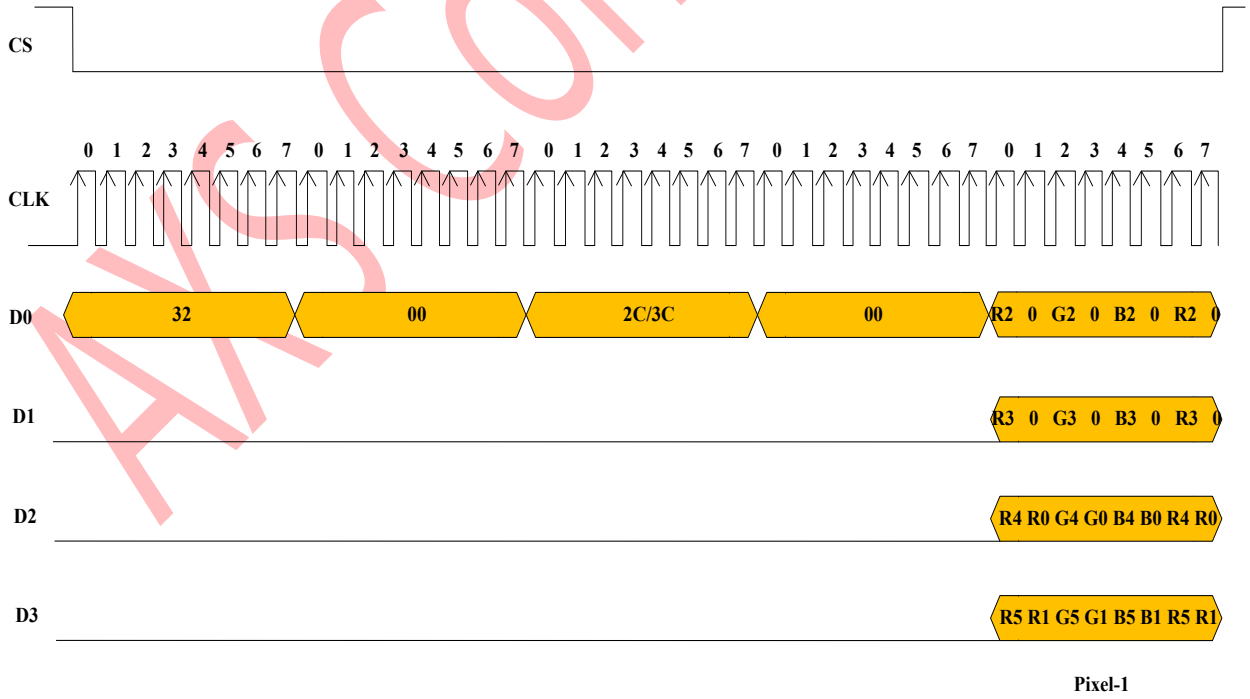
5.4.3.2. 4wire data 1wire Addr: first byte=0x32

5.4.3.2.1. 16.7M-Colors:24-bit/pixel (RGB 8, 8, 8 -bits input, Cr_qspis_datamode=3'b000)



5.4.3.2.2. 262-Colors:18-bit/pixel(RGB 6,6,6L-bits input, cr_ext_format = 01)



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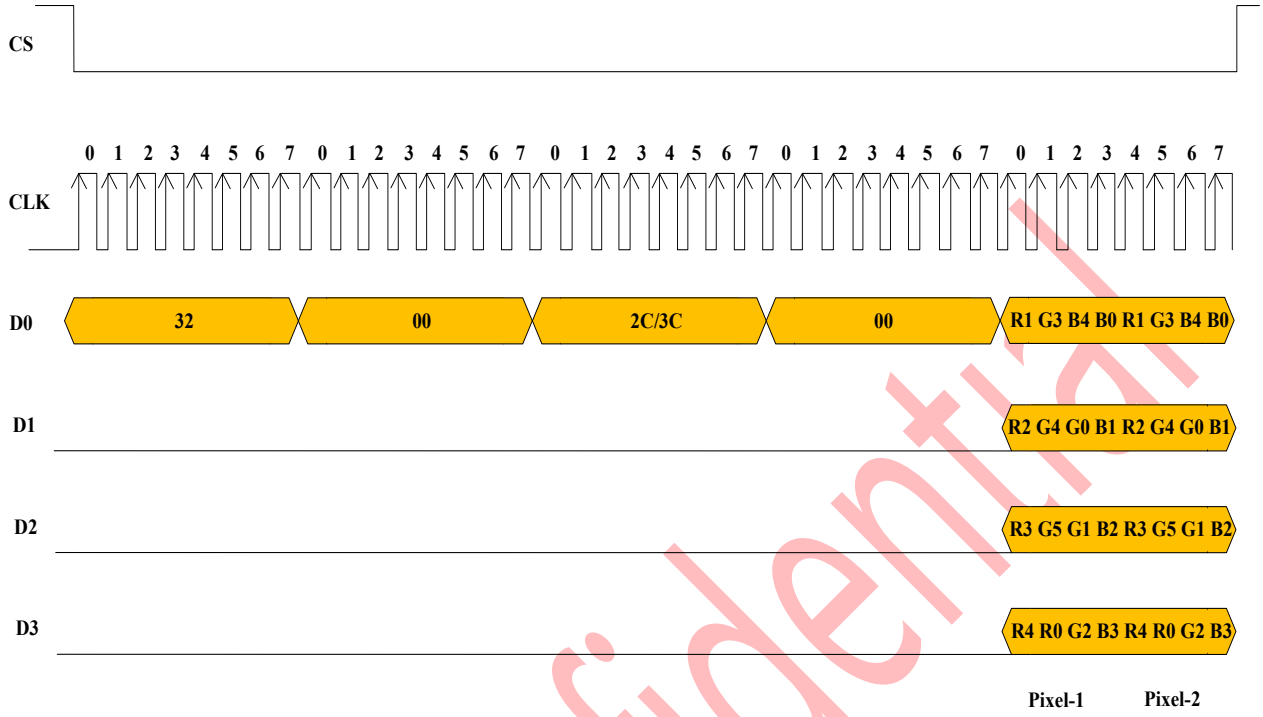
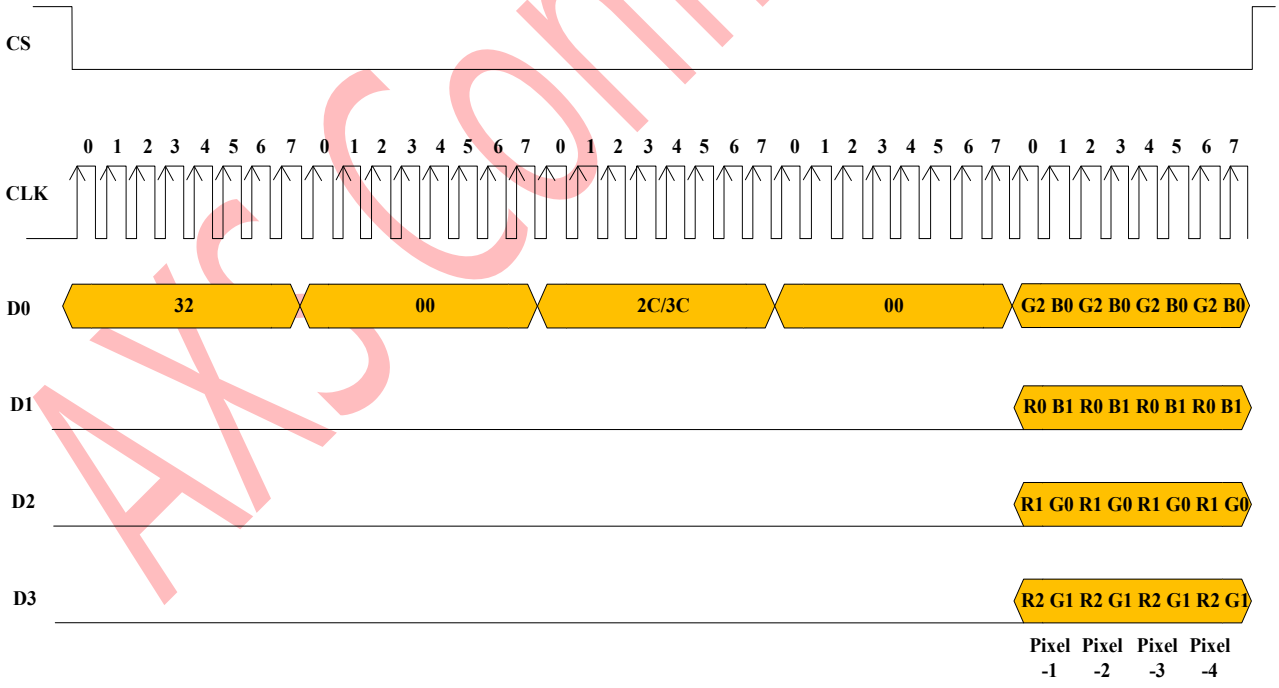
5.4.3.2.3. 65k-Colors:16-bit/pixel (RGB 5, 6,5 -bits input, Cr_qspis_datamode=3'b001)



5.4.3.2.4. 256-Colors:8-bit/pixel (RGB 3, 3,2 -bits input, Cr_qspis_datamode=3'b010)



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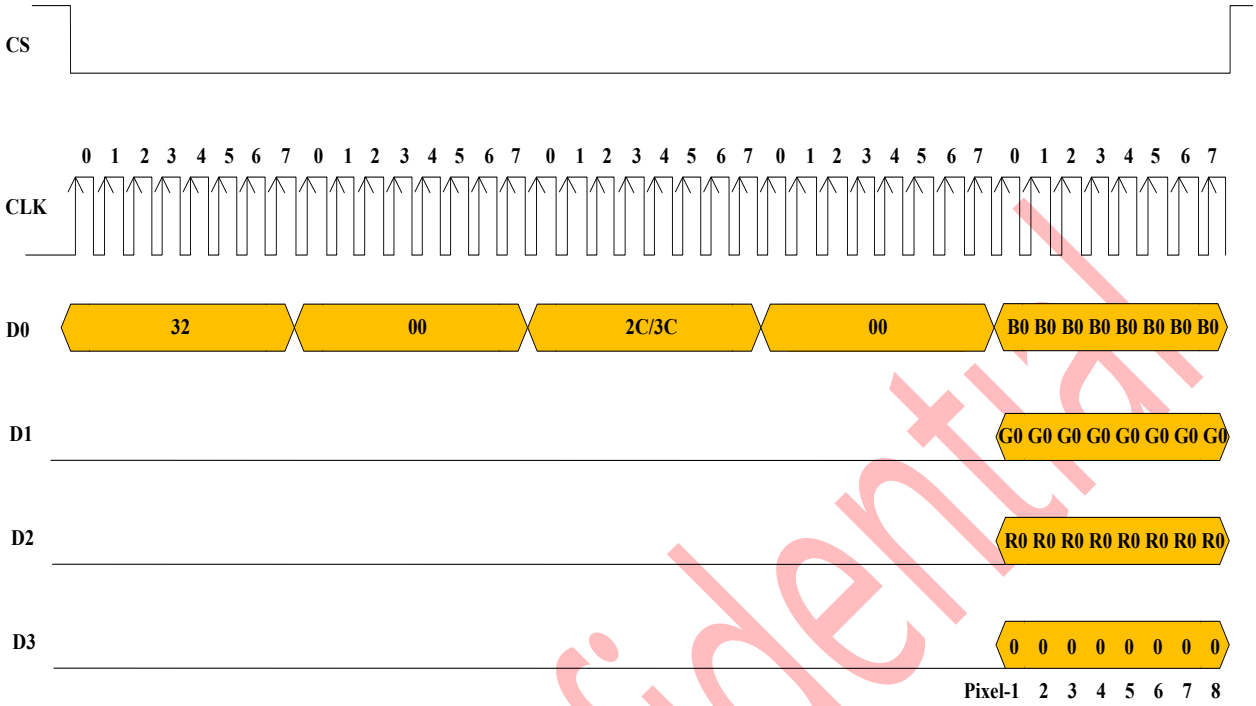
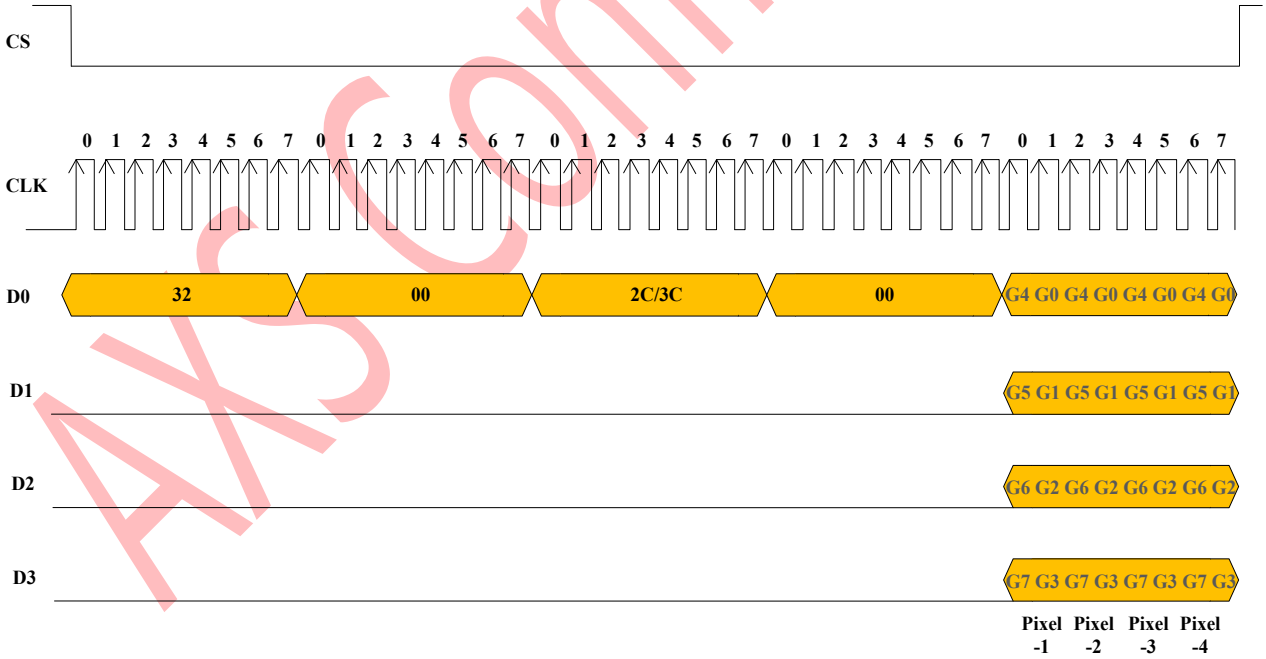
5.4.3.2.5. 8-Colors:3-bit/pixel (RGB 1, 1,1 -bits input, Cr_qspis_datamode=3'b011)



5.4.3.2.6. 256GRAY(data:bin0~bin11111111, Cr_qspis_datamode=3'b100)



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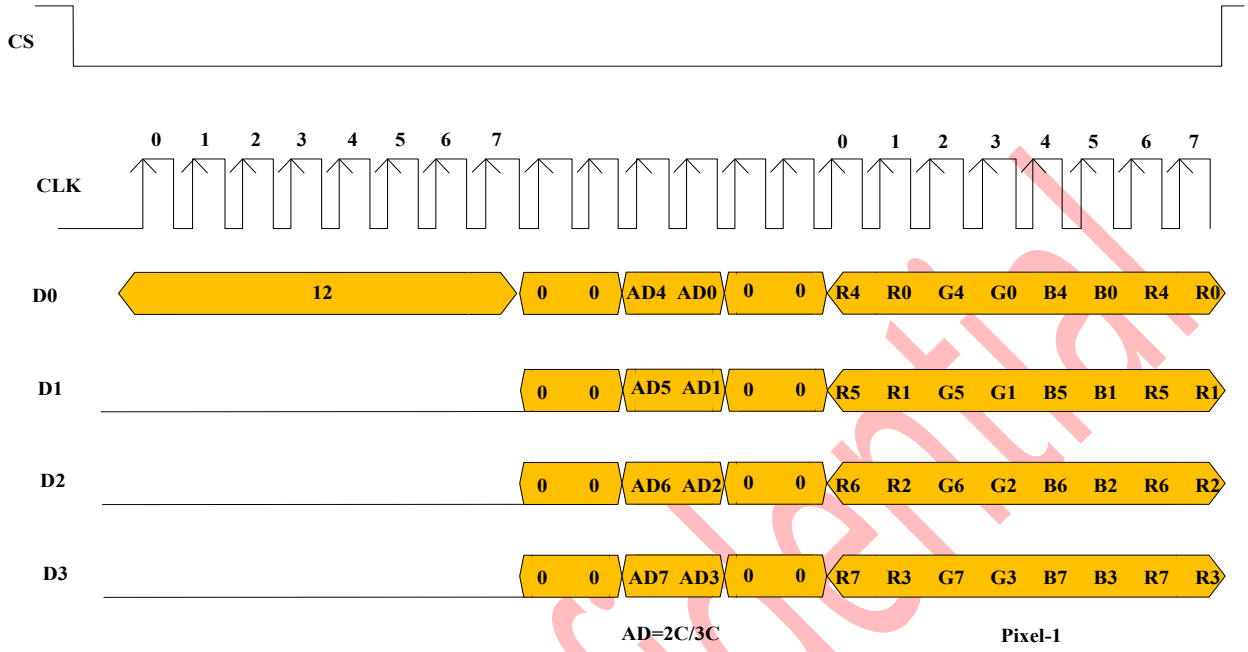
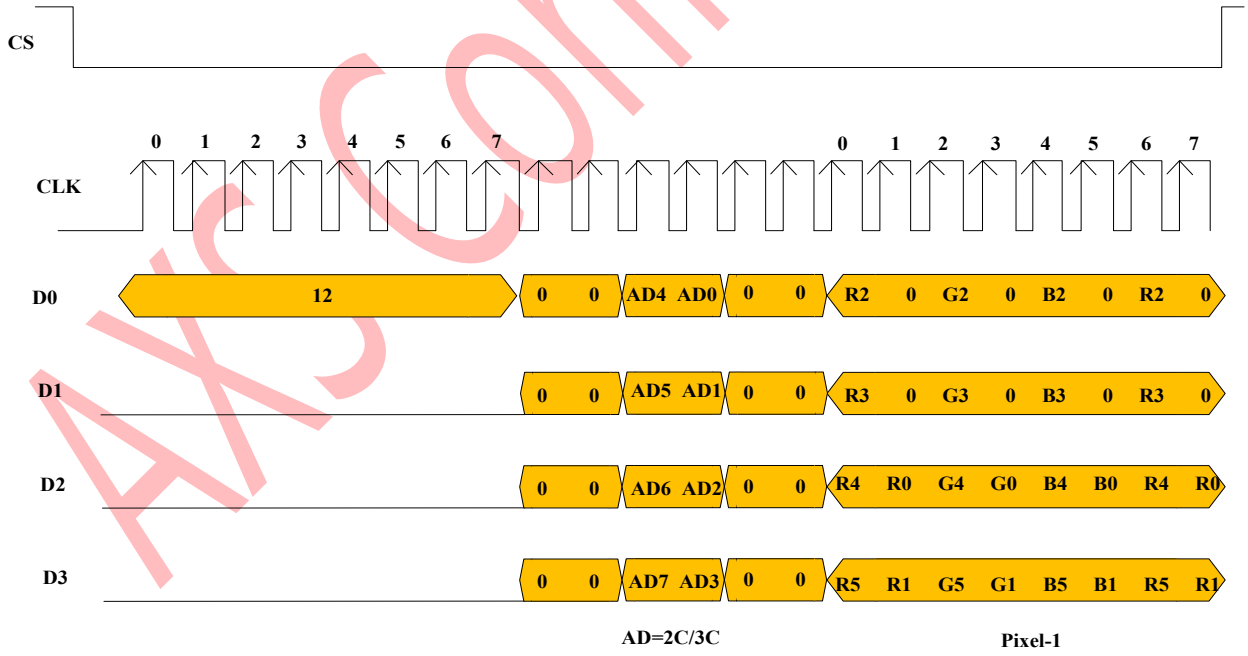
5.4.3.3. 4wire data 4wire Addr: first byte=0x12

5.4.3.3.1. 16.7M-Colors:24-bit/pixel (RGB 8, 8, 8 -bits input, Cr_qspis_datamode=3'b000)



5.4.3.3.2. 262k-Colors:18-bit/pixel (RGB 6, 6, 6L-bits input, Cr_qspis_datamode=3'b000)



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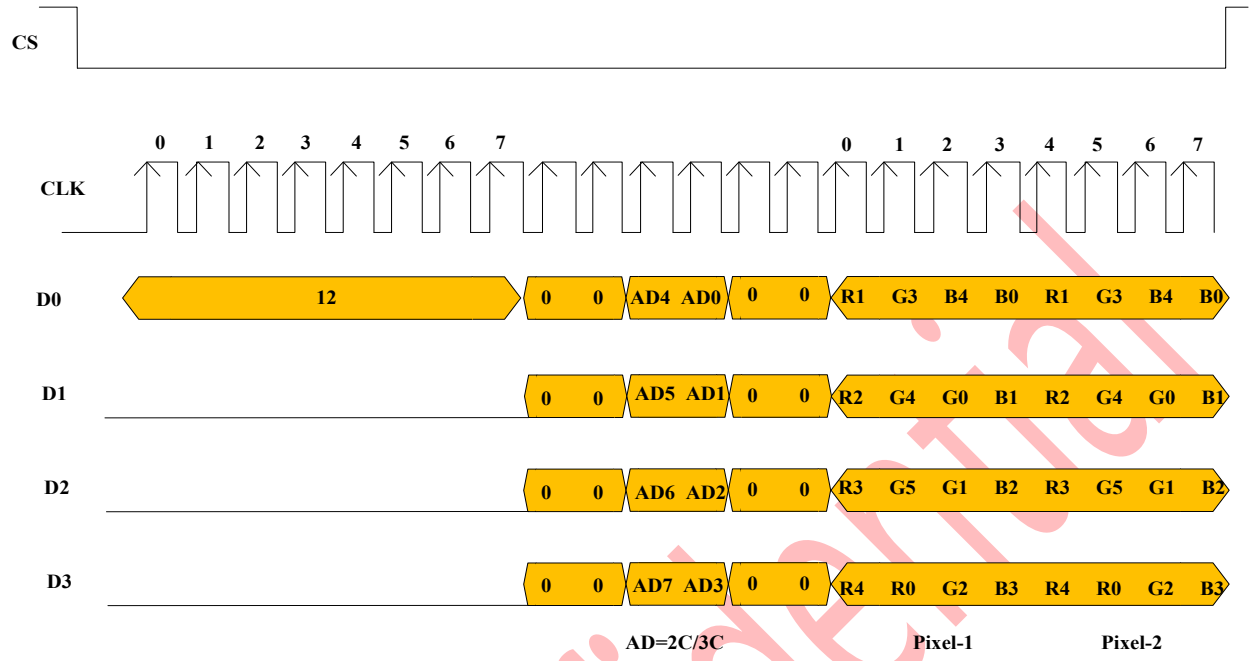
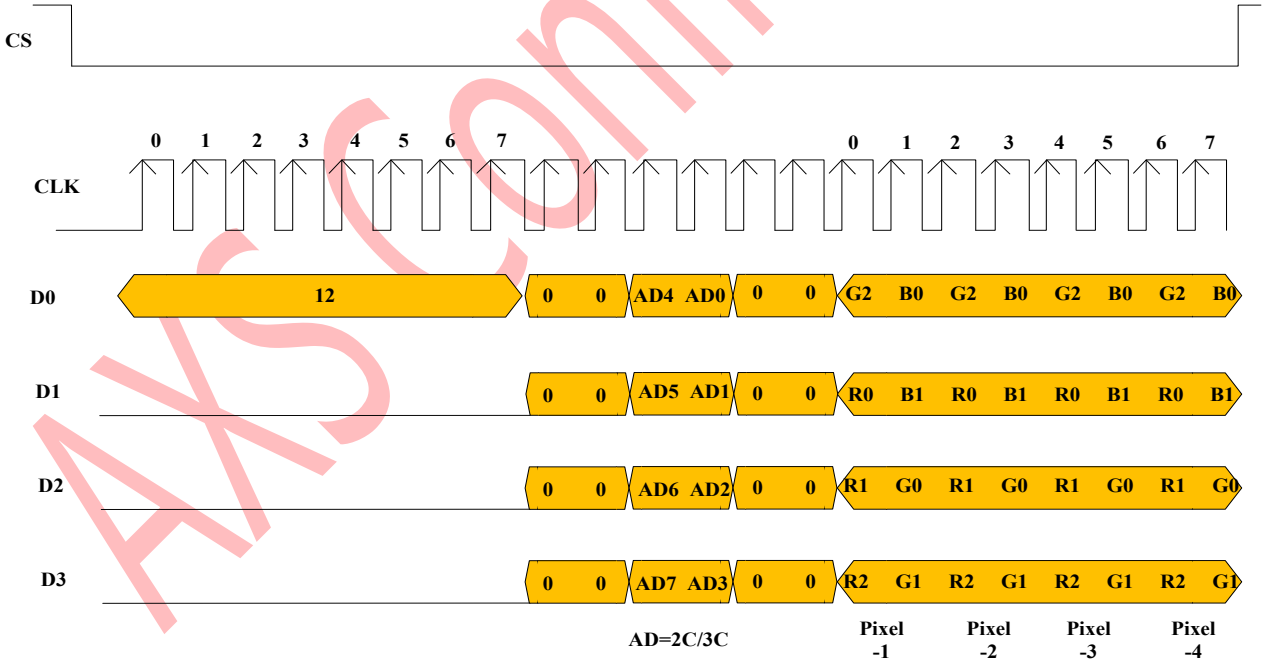
5.4.3.3.3. 65k-Colors:16-bit/pixel (RGB 5, 6,5 -bits input, Cr_qspis_datamode=3'b001)



5.4.3.3.4. 256-Colors:8-bit/pixel (RGB 3, 3,2 -bits input, Cr_qspis_datamode=3'b010)



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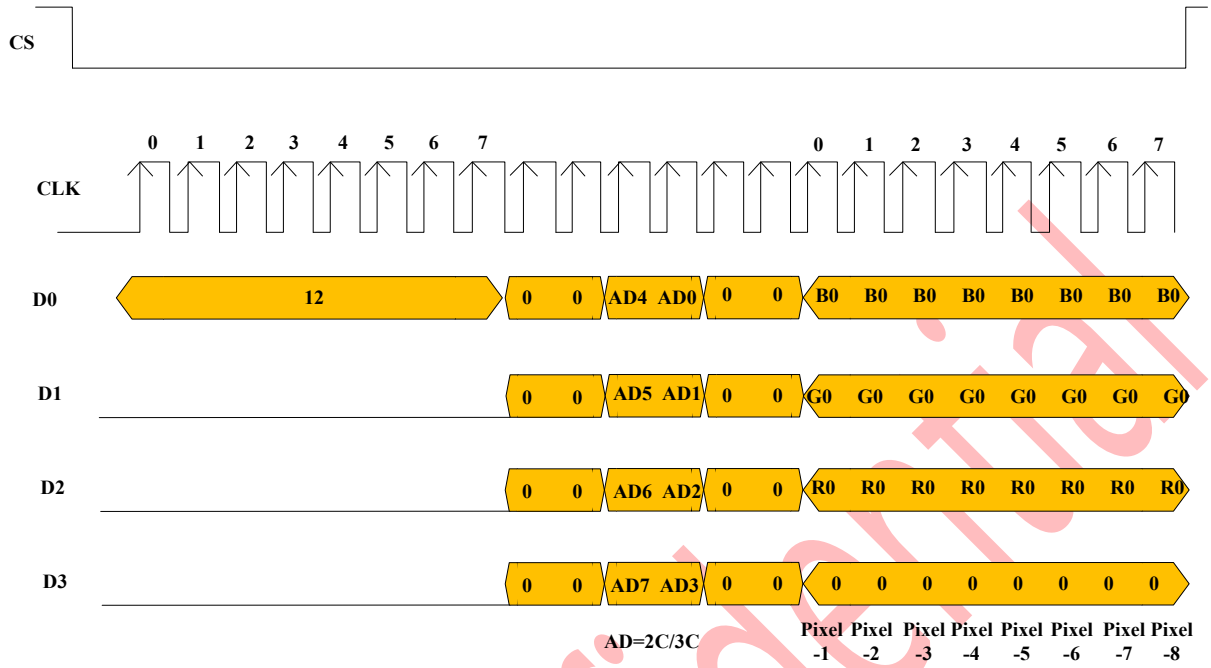
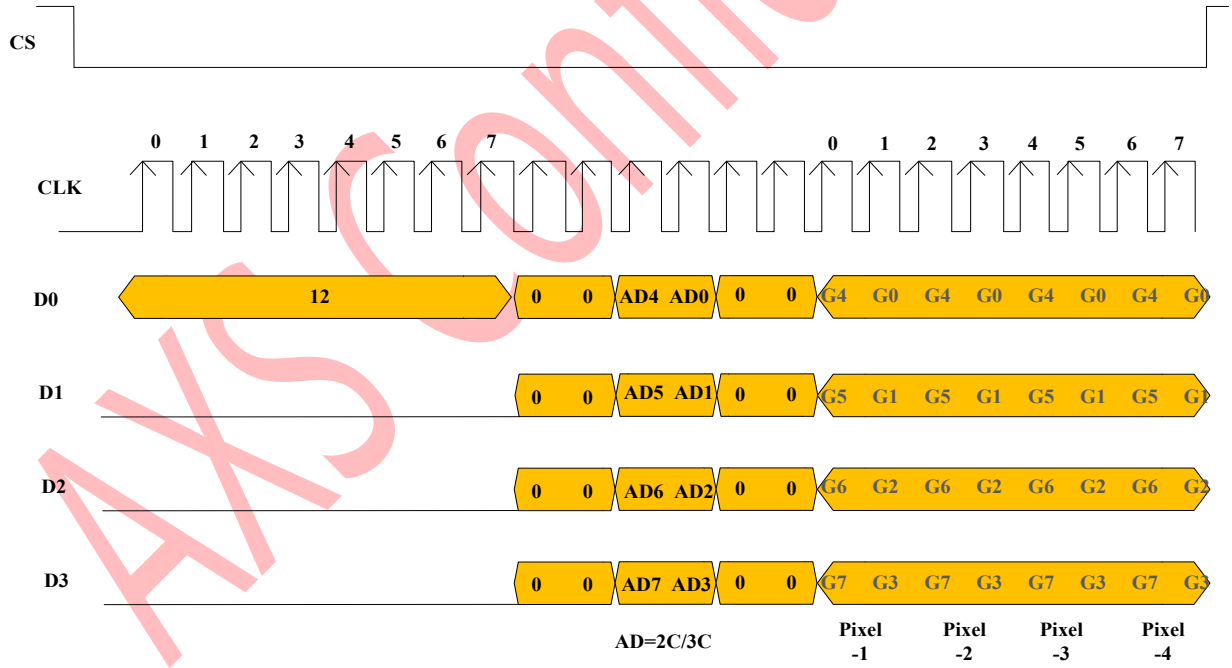
5.4.3.3.5. 8-Colors:3-bit/pixel (RGB 1, 1,1 -bits input, Cr_qspis_datamode=3'b011)



5.4.3.3.6. 256GRAY(data:bin0~bin11111111, Cr_qspis_datamode=3'b100)



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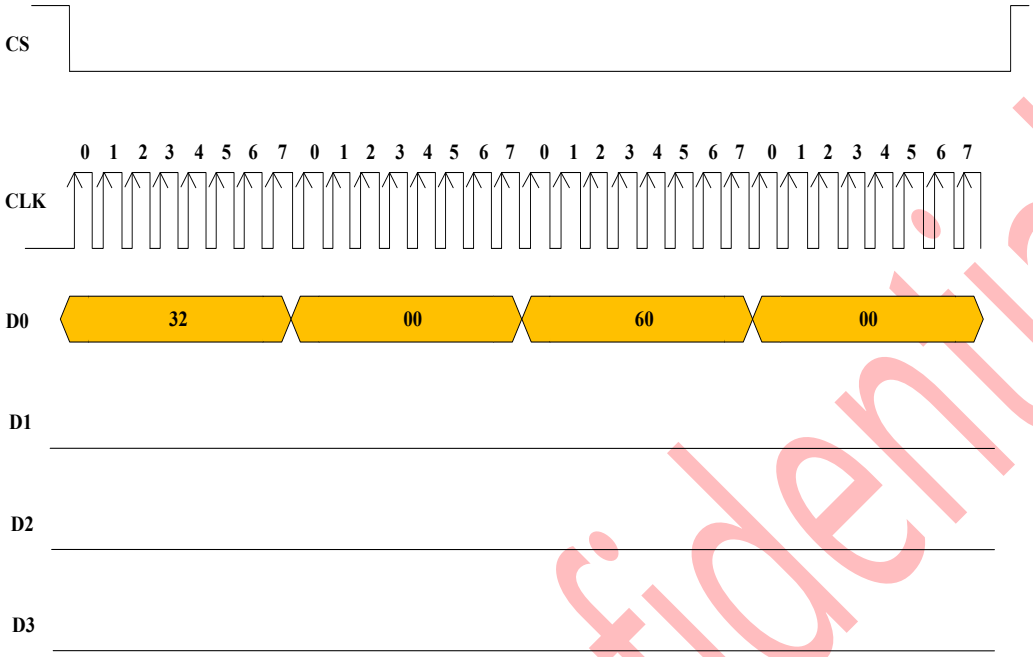
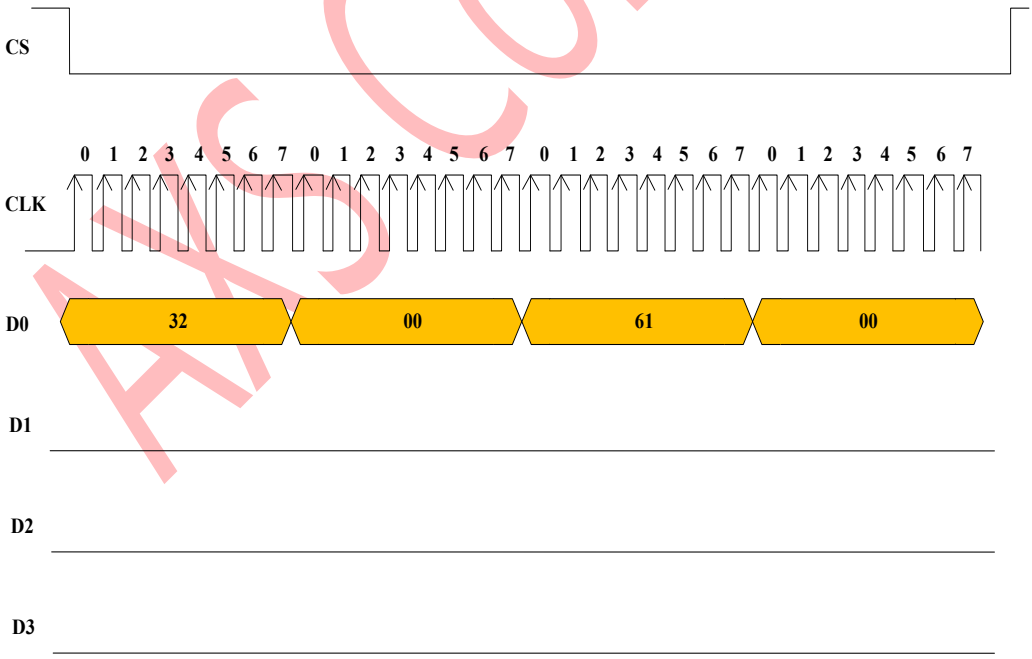
5.4.4. QSPI ramless

5.4.4.1.1. Vsync (cr_qspis_vidvs_code)



5.4.4.1.2. Hsync (cr_qspis_vidhs_code)



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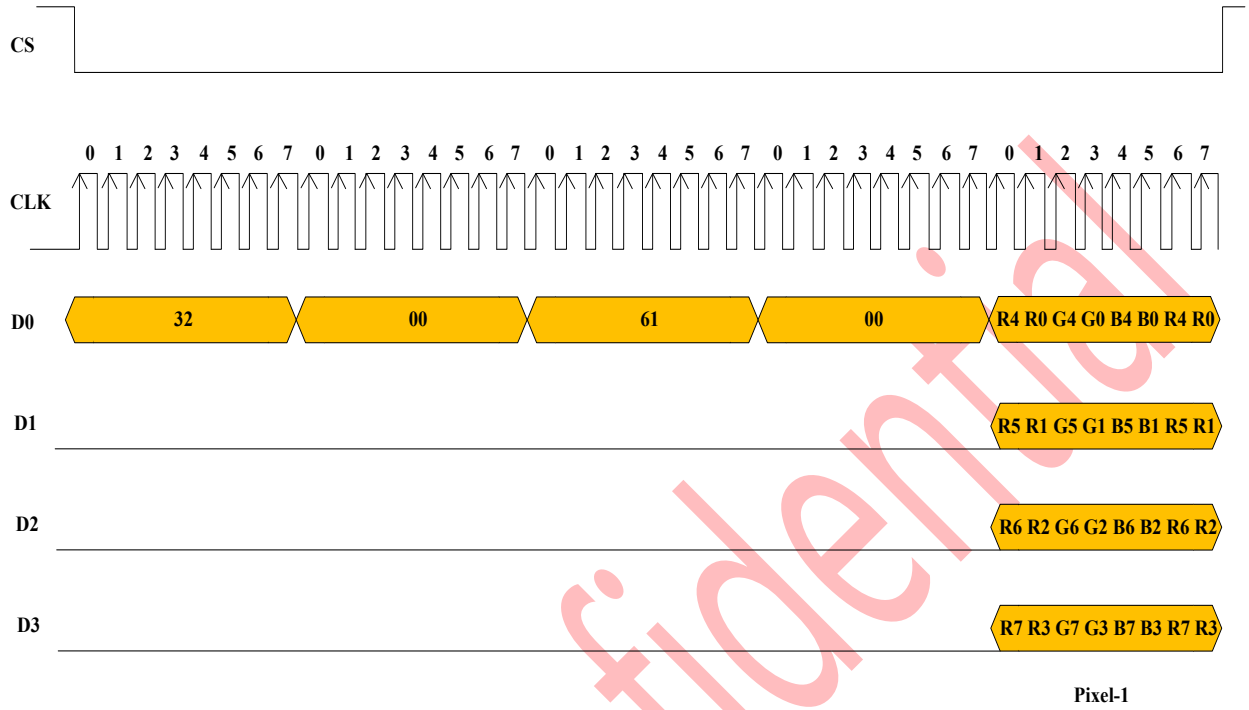
5.4.4.1.3. Pixstream (cr_qspis_vidhs_code)



5.5. 8080-Series MCU Interface

5.5.1. 8080-Series MCU Write Cycle Sequence

he write cycle means that the host writes information (register index / parameter) to the display via the interface. Each write cycle (WRX high-low-high sequence) consists of 3 control signals (D/CX, RDX, WRX) and data signals (DB[17:0]). D/CX is a control signal, which tells if the data is an index or a parameter. The data signals represent index number if the signal is low (D/CX=’0’) and vice versa the data signals represent parameter (D/CX=’1’).

5.5.2. 18-bit 8080-Series Interface Write Format

The 18-bit 8080-series interface is selected by setting the IM [3:0] =”1000”..

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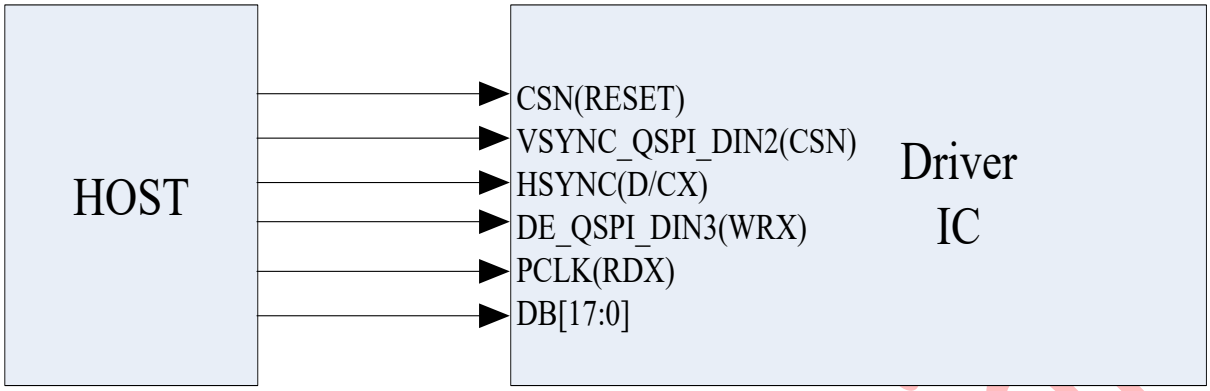

18-bit 8080-Series Interface Connection

This mode accepts only 262k colors format in display. In this interface, index, parameter, and pixel-data should be written according to the following figures.

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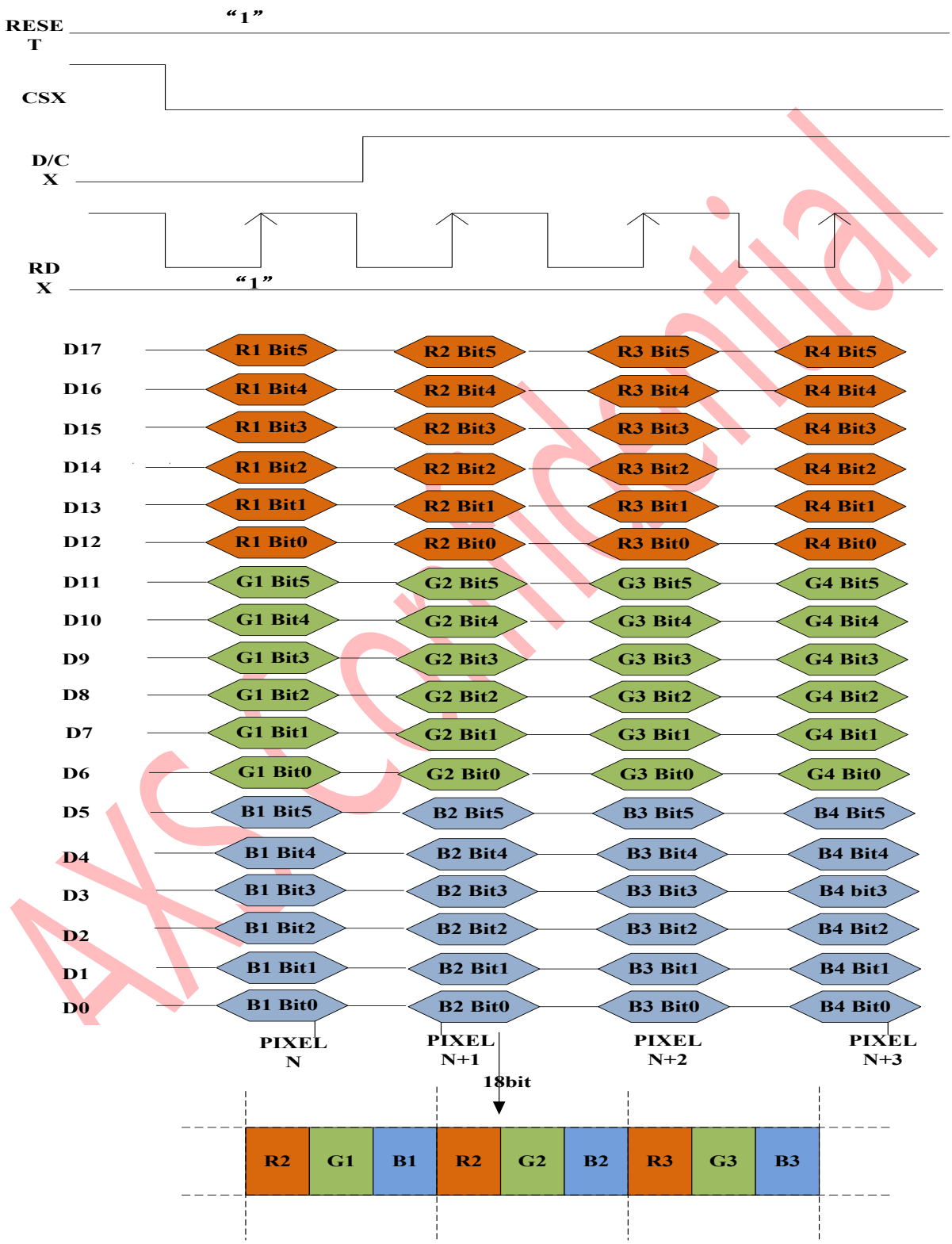
5.5.2.1. 18-bit data bus for 18-bit/pixel (RGB-6-6-6-bit input)，262K-Colors)cr_dbi_format = 2'b01



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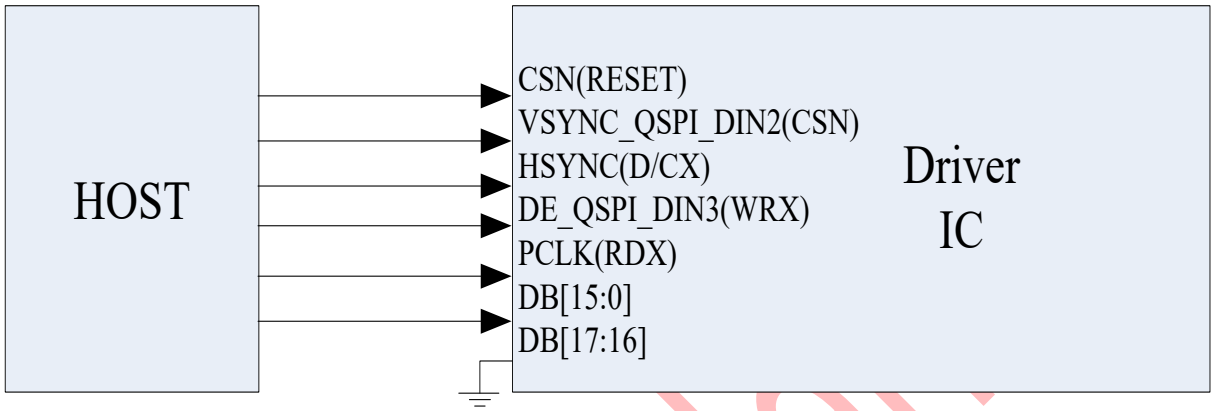
5.5.3. 16-bit 8080-Series Interface Write Format

The 16-bit 8080-series interface is selected by setting IM[3:0]="0111".



16-bit 8080-Series Interface Connection

AXS15231E accepts 262k-color or 65k-color format in this mode. When the 262k-color format is used, two transfers for each pixel are required.

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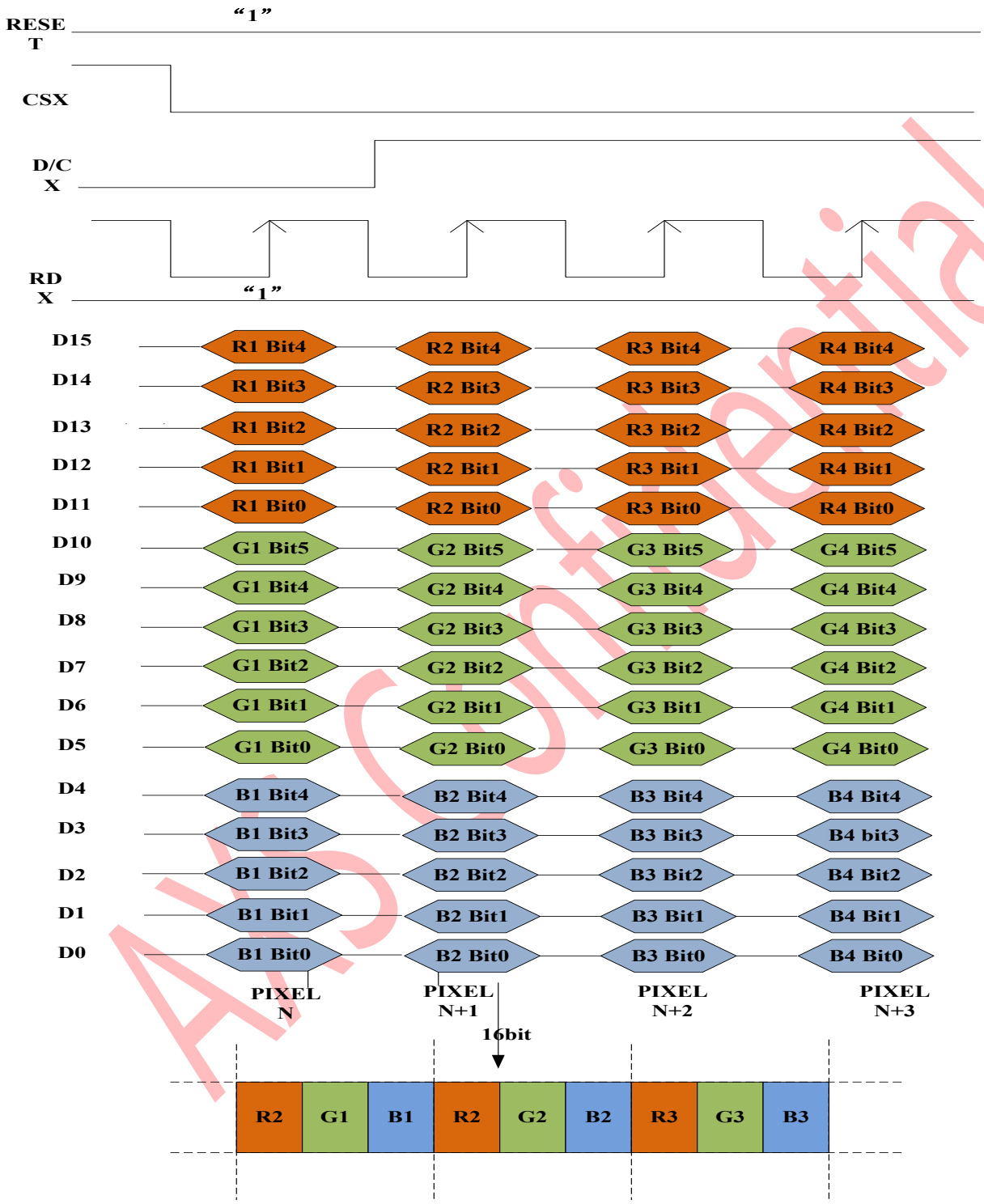
5.5.3.1. 16-bit data bus for 16-bit/pixel (RGB 5-6-5-bit input) 65K-Color, cr_dbi_format = 2'b00)



5.5.4. 9-bit 8080-Series Interface Write Format

The 9-bit 8080-series interface is selected by setting the IM [3:0] = "0110" and the DB [17:9] pins are used to transfer data. The display data is divided into upper part and lower part (9-bit for each part), and the upper part is

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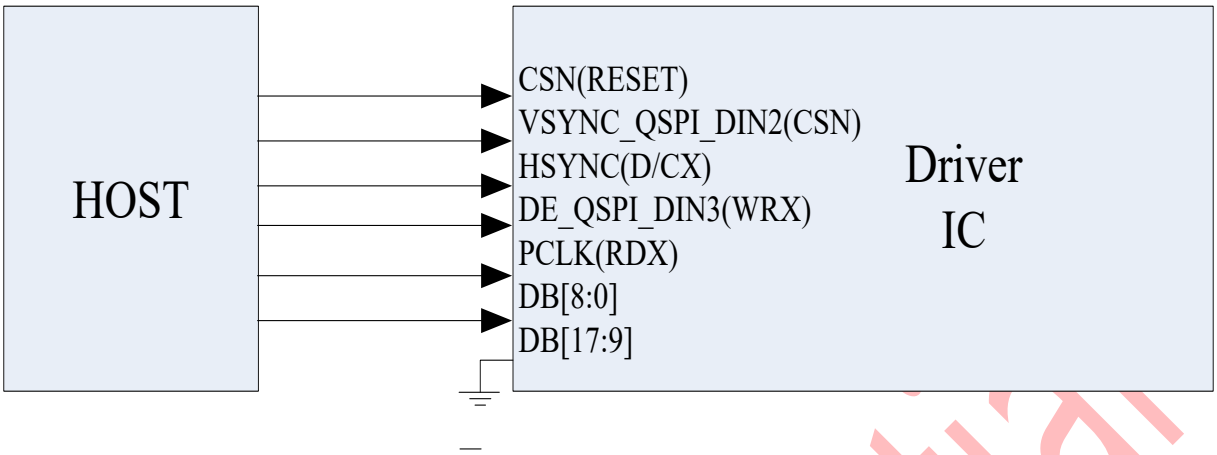
transferred first. The unused DB [8:0] pins must be tied to either VDDI or DGND.



9-bit 8080-Series Interface Connection

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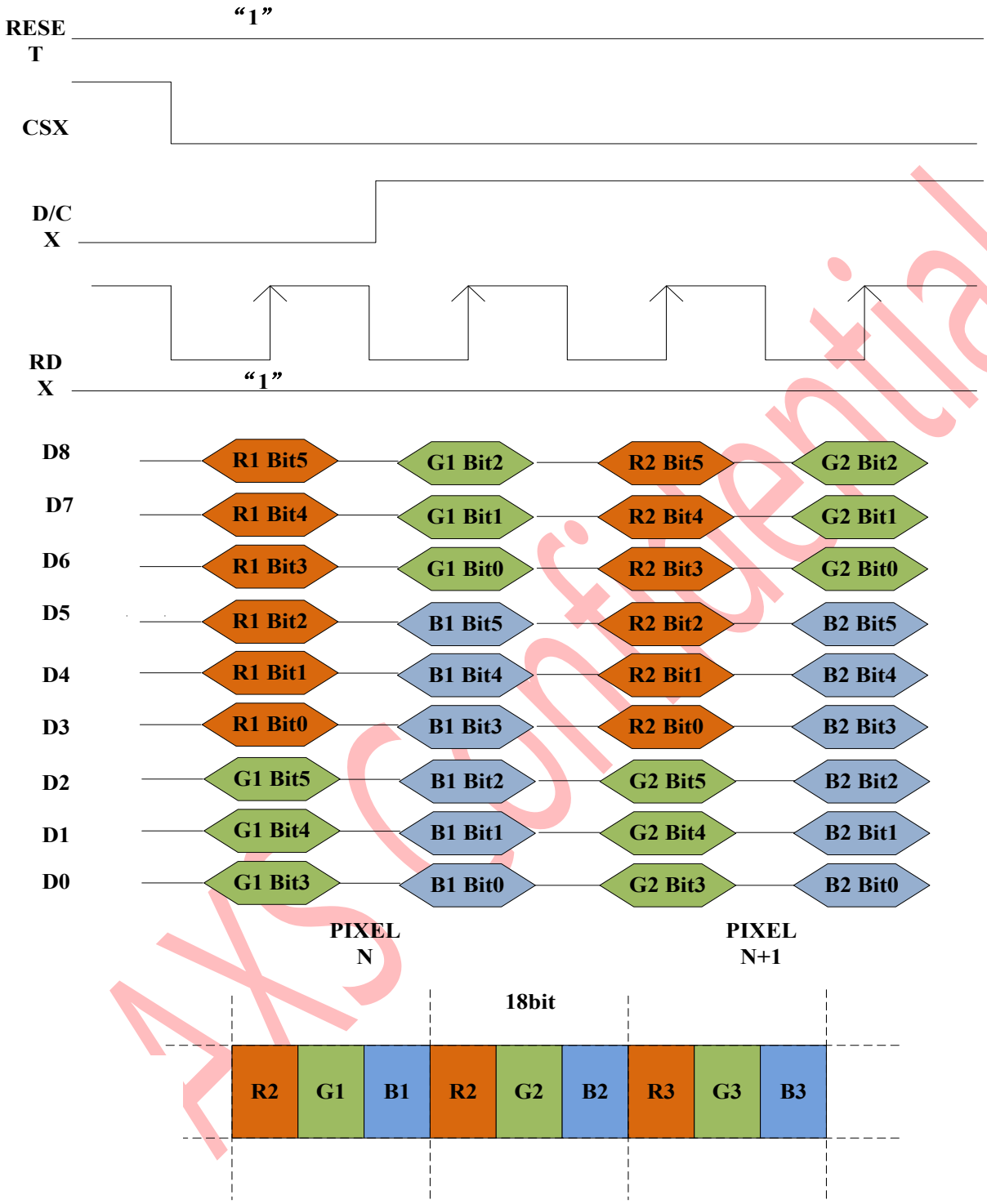
5.5.4.1. 9-bit data bus for 18-bit/pixel (RGB 6-6-6-bit input), 262K-Colors, cr_dbi_format = 2'b01



5.5.5. 8-bit 8080-Series Interface Write Format

The 8080 8-bit interface is selected by setting the IM [3:0] as "0101" and the DB [7:0] pins are used to transfer data.

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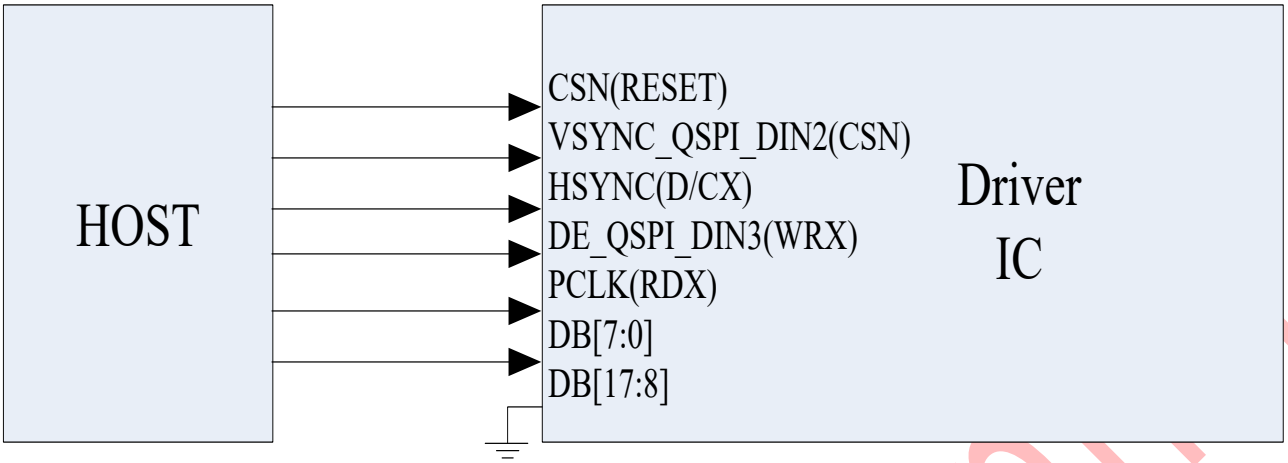
The mode accepts 262k-color or 65k-color format. The display data is divided into upper byte and lower byte, and the upper byte is transferred first. The written data is expanded into 18-bit internally (see the figure below) and then written into DRAM. The unused DB [17:8] pins must be tied to either VDDI or DGND.



8-bit 8080-Series Interface Connection

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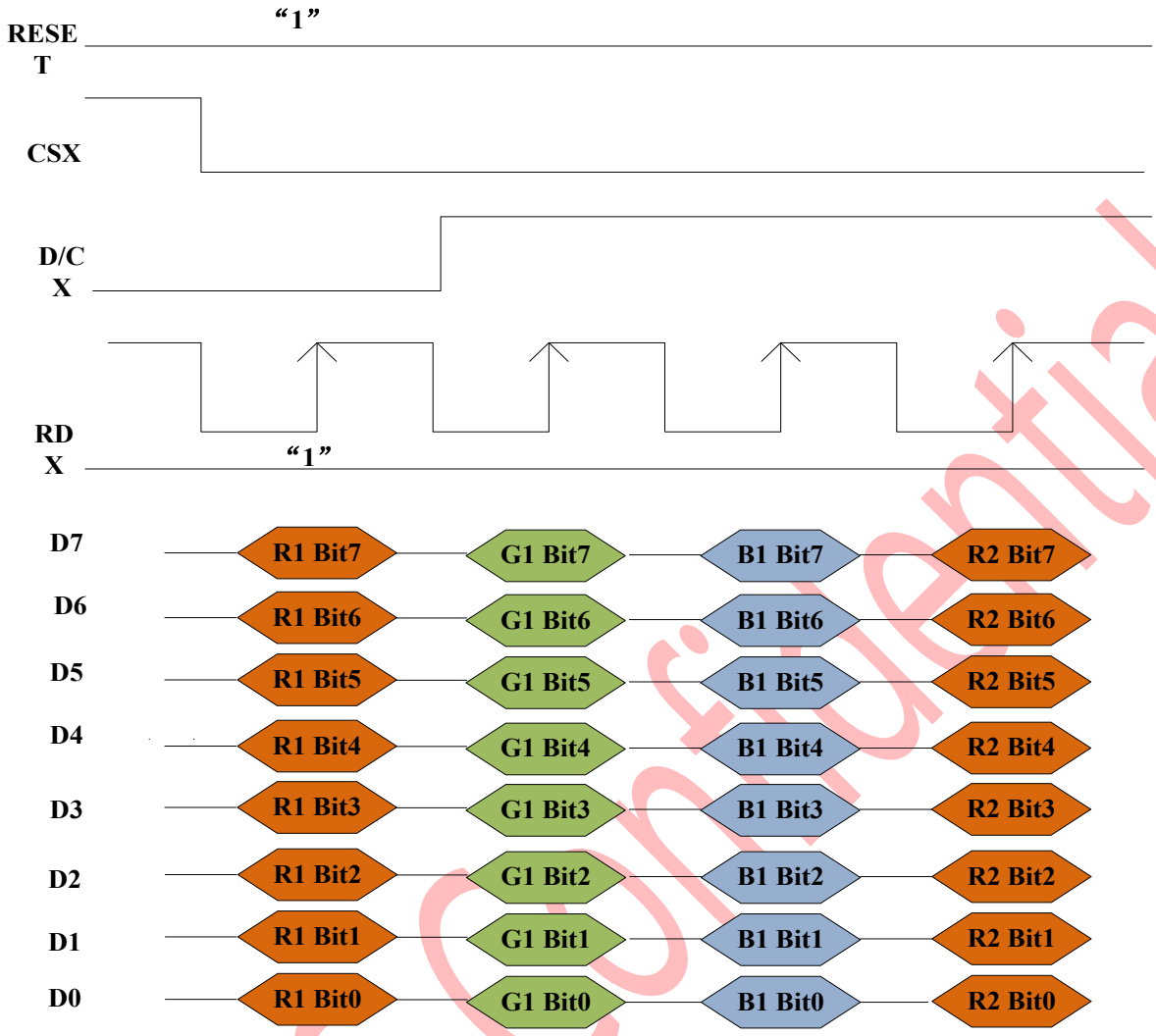
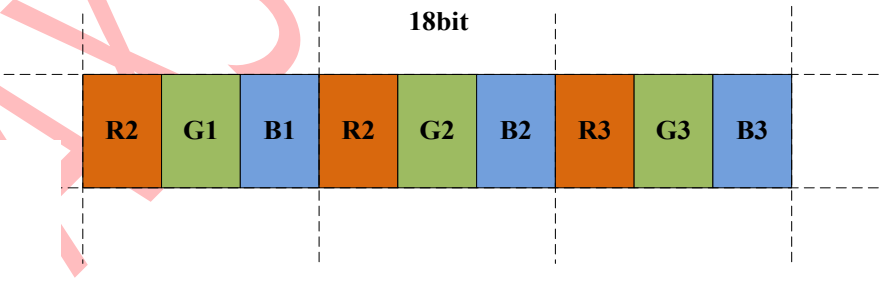
5.5.5.1. 8-bit data bus for 24-bit/pixel (RGB 8-8-8-bit input), 16.7M-Colors, cr_dbi_format = 2'b11





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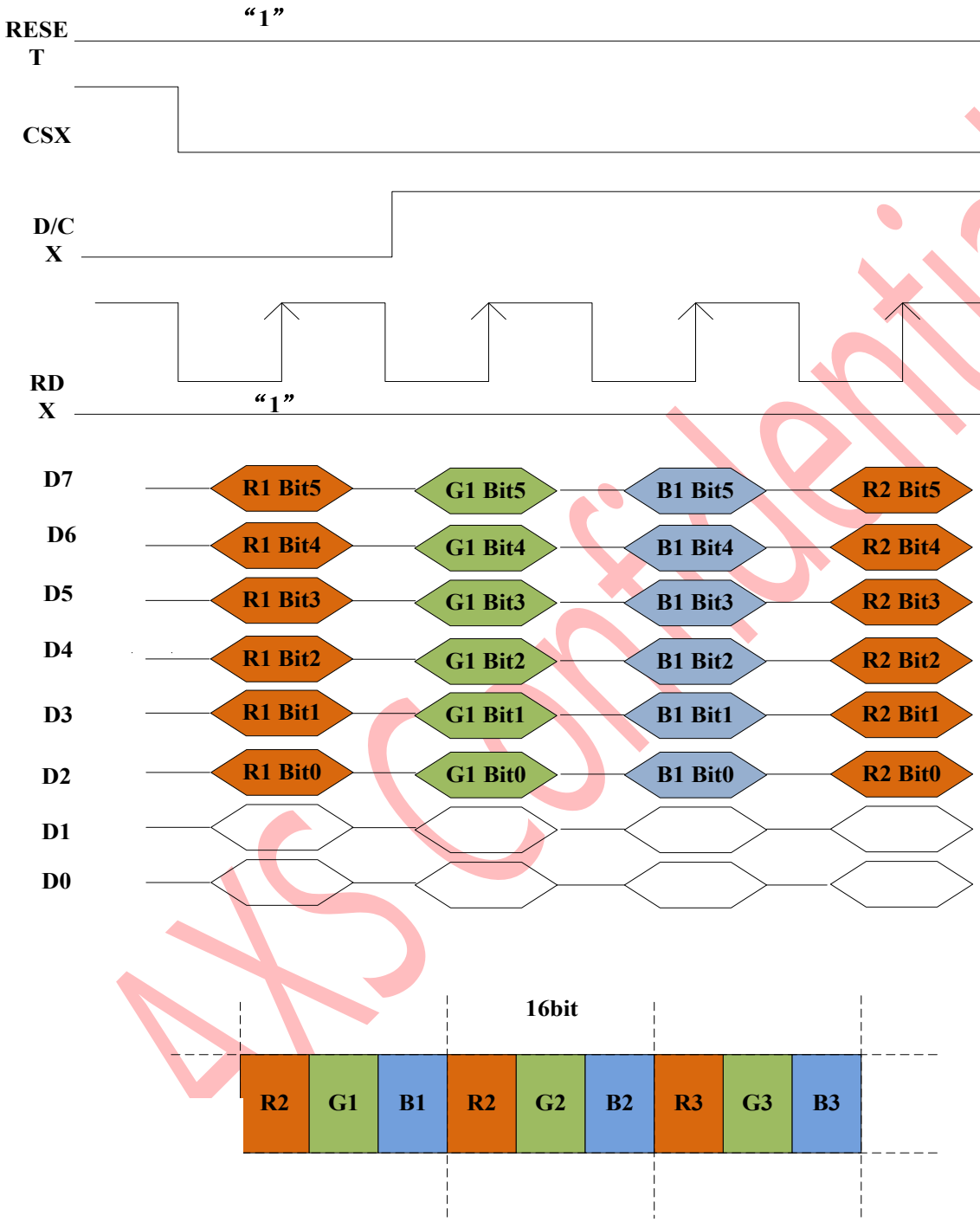
5.5.5.2. 8-bit data bus for 18-bit/pixel (RGB 6-6-6L-bit input), 262K-Colors, cr_dbi_format = 2'b01



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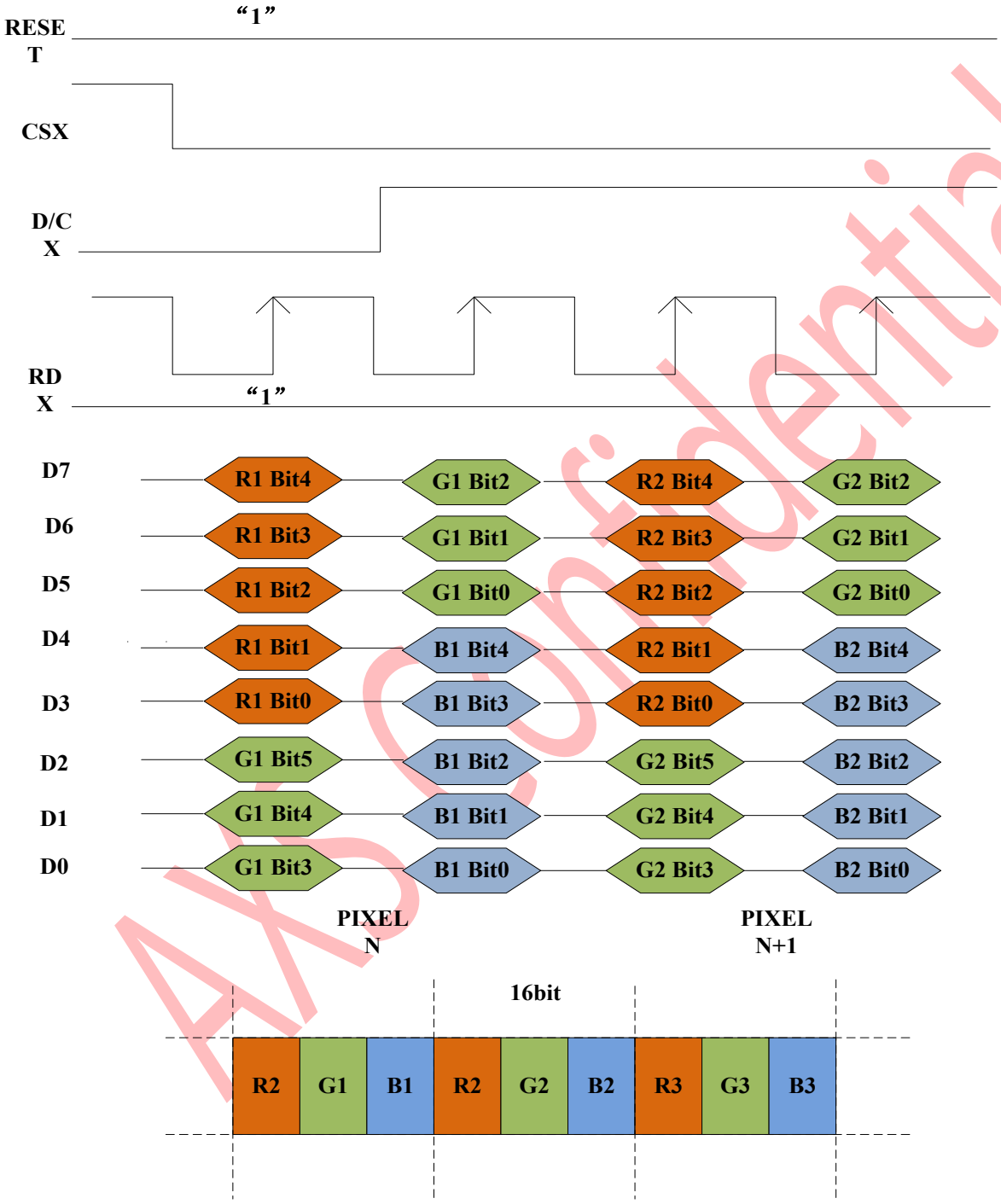
5.5.5.3. 8-bit data bus for 16-bit/pixel (RGB 5-6-5-bit input), 65K-Colors, cr_dbi_format = 2'b00



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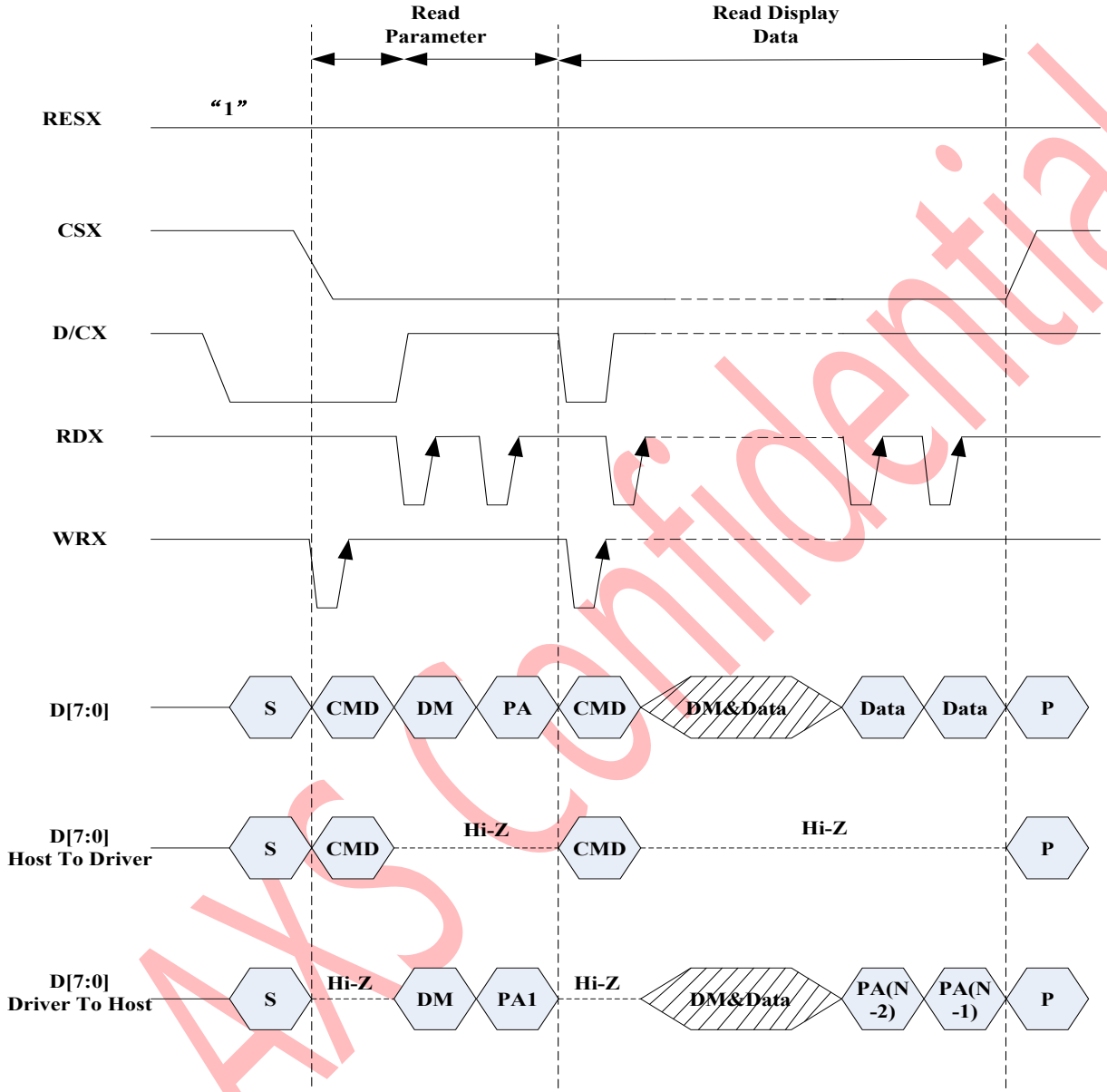
5.5.6. 8080-Series MCU Read Cycle Sequence

The read cycle (RDX high-low-high sequence) means that the host reads information from display via interface. The driver sends data (DB [7:0]) to the host when there is a falling edge of RDX and the host reads data when there is a rising edge of RDX.



8080-series interface read Protocol,read data from register

5.5.6.1.1. 8-bit data bus

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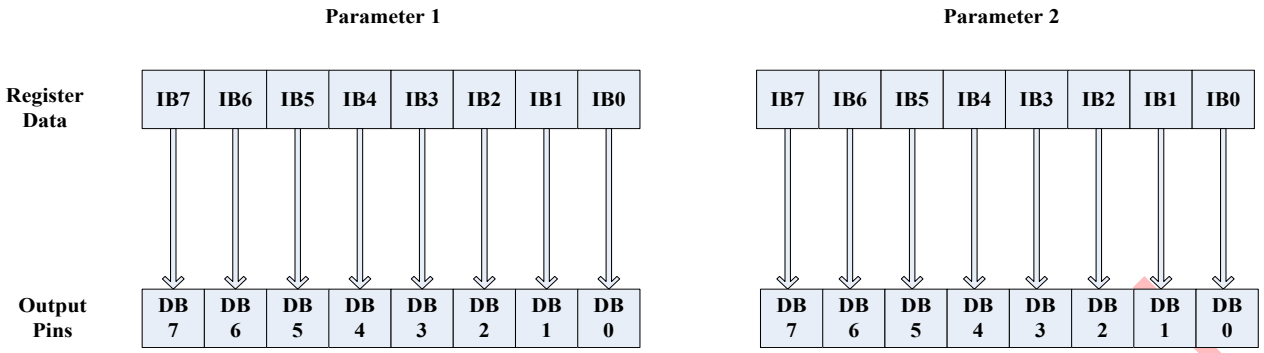

5.6. RGB Interface

5.6.1. RGB Color Format

AXS15231E supports two kinds of RGB interface, DE mode， and 16bit/18bit data format. When DE mode is selected and the VSYNC, HSYNC, DOTCLK, DE, D[17:0] pins can be used; When using RGB interface, only serial interface can be selected. IM [3:0] as “0010”or“0011”。

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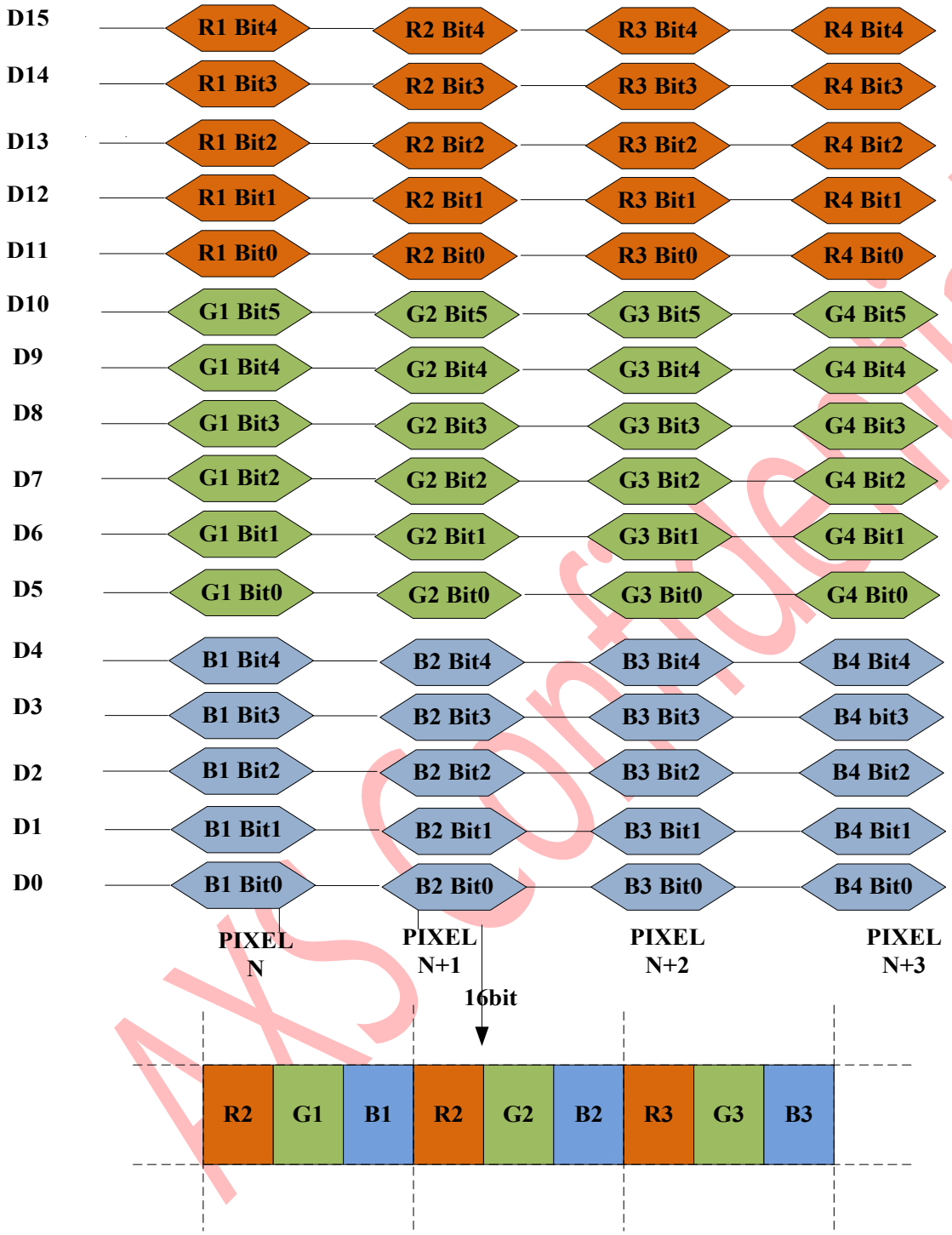
5.6.1.1. Write data for 16-bit/pixel (RGB 5-6-5-bit input), 65K-Colors，cr_ext_format = 00



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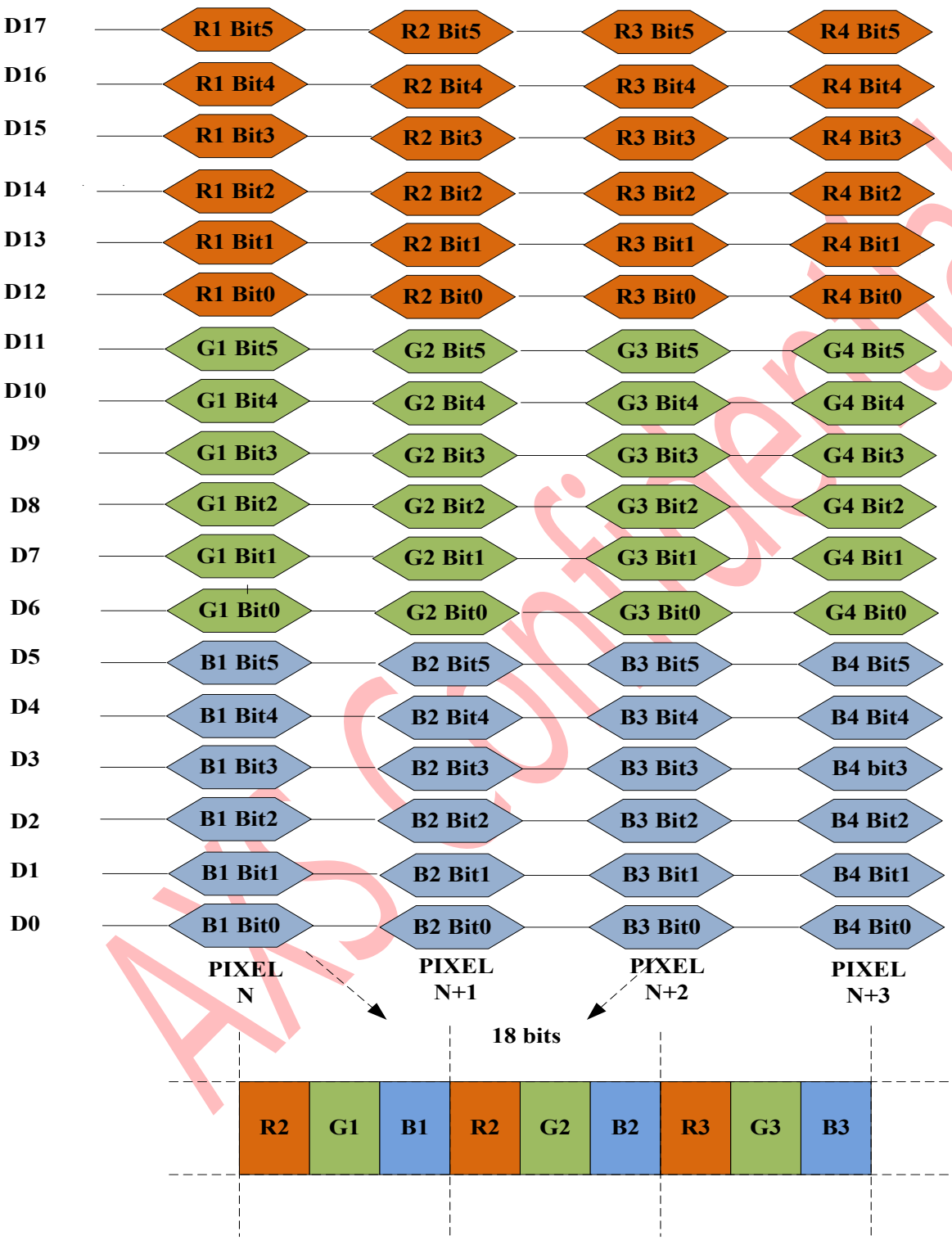
5.6.1.2. Write data for 18-bit/pixel (RGB 6-6-6-bit input), 262K-Colors，cr_ext_format = 01



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5.6.2. sRGB Color Selection

AXS15231E supports sRGB interface, DE mode， with rgb565, rgb666,rgb888 format. When DE mode is selected and the VSYNC, HSYNC, DOTCLK, DE, D [7:0] pins can be used; When using RGB interface, only serial interface can be selected. IM [3:0] as “1011”or“1100”。

The color format selection of RGB Interface for AXS15231E is selected by setting the IM and command 3Ah, DB [7:0].

IM	3Ah	RGB Interface Mode	Data pins
1011	101	3-SPI with RGB565	DB[7:2]/ DB[5:0]
1011	110	3-SPI with RGB666	DB[7:2] /DB[5:0]
1011	111	3-SPI with RGB888	DB[7:0]
1100	101	4-SPI with RGB565	DB[7:2] /DB[5:0]

5.6.2.1. RGB Color Format

In RGB565 and RGB666 formats, the register cr_rgb_chose_h can be used to configure whether the valid bit-width of each byte is the upper 5/6 bits or the lower 5/6 bits. By default, the register is set to 0, which selects the upper 5/6 bits as valid data. The data format is arranged as shown in the figure below.

serial RGB 565

Pin	1st Data	2nd Data	3rd Data	...	(3N+1)th Data
DAP[0]	x	x	x	...	x
DAP[1]	x	x	x	...	x
DAP[2]	x	1'G0	x	...	x
DAP[3]	1'R0	1'G1	1'B0	...	N'R0
DAP[4]	1'R1	1'G2	1'B1	...	N'R1
DAP[5]	1'R2	1'G3	1'B2	...	N'R2
DAP[6]	1'R3	1'G4	1'B3	...	N'R3
DAP[7]	1'R4	1'G5	1'B4	...	N'R4

serial RGB 666

Pin	1st Data	2nd Data	3rd Data	...	(3N+1)th Data
DAP[0]	x	x	x	...	x
DAP[1]	x	x	x	...	x
DAP[2]	1'R0	1'G0	1'B0	...	N'R0
DAP[3]	1'R1	1'G1	1'B1	...	N'R1
DAP[4]	1'R2	1'G2	1'B2	...	N'R2
DAP[5]	1'R3	1'G3	1'B3	...	N'R3
DAP[6]	1'R4	1'G4	1'B4	...	N'R4
DAP[7]	1'R5	1'G5	1'B5	...	N'R5

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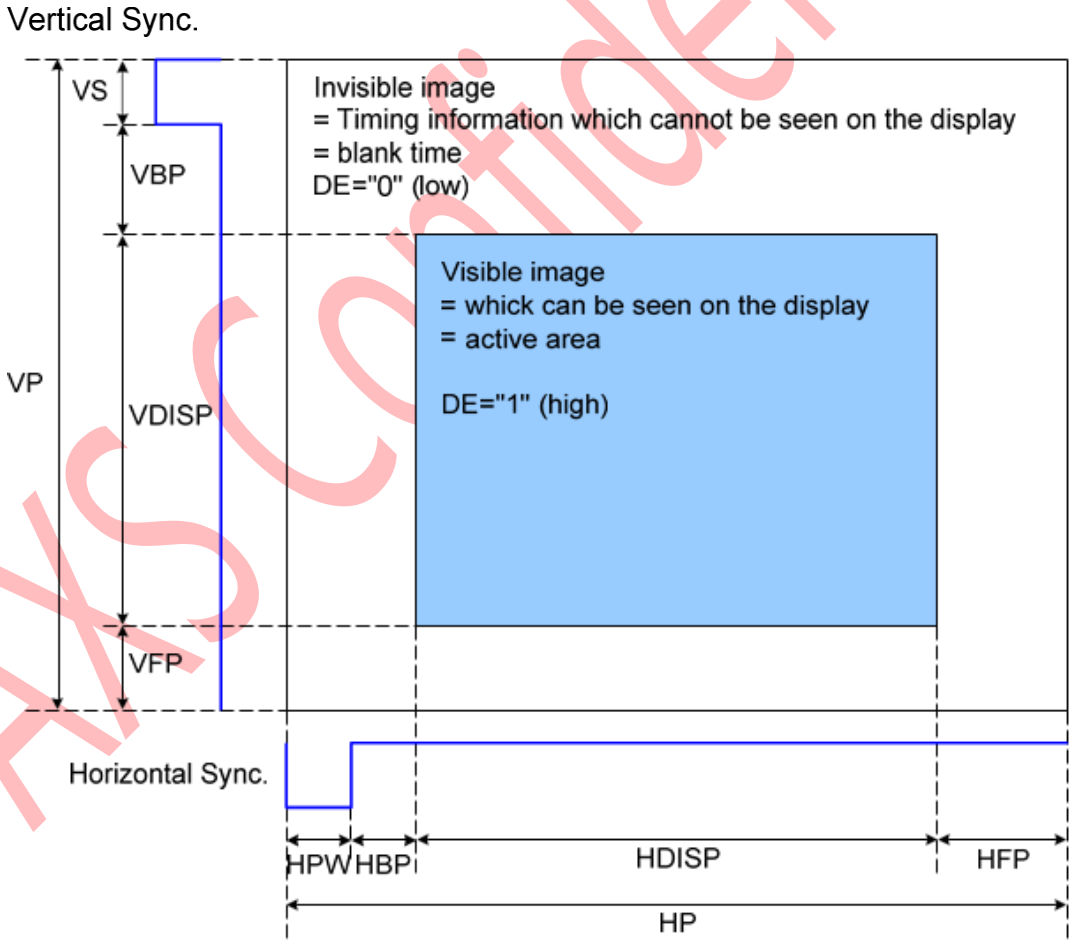
serial RGB 888					
Pin	1st Data	2nd Data	3rd Data	...	(3N+1)th Data
DAP[0]	1'R0	1'G0	1'B0	...	N'R0
DAP[1]	1'R1	1'G1	1'B1	...	N'R1
DAP[2]	1'R2	1'G2	1'B2	...	N'R2
DAP[3]	1'R3	1'G3	1'B3	...	N'R3
DAP[4]	1'R4	1'G4	1'B4	...	N'R4
DAP[5]	1'R5	1'G5	1'B5	...	N'R5
DAP[6]	1'R6	1'G6	1'B6	...	N'R6
DAP[7]	1'R7	1'G7	1'B7	...	N'R7

Figure 2 RGB Interface Data Format

5.6.3. RGB Interface Definition

The display operation via the RGB interface is synchronized with the VSYNC, HSYNC, and DOTCLK signals. The data can be written only within the specified area with low power consumption by using window address function. The back porch and front porch are used to set the RGB interface timing.



DRAM Access Area by RGB Interface

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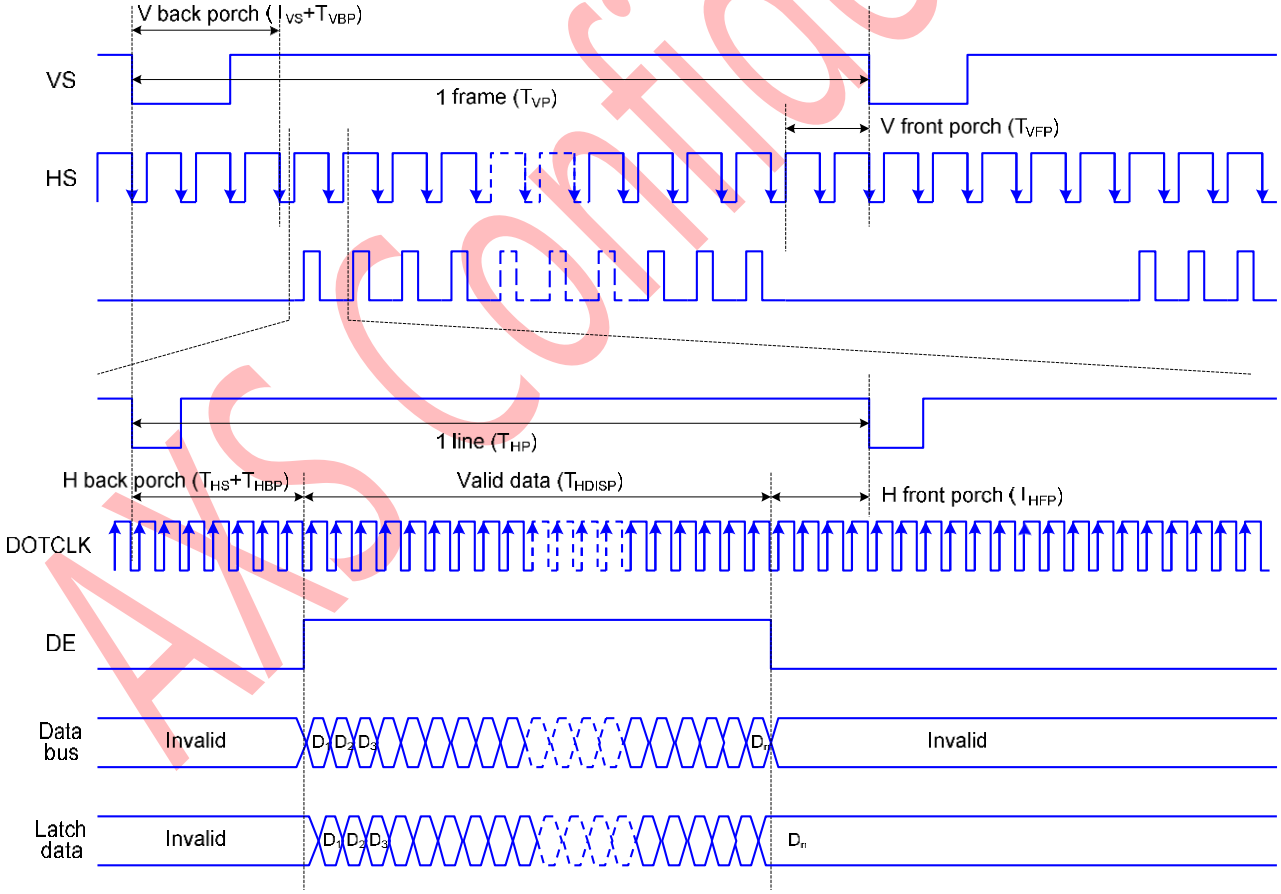
Please refer to the following table for the setting limitation of RGB interface signals.

Parameter	Symbol	Min.	Typ.	Max.	Unit
Horizontal Sync. Width	hpw	2	-	hpw+hbp=75	Clock
Horizontal Sync. Back Porch	hbp	20	-		Clock
Horizontal Sync. Front Porch	hfp	20	38	-	Clock
Vertical Sync. Width	vs	2	4	-	Line
Vertical Sync. Back Porch	vbp	2	4		Line
Vertical Sync. Front Porch	vfp	2	8	-	Line

5.6.4. RGB Interface Timing

The timing chart of RGB interface DE mode is shown as follows.



Note: The setting of front porch and back porch in host must match that in IC as this mode. VSYNC, HSYNC, and DOTCLK signals must be supplied during a display operation period.

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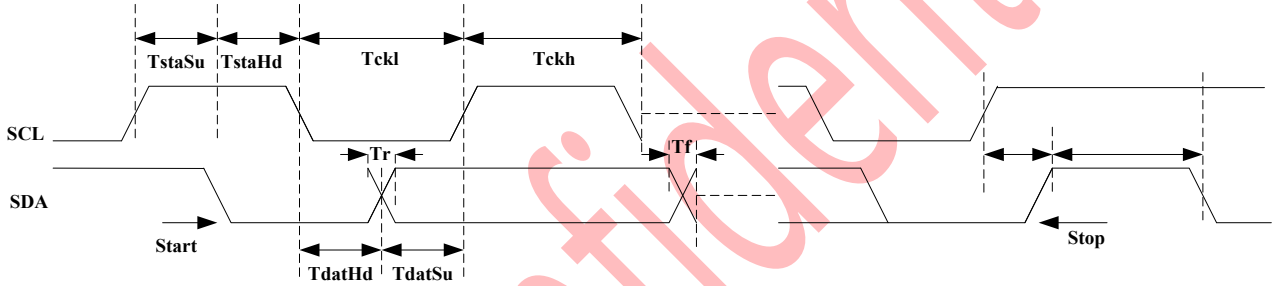
In RGB interface mode, the panel controlling signals are generated from DOTCLK, not the internal clock generated from the internal oscillator.

When switching between the internal operation mode and the external display interface operation mode, follow the sequences below in setting instruction.

In RGB interface mode, the front porch period continues until the next VSYNC input is detected after drawing one frame.In RGB interface mode, a RAM address is set in the address counter every frame on the falling edge of VSYNC.

5.7. Touch part interface

5.7.1. I2C Interface



Parameter	Symbol	Min.	Typ	Max.	Unit
Working Frequency	F_{clk}	20	-	400	Khz
I2C Clock Low	T_{CKL}	1300	-	-	ns
I2C Clock High	T_{CKH}	600	-	-	ns
I2C Clock and Data rising time	T_r	-	-	300	ns
I2C Clock and Data falling time	T_f	-	-	300	ns
I2C Data hold time	T_{DatHd}	0	-	-	ns
I2C Data setup time	T_{DatSu}	100	-	-	ns
I2C Start Condition hold time	T_{StaHd}	600	-	-	ns
I2C Start Condition setup time	T_{StaSu}	600	-	-	ns
I2C Stop Condition setup time	T_{StpSu}	600	-	-	ns
I2C Bus free time	$T_{BusFree}$	1300	-	-	ns

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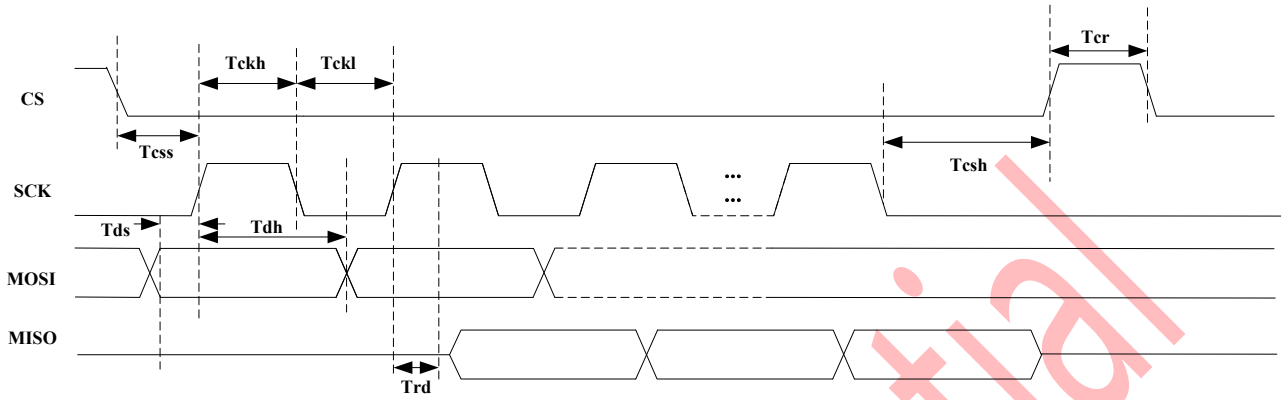
5.7.2. SPI Interface



SPI Timing

Parameter	Symbol	Min.	Typ	Max.	Unit
SCK Frequency	f_{SCK}			16	Mhz
CS Set-up Time	t_{CSS}	200			ns
CS Hold Time	t_{CSH}	200			ns
CS Recovery Time	t_{CR}	1			ns
SCK clock High Time	t_{CKH}	31.25			ns
SCK clock Low Time	t_{CKL}	31.25			ns
Data Output Delay Time	t_{RD}			50	ns
Input Data Set-up Time	t_{DS}	25			ns
Input Data Hold Time	t_{DH}	25			ns

5.8. Display Reference Clock Function

The AXS15231E provides a function to decide internal oscillator for display clock reference of driver IC.

Relationship between Liquid Crystal Driver Duty and the Frame Frequency

The formula below is used to calculate the relationship between the liquid crystal driver duty and the frame frequency. The frame frequency is determined by setting the 1H period adjustment (RTN) bit.

RTN setting for 1H period:

Step1: To decide real one line period in Command Mode:

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$$RTN = 1H(period) = \frac{Fosc - 5\%}{(Line + BP + FP) * FrameRate(Hz)}$$

$$RTN = 1H(period) = \frac{F_{pll} - 5\%}{(Line + BP + FP) * FrameRate(Hz)}(us)$$ (Note.1, Note.2, Note.3)

RTN: Number of clocks per line.
Line: Display Line Number
FP: Number of lines for the front porch.
BP: Number of lines for the back porch.
Note.1: The RTN formula can cover full temp range variation (75℃ ~ -30℃)
Note.2: When Touch function ON (must take account of DP/TP ratio)
Note.3: For detailed RTN calculation method, please contact AXS.

5.9. Gamma Function

The structure of the grayscale amplifier is shown below. The 15 voltage levels between VSPR/VSNR and GND determined by the gradient adjustment register, the reference adjustment register, the amplitude adjustment resister and the micro-adjustment register.

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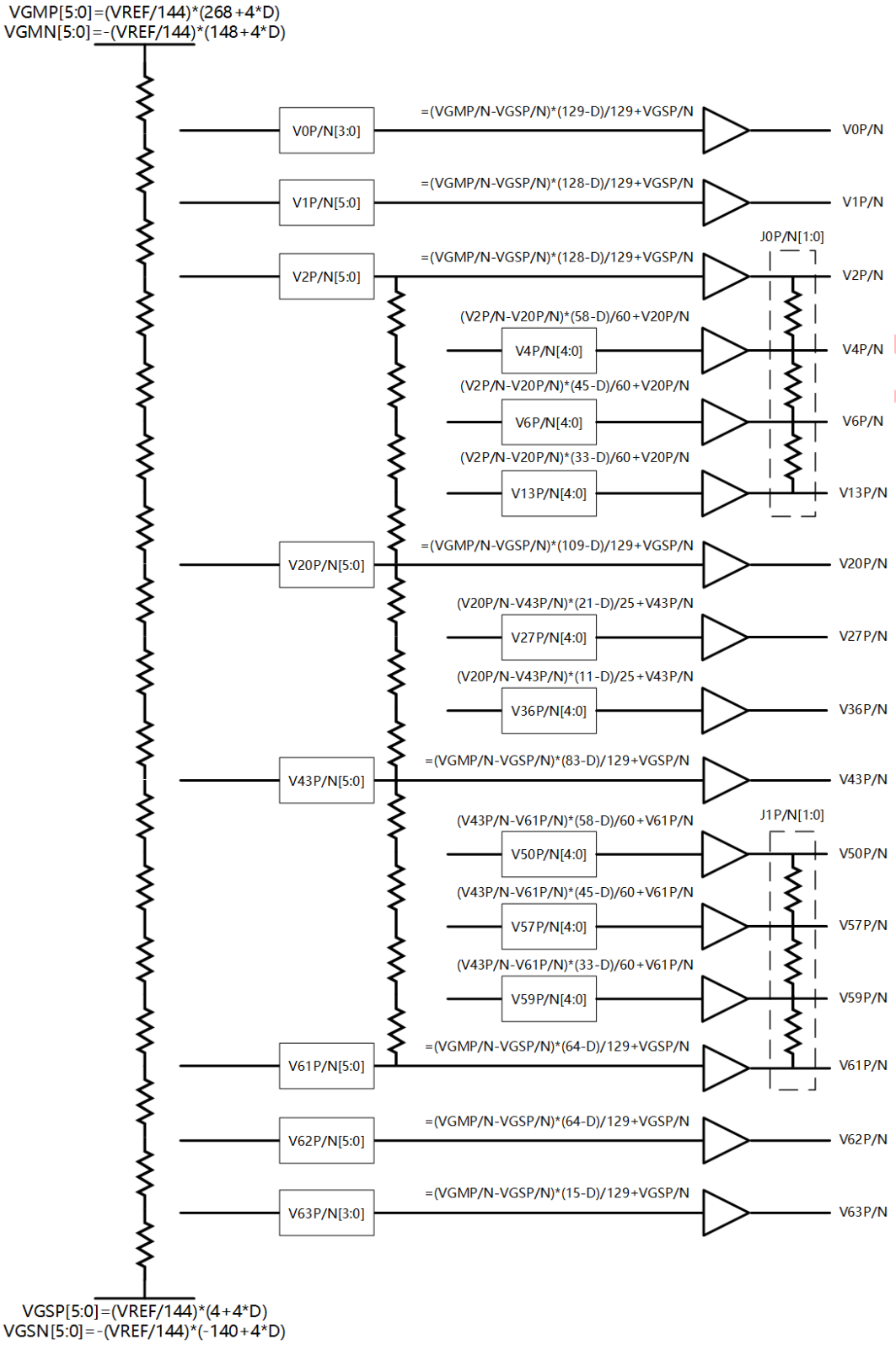

Figure：Gamma Architecture for AXS15231E

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5.10.Reset Function

The RESET function of AXS15231E is triggered by a RESX input. After reset function triggered, the AXS15231E enter a reset period, and the duration of this period must be at least 5ms. During this period, the AXS15231E and its power circuit will be initialized.

Initial States of Output Pins

The following table represents the output pins and its initial state (2-power mode: VCI, IOVCC).

Output Pins	Initial State
S<540:1>	GND
SX<98:3>	GND
VCOM	Disabled (GND level output)
GOUT_L[12:1], GOUT_R[12:1]	Disabled (GND level output)
LED_PWM	Disabled (GND level output)
VGH	Disabled (Hi-z)
VGL	Disabled (Hi-z)
VGHO	Disabled (Hi-z)
VGLO	Disabled (Hi-z)
VDD	1.2~1.48v
VREF	1.8v
VREF_TP	Disabled (Hi-z)
VCG_TP	Disabled (Hi-z)

5.11.Driver Operation Mode

AXS15231E driver can work in four operation modes of Reset State, Power Off state, Power On state and Display On State.

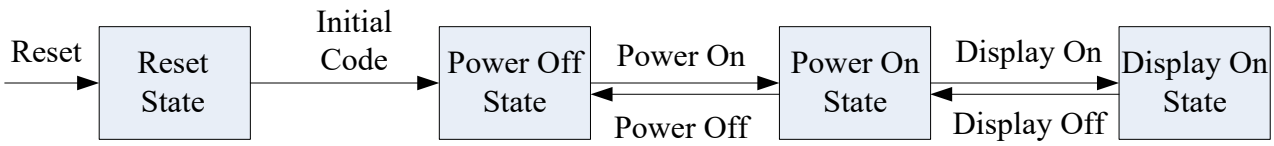
After reset, AXS15231E driver is in Reset state. In this state, all configurations are not initialized. Driver powers are not setup.

Initial code can be loaded from internal OTP or external flash or sent by host via MIPI interface. After the Initial code is loaded, AXS15231E driver enters Power Off state. AXS15231E driver is configured but powers are not up.

Power on command is sent from the Host. AXS15231E driver changes to Power On state on receiving power on command. All powers will be generated internally.

In Power on state, display on command can turn on the data path for display.

In Display on state, display off command can turn AXS15231E driver to Power On state and power off command can turn it to Power Off state.



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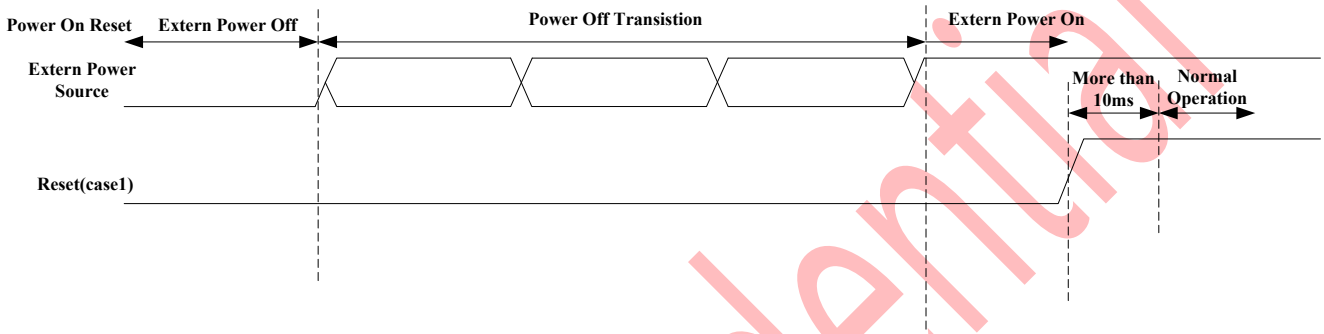
5.11.1. Timing of Reset Pin

AXS15231E provides H/W pin to do driver IC initialization. For power-on reset, one-finger reset (Case1) methods can be applied to do driver IC initialization. The detailed H/W reset pin timing is shown as below.
Of the two methods, RESET(Case 2) is recommended.



H/W reset pin timing for power-on reset

5.12. Tear Effect Information

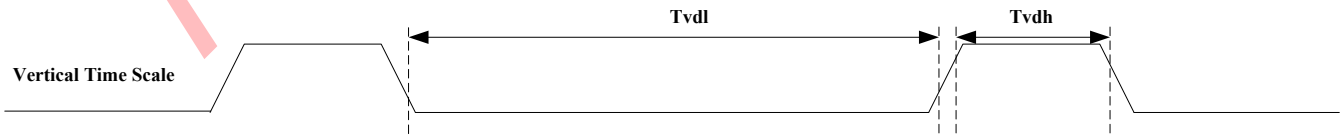
5.12.1. General

Tearing Effect line supplies to the MCU a Panel synchronization signal and this signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect Signal is defined by the Parameter of the Tearing Effect Line On command

5.12.2. Tearing effect line models

The Tearing Effect line supplies to the MCU a Panel synchronization signal and this signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect Signal is defined by the Parameter of the Tearing Effect Line On command.

Mode1: The Tearing Effect Output signal consists of V-Sync information only:



tvdh = The display panel is not updated from the Frame Memory.
tvdl = The display panel is updated from the Frame Memory (except Invisible Line – see below).

Mode 2: The Tearing Effect Output signal consists of V-Sync and H-Sync information; There is

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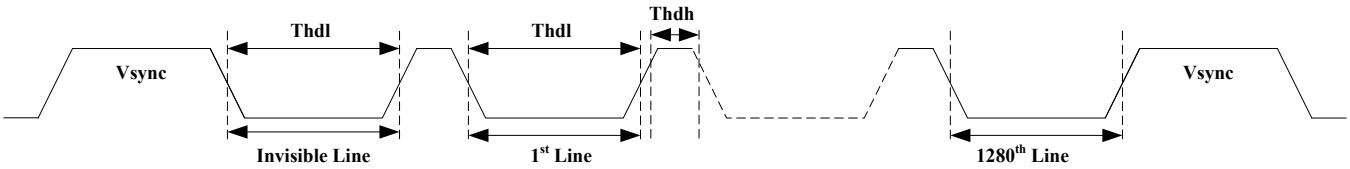
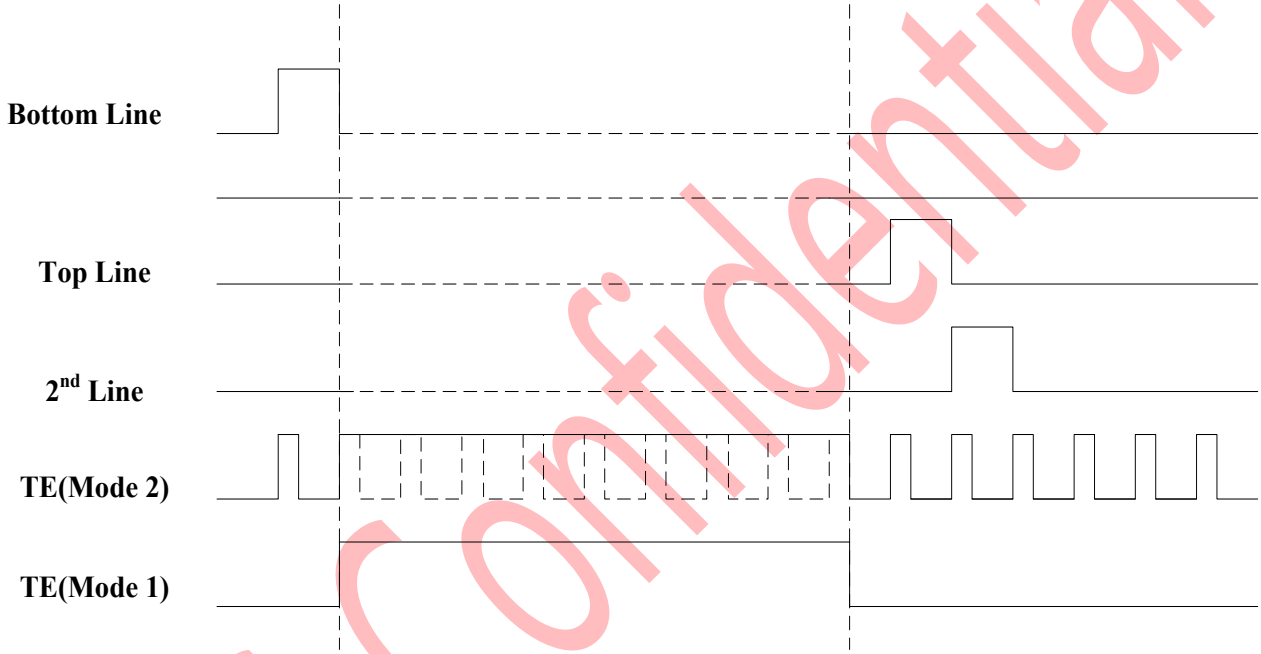
one V-sync and 4 H-sync pulses per field:



t_{vdh} = The display panel is not updated from the Frame Memory.

$t_{vd}l$ = The display panel is updated from the Frame Memory (except Invisible Line – see below).

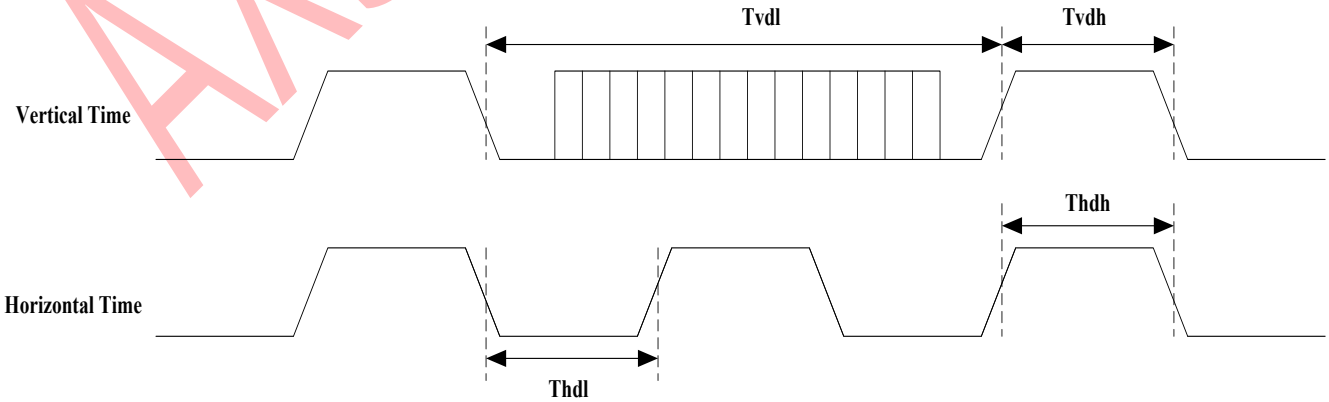
TE Line mode1 and Mode2 is shown as below graph:



Note: During Sleep In Mode, the Tearing Effect Output Pin is active Low.

5.12.2.1. Tearing effect line timing

The Tearing Effect signal is described below:



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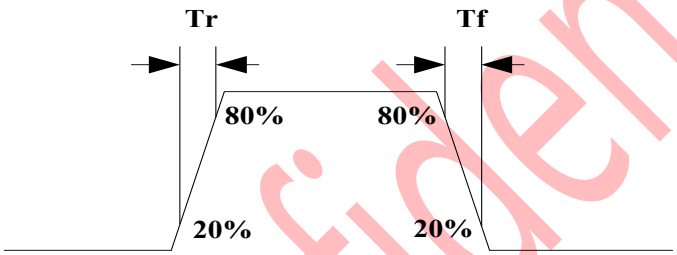
Symbol	Parameter	min	max	unit	description
tvdl	Vertical Timing Low Duration	13	-	ms	
tvdh	Vertical Timing High Duration	1000	-	µs	
thdl	Horizontal Timing Low Duration	16	-	µs	
thdh	Horizontal Timing Low Duration	-	500	µs	

Idle Mode Off/On

The TE signal rising and falling timing is described below:



5.13.OTP Programming Procedure

5.13.1. Power function description

The OTP control signals control data reading and writing, only load once when reset. According to the request of the OTP, reset signal need delay at least 20ns to generate control signal. And signal transition should be less than 1ns.

STEP: Write the register parameters, then use index read all index, if both consistent, to write read content into the OTP. This method requires each register readout parameters contend is the same as written contend before. Each number of parameter is the same. And it may waste OTP resources if did not in byte. In order to prevent the wrong, the rest of resource as a reserve. The content behind can cover the front.

In the program, Write the index and parameters, matching read contend with register number, and loading the content behind in register.

In addition, you can also load OTP after reset release, and programming OTP by external interface generating timing.

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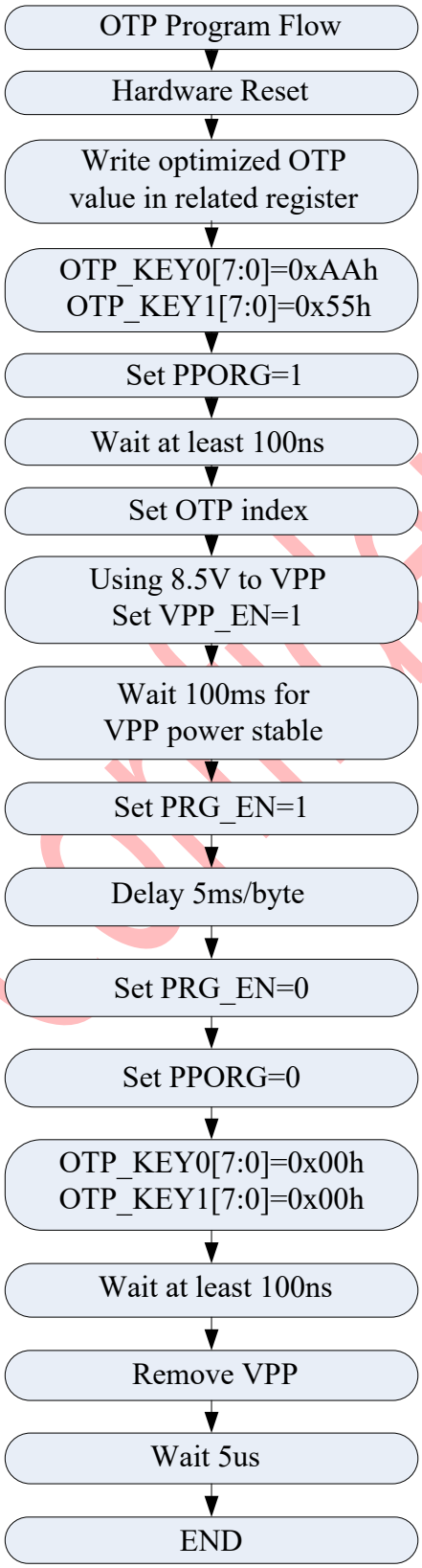
5.13.2. OTP program flow chart



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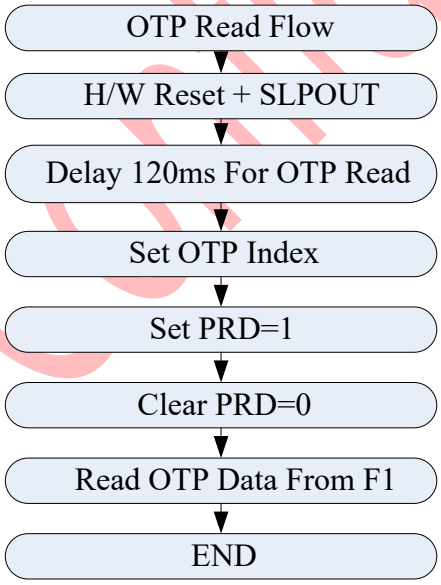
Step	External Power OTP Program Sequence
1	Power on and reset the module
2	Write optimized OTP value in related register
3	OTP_KEY 0xAA 0x55
4	Set PPORG=1, wait 100ns
5	Set OTP index
6	Use 8.5V to VPP, Set VPP_EN=1, wait 100ms
7	Set PRG_EN=1, wait 5ms/byte
8	Set PRG_EN=0
9	Set PPORG=0, wait 100ns
10	OTP_KEY 0x00 0x00
11	Remove VPP, wait 5us

5.13.3. OTP read program flow chart with External Power



When testing, connect signal with the test port, then observe the contend.

5.13.4. Timing description

Program timing：

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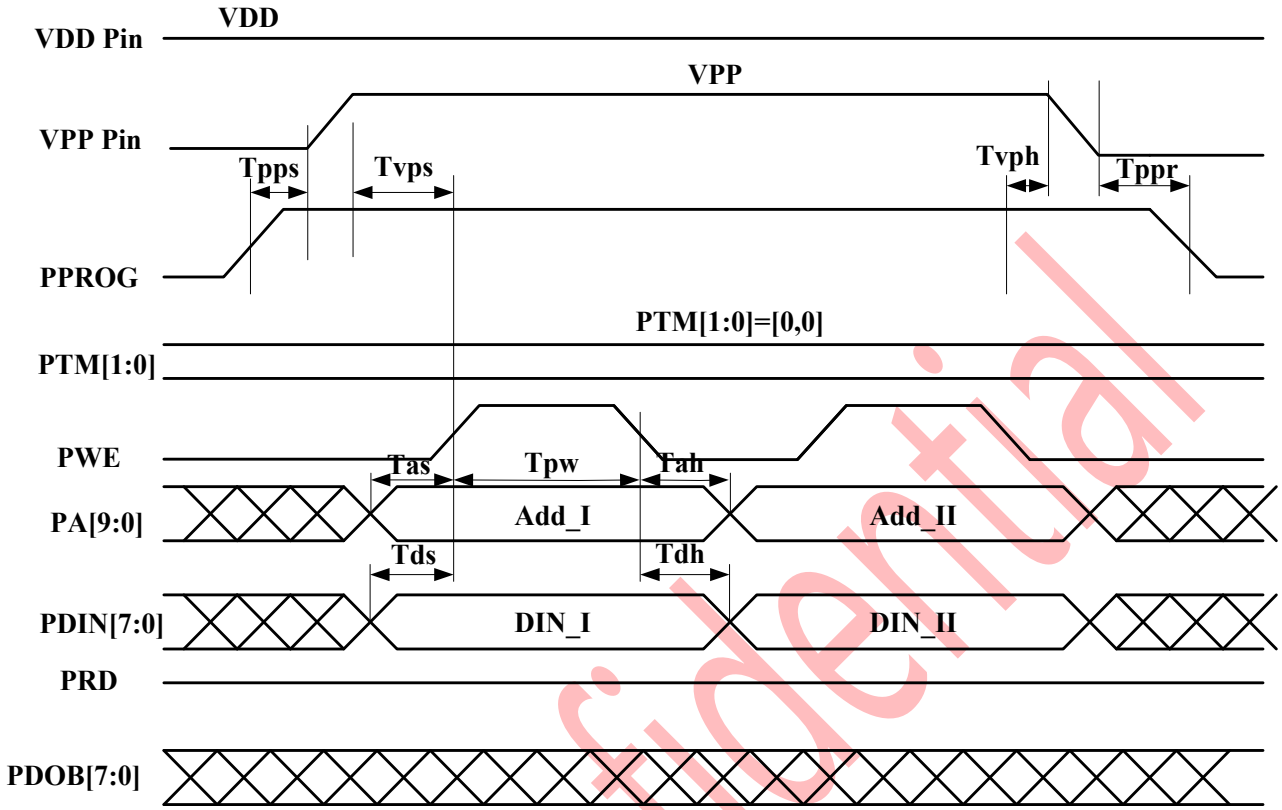

Parameter	Symbol	Min	Max	Unit
Address Setup Time	Tas	4	-	ns
Address Hold Time	Tah	9	-	ns
Data Setup Time	Tds	4	-	ns
Data Hold Time	Tdh	9	-	ns
Program Mode Setup Time	Tpps	10	-	ns
Program Mode Recovery Time	Tppr	10	-	ns
External VPP Setup Time	Tvps	0	-	ns
External VPP Hold Time	Tvph	0	-	ns
Program Pulse Width Time	Tpw	300	350	ns

load otp timing description, time is default value

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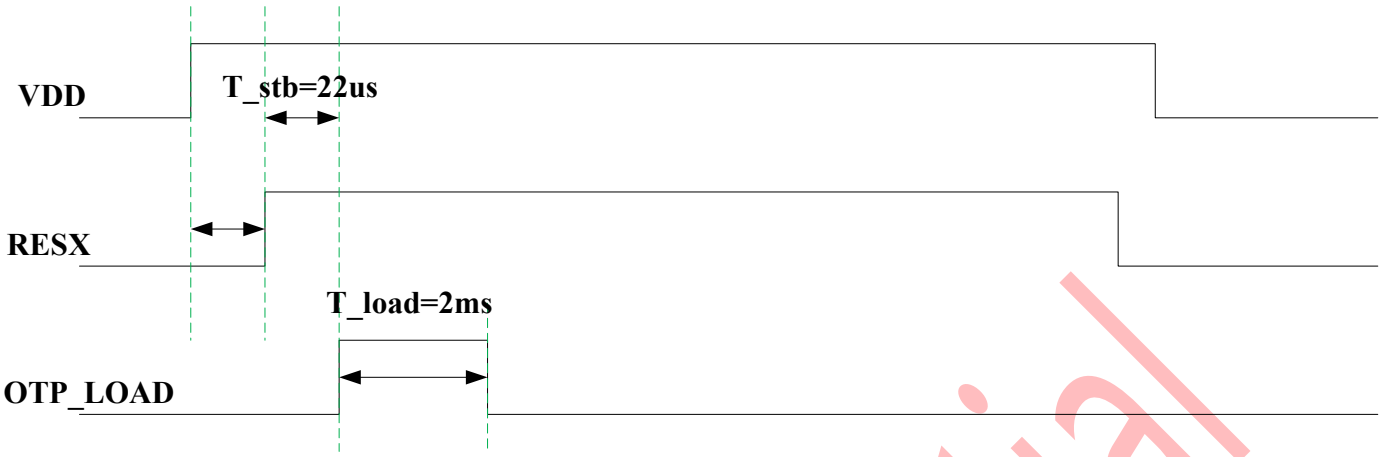
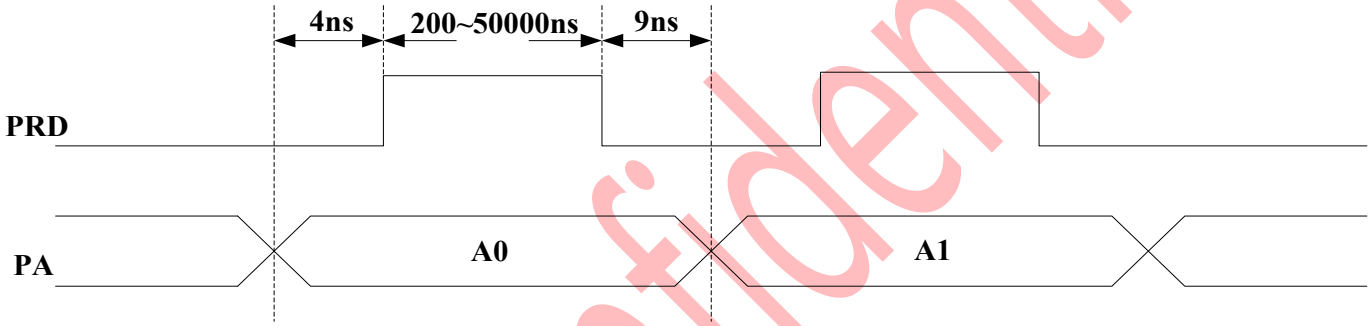


when read, tprd should set as short as possible:



5.14.BIST Function

The BIST (Build In Self Test) is used for inspection, fabrication process and reliability test without external interface operation. this function is controlled by A1 command.

The following BIST patterns are built in the AXS15231E, every pattern and its definition number is also defined as follows:

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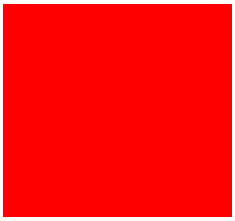
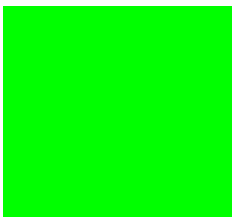
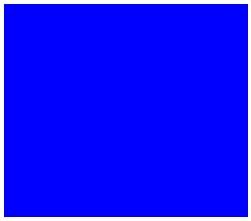
Pattern0：Red
Cr_pat_sel[0]=1



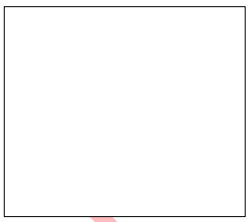
Pattern1：Green
Cr_pat_sel[1]=1



Pattern2：Blue
Cr_pat_sel[2]=1

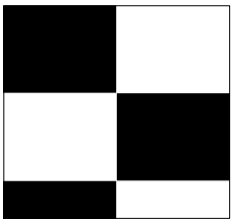


Pattern3：White
Cr_pat_sel[3]=1

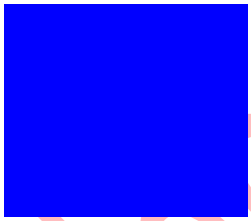


Pattern4：Black
Cr_pat_sel[4]=1

Pattern5：Chese
Cr_pat_sel[5]=1



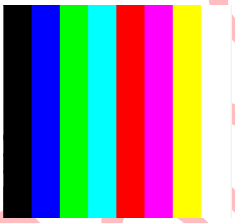
Pattern6：Mid gray
Cr_pat_sel[6]=1



Pattern7：Gray col
Cr_pat_sel[7]=1

Pattern8：Gray row
Cr_pat_sel[1]=1

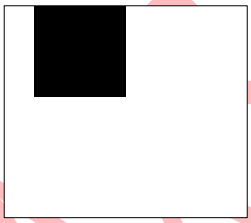
Pattern9：strp col
Cr_pat_sel[1]=1



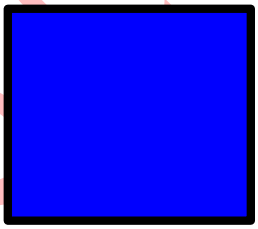
Pattern10：strp row
Cr_pat_sel[1]=1

Pattern11：data partial
Cr_pat_sel[11]=1

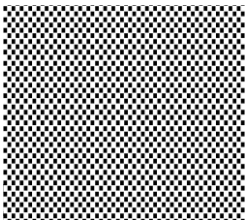
Pattern12：partial inverse
Cr_pat_sel[12]=1



Pattern13：Display rec
Cr_pat_sel[13]=1



Pattern14：data one
Cr_pat_sel[14]=1



Pattern15：crosstalk Grayscale partial mode
Cr_pat_sel[15]=1

Note:

1.cr_bist_en_mode: Bist mode enable

2.cr_pat_sel: display pattern select

3.Pattern 6(Mid Gray): RGB value(gray_red,gray_g,gray_b)can be defined by the user;
The default color display blue(gray_red=gray_g=0,gray_b=8’h FF);

4.Pattern 13(Display rec):
RGB value (gray_red,gray_g, gray_b)can be defined by the user;
the default color display blue (gray_red=gray_g=0, gray_b=8’h FF);
but the whole picture will add a black border

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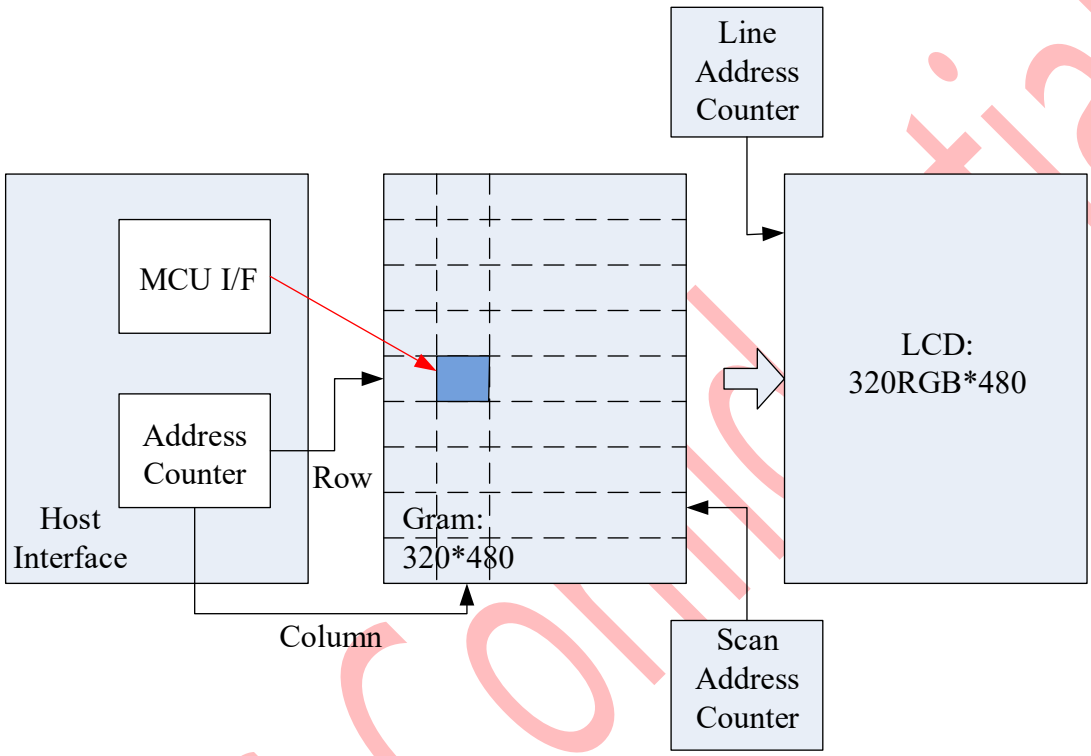
5.15.DISPLAY DATA GRAM

5.15.1. Configuration

The display module has an integrated graphic type static RAM. There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Read or Write to the same location of the Frame Memory



GRAM organization

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5.15.2. Memory to display address mapping

Note:Let's Assume that the size of GRAM is 320x480 for illustration

RGB alignment														
Data control command				Column										
Row	MX=1			319			318			…		0		
				←										
	MX=0			0			1			…		319		
				→										
	MY=1		MY=0	R	G	B	R	G	B	…		R	G	B
	479	↑	0	R	G	B	R	G	B	…		R	G	B
	478		1	R	G	B	R	G	B	…		R	G	B
	477		2	R	G	B	R	G	B	…		R	G	B
	476		3	R	G	B	R	G	B	…		R	G	B
	:		:	R	G	B	R	G	B	…		R	G	B
	3		476	R	G	B	R	G	B	…		R	G	B
	2		477	R	G	B	R	G	B	…		R	G	B
	1		478	R	G	B	R	G	B	…		R	G	B
	0		479 ↓	R	G	B	R	G	B	…		R	G	B
Source output				0	1	2	3	4	5	…		957	958	959

5.15.3. Address Control

The address counter sets the addresses of the display data RAM for writing and reading. Data is written pixel-wise into the RAM matrix of DRIVER. The data for one pixel or two pixels is collected (RGB 5-6-5-bit), according to the data formats. As soon as this pixel-data information is complete the "Write access" is activated on the RAM. The locations of RAM are addressed by the address pointers. The address ranges are X=0 to X=359 and Y=0 to Y=179. Addresses outside these ranges are not allowed. Before writing to the RAM, a window must be defined that will be written. The window is programmable via the command registers XS, YS designating the start address and XE, YE designating the end address.

For example the whole display contents will be written, the window is defined by the following values: XS=0 (0h) YS=0 (0h) and XE=479, YE=319.

In vertical addressing mode (MV=1), the Y-address increments after each byte, after the last Y-address (Y=YE), Y wraps around to YS and X increments to address the next column. In horizontal addressing mode (V=0), the X-address increments after each byte, after the last X-address (X=XE), X wraps around to XS and Y increments to address the next row. After the every last address (X=XE and Y=YE) the address pointers wrap around to address (X=XS and Y=YS).

For flexibility in handling a wide variety of display architectures, the commands "CASET, RASET and MADCTL", define flags MX , which allows mirroring of the X-address. All combinations of flags are allowed.

For each image condition, the controls for the column and row counters apply as below

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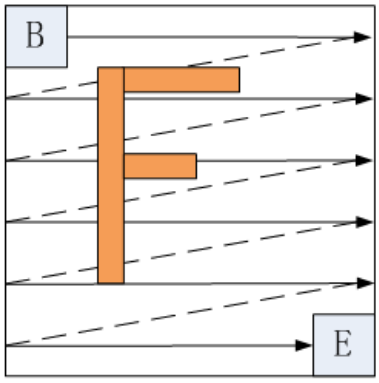
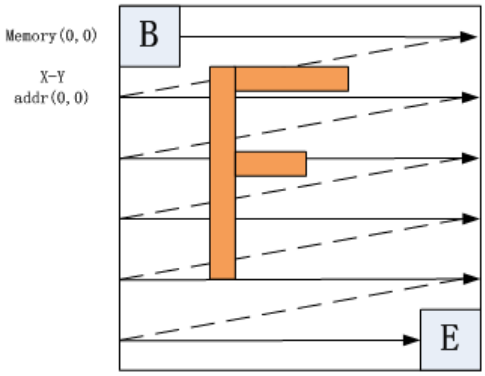
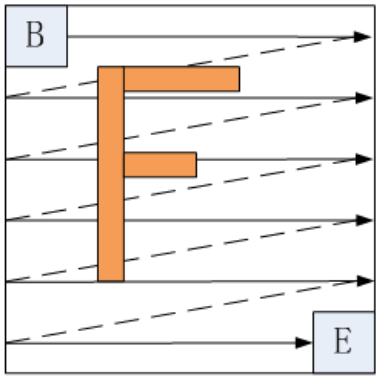
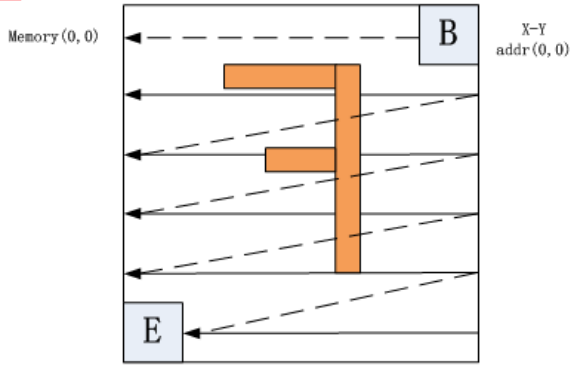
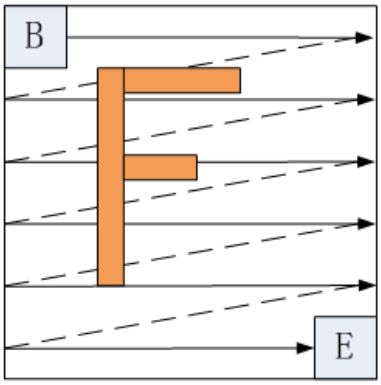
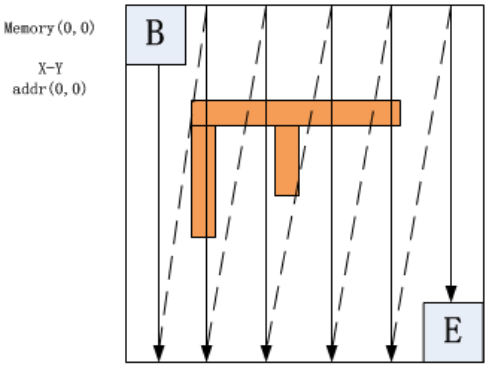
Note:Let's Assume that the size of GRAM is 320x480 for illustration

Condition	Column	Page
Read/Write RAM	Increment by 1	No change
Column value > "End Column"	Return to "Start Column"	Increment by 1
Page value > "End Page"	Return to "Start Column"	Return to "Start Page"
Command "2C/2E" is accepted	Return to "Start Column"	Return to "Start Page"

Display Data Direction	Register	Image in the Host	Image in the GRAM
Normal	cr_dsh_shr =0 cr_rot9_ en=0 cr_36_opt[0]=0		
X-Mirror	cr_dsh_shr =1		
X-Y Exchange	cr_rot9_ e n=1 cr_dsh_shr =1		

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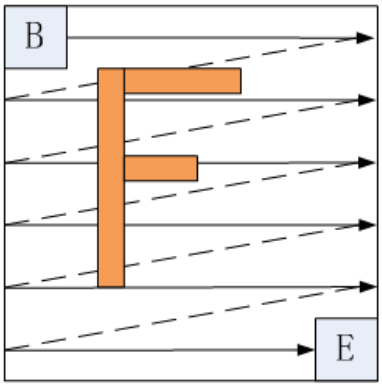
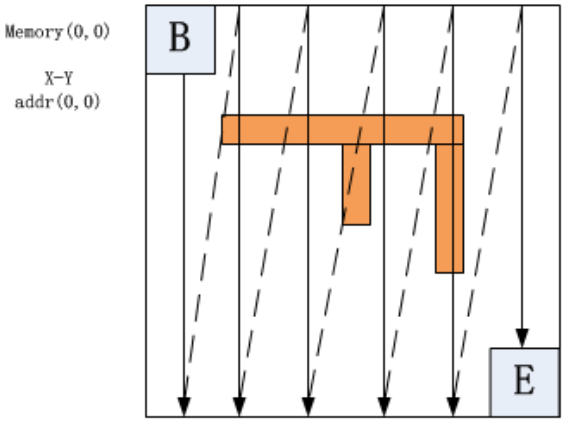
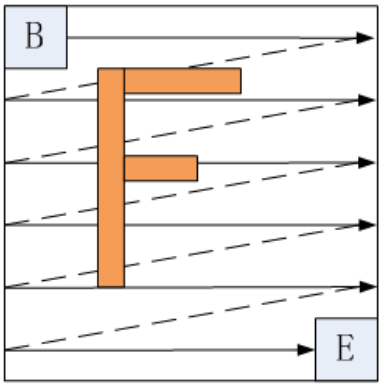
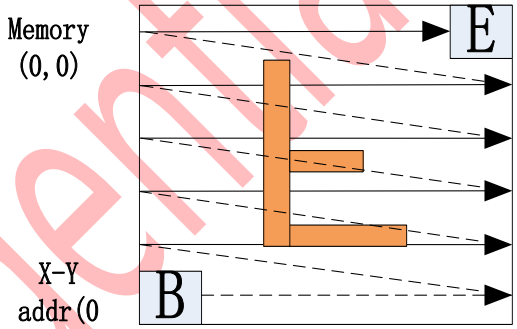
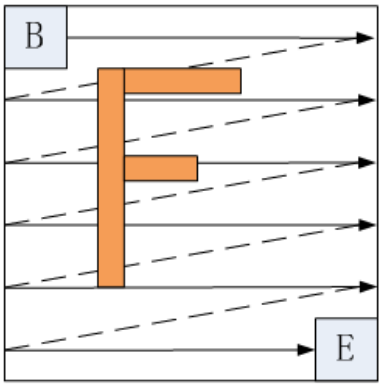
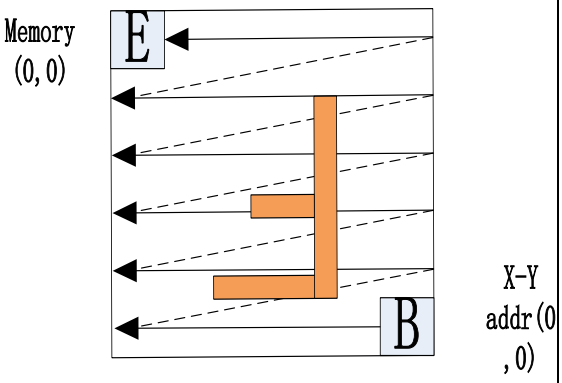
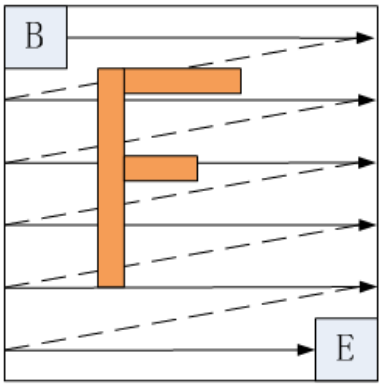
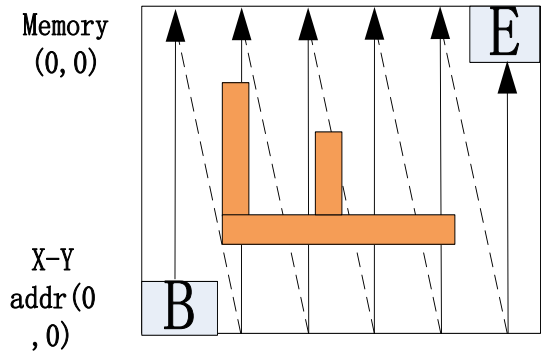
X-Y Exchange X-Mirror	cr_rot9_en=1		
Y-Mirror	cr_36_opt[0]=1		
X-Mirror Y-Mirror	cr_dsh_shr=1 cr_36_opt[0]=1		
X-Y Exchange Y-Mirror	cr_rot9_en=1 cr_dsh_shr=1 cr_36_opt[0]=1		

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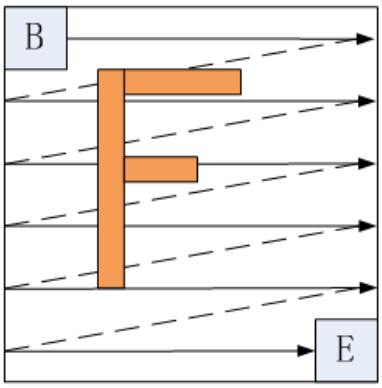
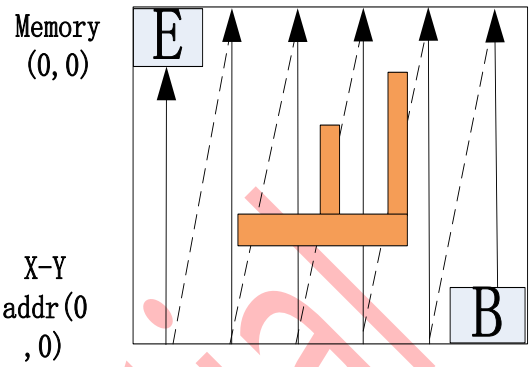
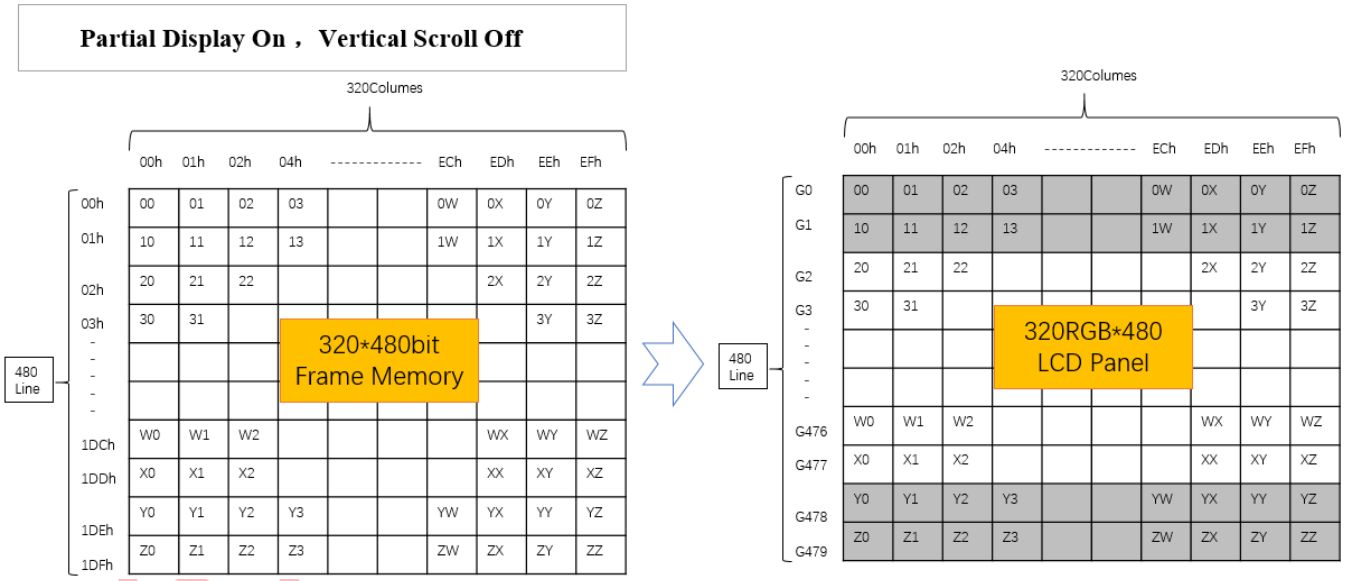
X-Y Exchange X-Mirror Y-Mirror	cr_rot9_en=1 cr_36_opt[0]=1		

5.15.4. Normal Display On， Vertical Scroll Off

To display a dot on leftmost top corner, store the dot data at (column address, row address) = (0,0).



Note:Let's Assume that the size of GRAM is 320x480 for illustration

5.15.5. Vertical Scroll Mode

There are 2 types of vertical scrolling, which are determined by the commands "Vertical Scrolling Definition" (33h) and "Vertical Scrolling Start Address" (37h).

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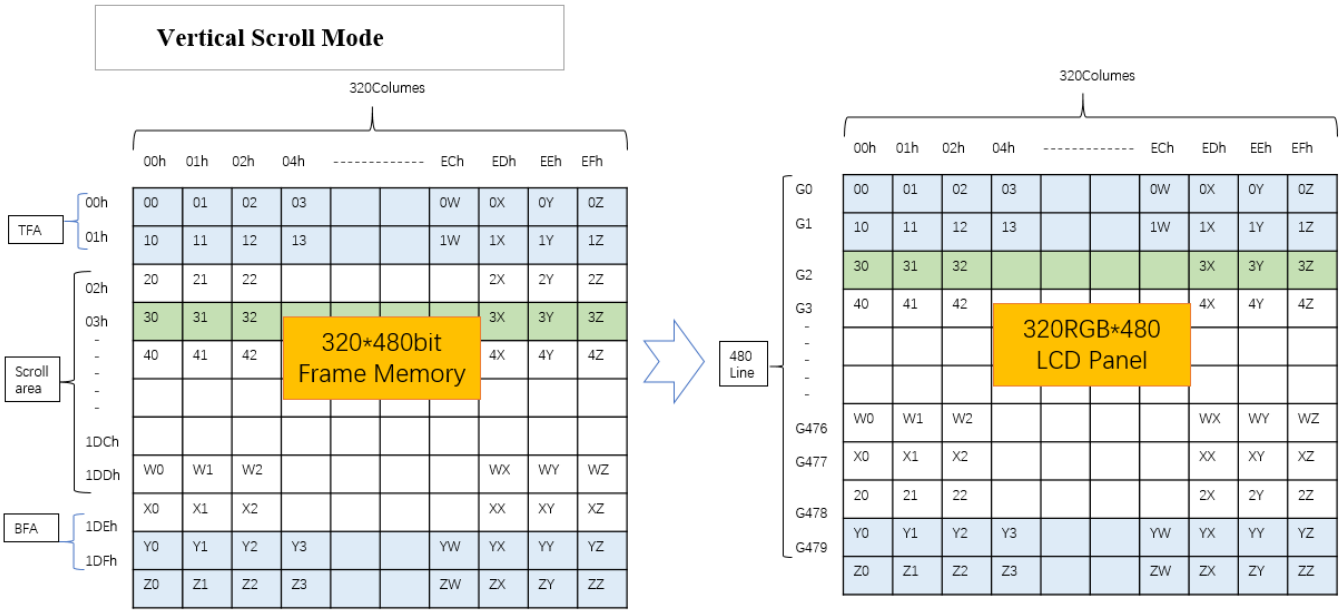
Vertical Scrolling Definition Parameters: TFA , VSA, BFA, VSP: Rolling Scroll
TFA + VSA + BFA= Panel total scan lines, scrolling is applied as shown below
Panel size=320 x 480, TFA =2, VSA=476, BFA=2, VSP: Rolling Scroll



Note:Let's Assume that the size of GRAM is 320x480 for illustration

6. ELECTRICAL CHARACTERISTICS

6.1. Absolute Operation Range

VDDI : VDDI VDDI_TP VDDI_F VDDI_LDO VDDI_DRV VDDI_M

Item	Symbol	Min	Max	Unit
Supply Voltage(Analog)	VCI_A	-0.3	+4.0	V
Supply Voltage(Analog)	VCI_C	-0.3	+4.0	V
Supply Voltage(I/O)	VDDI	-0.3	+4.0	V
Supply Voltage(Logic)	VDD	-0.3	+1.7	V
Driver Supply Voltage	VGH-VGL	-0.3	+30	V
Logic Input Voltage Range	VIN	-0.3	VDDI+0.3	V

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Logic Output Voltage Range	VO	-0.3	VDDI+0.3	V
Operating Temperature Range	TOPR	-30	+85	℃
Storage Temperature Range	TSTG	-40	+125	℃

6.2. DC characteristic

6.2.1. Basic DC characteristic

(VCI=2.65V~3.6V, IOVCC = 1.65V~3.6V, Ta = -30ºC ~ 70ºC)

Parameter	Symbol	Conditions	Specification			Unit	Notes
			MIN	TYP	MAX		
Power & Operation Voltage							
Analog Operating voltage	VCI	Operating Voltage	2.65	3.3	3.6	V	
Logic Operating voltage	VDDI	I/O supply voltage	1.65	1.8	3.6	V	
Digital Operating voltage	VDD	Digital supply voltage	1.2	1.32	1.48	V	
Input / Output							
Logic High level input voltage	V_{IH}	-	0.7 IOVCC	-	IOVCC	V	
Logic Low level input voltage	V_{IL}	-	VSS	-	0.3 IOVCC	V	
Logic High level output voltage	V_{OH}	I_{OH} = -1.0mA	0.7 IOVCC	-	IOVCC	V	
Logic Low level output voltage	V_{OL}	I_{OL} = +1.0mA	VSS	-	0.3 IOVCC	V	
Logic High level input current	I_{IH}	-	-	-	1	uA	
Logic Low level input current	I_{IL}	-	-1	-	TBD	uA	
Logic Input leakage current	I_{IL}	VIN = IOVCC or VSS	-0.1	-	0.1	uA	
VCOM Operation							
VCOM DC voltage	VCOM	-	-2.5	-	0	V	0
Source Driver							
Source positive output range	Vsout	-	0.75		6.50	V	＜VSP-0.3

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Source negative output range	Vsout	-	-5.0		0.70	V	> VSN+0.3
Output offset voltage	VOFSET	- TBD	-	-	-	mV	
Reference Voltage							
Internal reference voltage	VREF_TP	Supply by VSP	2.9	-	6.0	V	
		Supply by VCI	1.4	-	2.8	V	
Internal reference voltage	VCG_TP	Supply by VSP	2.9	-	6.0	V	
		Supply by VCI	1.4	-	2.8	V	
Internal reference voltage	VREF	-	-	1.8	-	V	
Charge pump voltage							
VSP charge pump	VSP		5.0	-	6.8	V	
VSN charge pump	VSN		-5.4	-	-4.0	V	
VGH charge pump	VGH		10.4	15.0	15.9	V	
VGL charge pump	VGL		-14.2	-12.0	-7.6	V	

6.2.2. MIPI DC character

DC characteristics for MIPI-DSI

(VCI=2.65V~3.6V, IOVCC = 1.65V~3.6V, Ta = -30°C ~ 70°C)

Parameter	Symbol	Conditions	Specification			Unit
			MIN	TYP	MAX	
Power supply voltage for MIPI Interface						
Power supply voltage for MIPI interface	VDDI_M	-	1.65	1.8	3.6	V
LPDT Input Characteristics						
Pad signal voltage range	VI	-	-50	-	1350	mV
Ground Shift	HS_VSS	-	-50	-	50	mV
Logic 0 input threshold	VIL	-	0	-	550	mV
Logic 1 input threshold	VIH	-	880	-	VDDI_M	mV
Input hysteresis	VHYST	-	25	-	-	mV
LPDT Output Characteristics						
Output low level	VOL	-	-50	-	50	mV

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Output high level	VOH	-	1.1	1.2	1.3	V
Logic 1 contention threshold	VIHCD,MIN	-	450	-	HS_LDO	mV
Logic 0 contention threshold	VILCD,MAX	-	0	-	200	mV
Output impedence of LPDT	ZOLP	-	80	-	125	ohm
Hi-speed Input/Output Characteristics						
Single-end input low voltage	VILHS	-	-40	-	-	mV
Single-end input high voltage	VIHHS	-	-	-	460	mV
Common mode voltage	VCMRXDC	-	70	-	330	mV
Hi-speed transmit voltage	VOD	-	140	200	250	mV
Differential input impedence	ZID	-	80	100	125	ohm

6.3. AC characteristic

6.3.1. Reset

The part of touch

POR（Power on Reset）Detect VCI, Vth=2.2V

External Reset: 0~VDDI/0~VCI

Soft reset

Host can issue reset instructions to reset the system

6.3.2. Serial interface characteristics (3-line SPI)

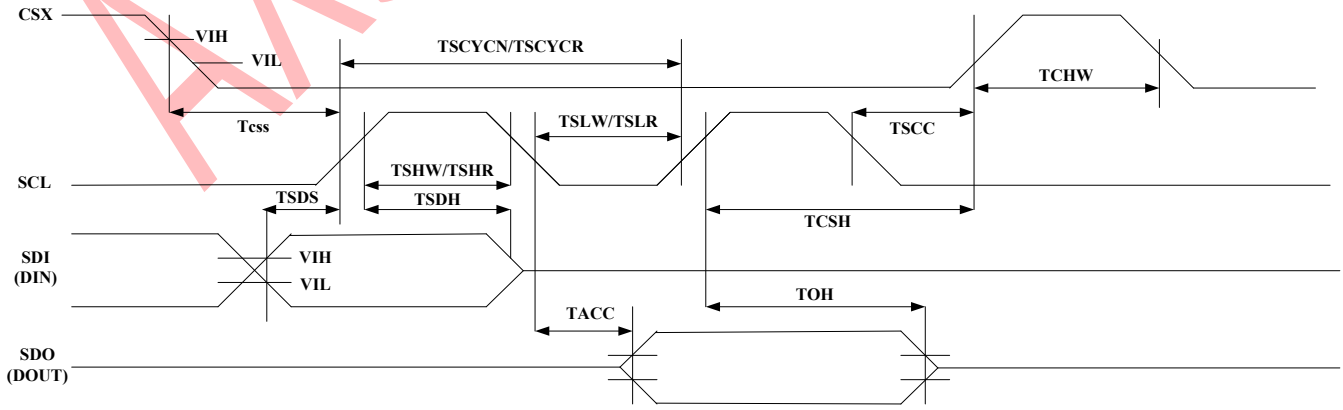

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Figure: 3-pin Serial Interface Characteristics

Table: SPI Interface Characteristics

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	TCSS	Chip select setup time	15	-	ns	-
	TCSH	Chip select hold time	15	-	ns	-
	TSCC	Chip select setup time	60	-	ns	-
	TCHW	Chip select setup time	40	-	ns	-
SCL	TSCYCW	Serial clock cycle (Write)	20	-	ns	-
	TSHW	SCL “H” pulse width (Write)	10	-	ns	-
	TSLW	SCL “L” pulse width (Write)	10	-	ns	-
	TSCYCR	Serial clock cycle (Read)	150	-	ns	-
	TSHR	SCL “H” pulse width (Read)	60	-	ns	-
	TSLR	SCL “L” pulse width (Read)	60	-	ns	-
SDA (DIN) (DOUT)	TSDS	Data setup time	10	-	ns	-
	TSDH	Data hold time	10	-	ns	-
	TACC	Access time	10	50	ns	For maximum CL=30pF For minimum CL=8pF
	TOH	Output disable time	15	50	ns	

Note 1: IOVCC= 3.3V, VCI=2.65 to 3.6V, VSSA=VSS=0V, Ta=-30 to 70°C

Note 2: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

6.3.3. Serial interface characteristics (4-line SPI)

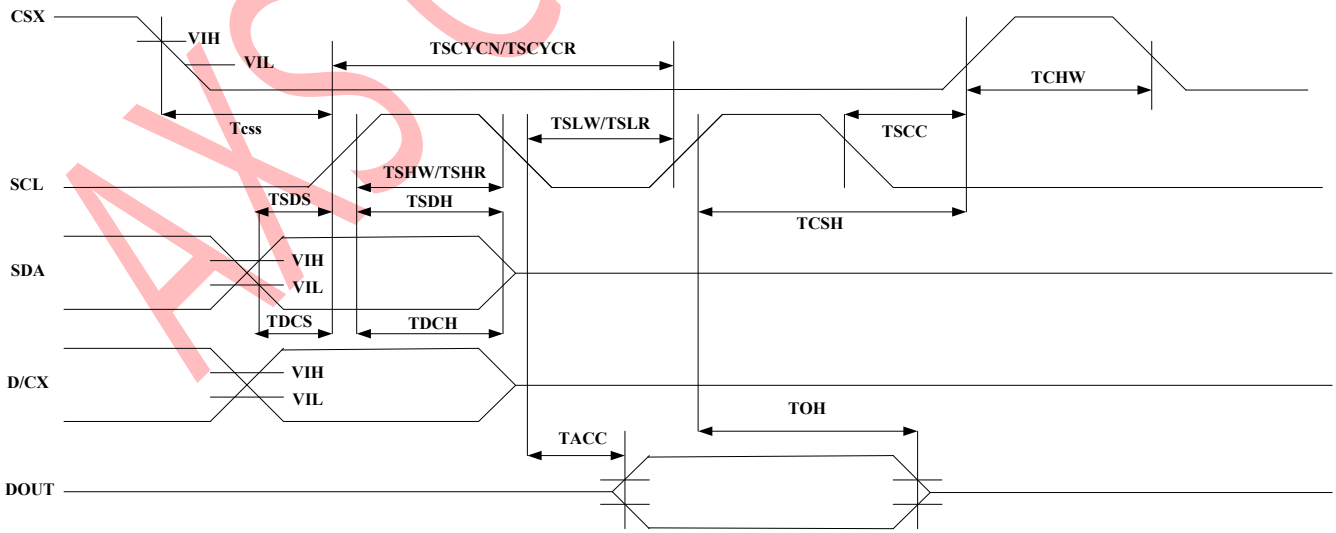

Figure: 4-pin Serial Interface Characteristics

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Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15	-	ns	
	T_{CSH}	Chip select hold time (write)	15	-	ns	
	T_{CSS}	Chip select setup time (read)	60	-	ns	
	T_{SCC}	Chip select hold time (read)	65	-	ns	
	T_{CHW}	Chip select "H" pulse width	40	-	ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	20	-	ns	-write command & data ram
	T_{SHW}	SCL "H" pulse width (Write)	10	-	ns	
	T_{SLW}	SCL "L" pulse width (Write)	10	-	ns	
	T_{SCYCR}	Serial clock cycle (Read)	150	-	ns	-read command & data ram
	T_{SHR}	SCL "H" pulse width (Read)	60	-	ns	
	T_{SLR}	SCL "L" pulse width (Read)	60	-	ns	
D/CX	T_{DCS}	D/CX setup time	10	-	ns	
	T_{DCH}	D/CX hold time	10	-	ns	
SDA (DIN)	T_{SDS}	Data setup time	10	-	ns	
	T_{SDH}	Data hold time	10	-	ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum CL=30pF
	T_{OH}	Output disable time	15	50	ns	For minimum CL=8pF

Note 1: IOVCC= 3.3V, VCI=2.65 to 3.6V, VSSA=VSS=0V, Ta=-30 to 70°C
Note 2: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

6.3.4. Quad Serial interface characteristics

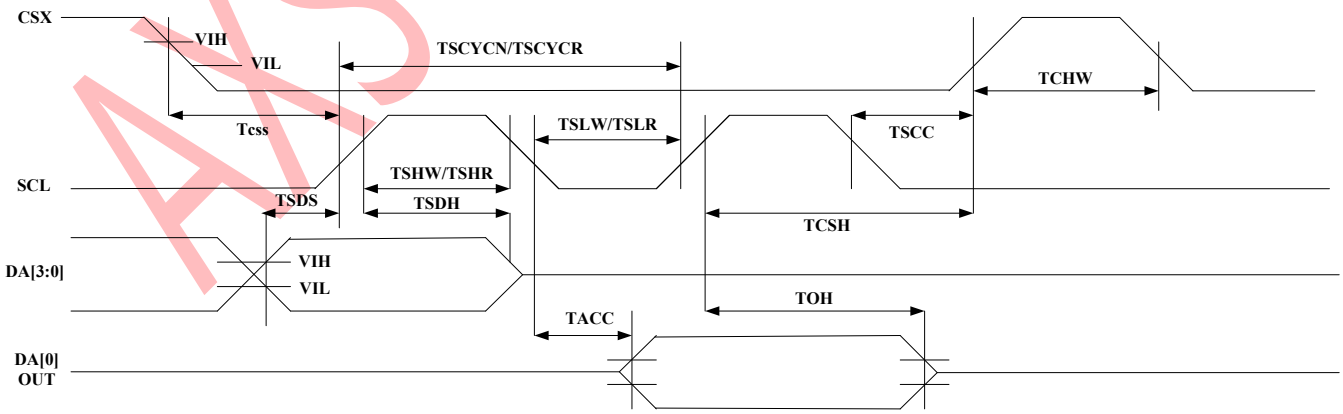

Figure: Quad SPI Interface Characteristics

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Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	60		ns	
	T_{SCC}	Chip select hold time (read)	65		ns	
	T_{CHW}	Chip select "H" pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (Write)	11		ns	
	T_{SHW}	SCL "H" pulse width (Write)	5		ns	
	T_{SLW}	SCL "L" pulse width (Write)	5		ns	
	T_{SCYCR}	Serial clock cycle (Read)	150		ns	
	T_{SHR}	SCL "H" pulse width (Read)	60		ns	
	T_{SLR}	SCL "L" pulse width (Read)	60		ns	
SDA (DIN)	T_{SDS}	Data setup time	5		ns	
	T_{SDH}	Data hold time	5		ns	
DOUT	T_{ACC}	Access time	5	50	ns	For maximum CL=30pF
	T_{OH}	Output disable time	5	50	ns	For minimum CL=8pF

Note 1: IOVCC=3.3V, VCI=2.65 to 3.6V, VSSA=VSS=0V, Ta=-30 to 70°C
Note 2: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

6.3.5. RGB interface characteristics

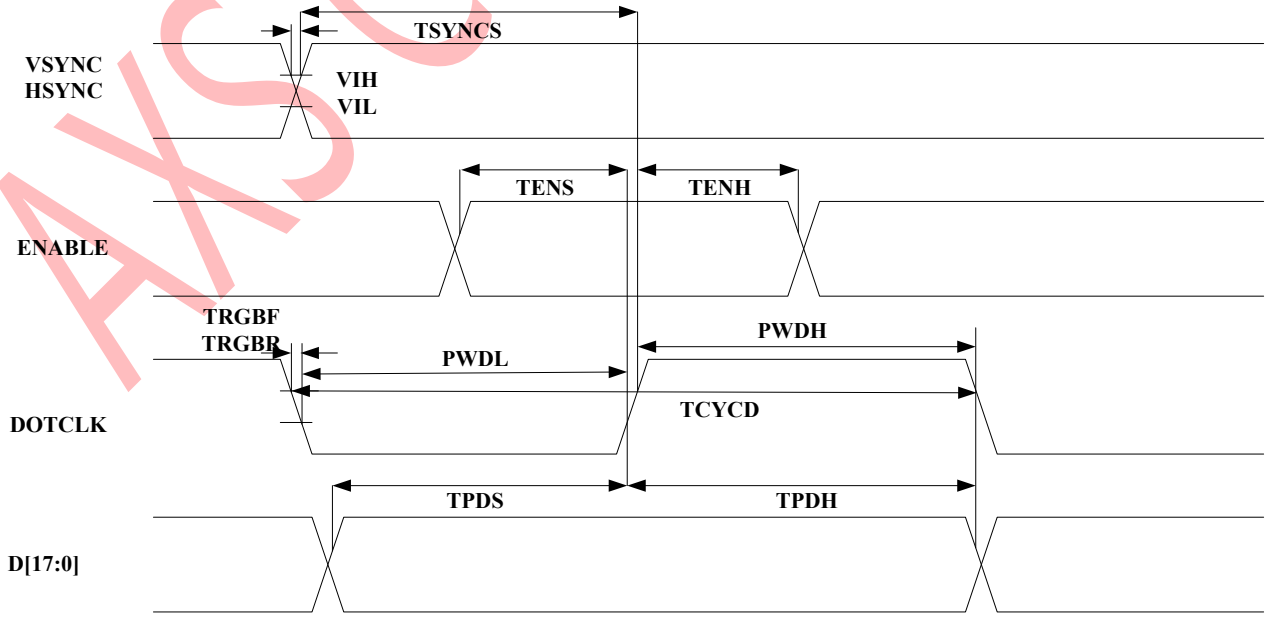

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Figure: RGB Interface Characteristics

Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC/HSYNC	tsyncs	VSYNC/HSYNC setup time	15	-	ns	18/16-bit bus RGB interface mode
	tsynch	VSYNC/HSYNC hold time	15	-	ns	
DE	tens	DE setup time	15	-	ns	
	tenh	DE hold time	30	-	ns	
D[17:0]	tpds	Data setup time	15	-	ns	
	tpdh	Date hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level period	30	-	ns	
	PWDL	DOTCLK low-level period	30	-	ns	
	tcycd	DOTCLK cycle time	32	-	ns	
	trgbr,trgbf	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	

6.3.6. 8080 Series MCU Parallel Interface Characteristics: 18/16/9/8-bit Bus

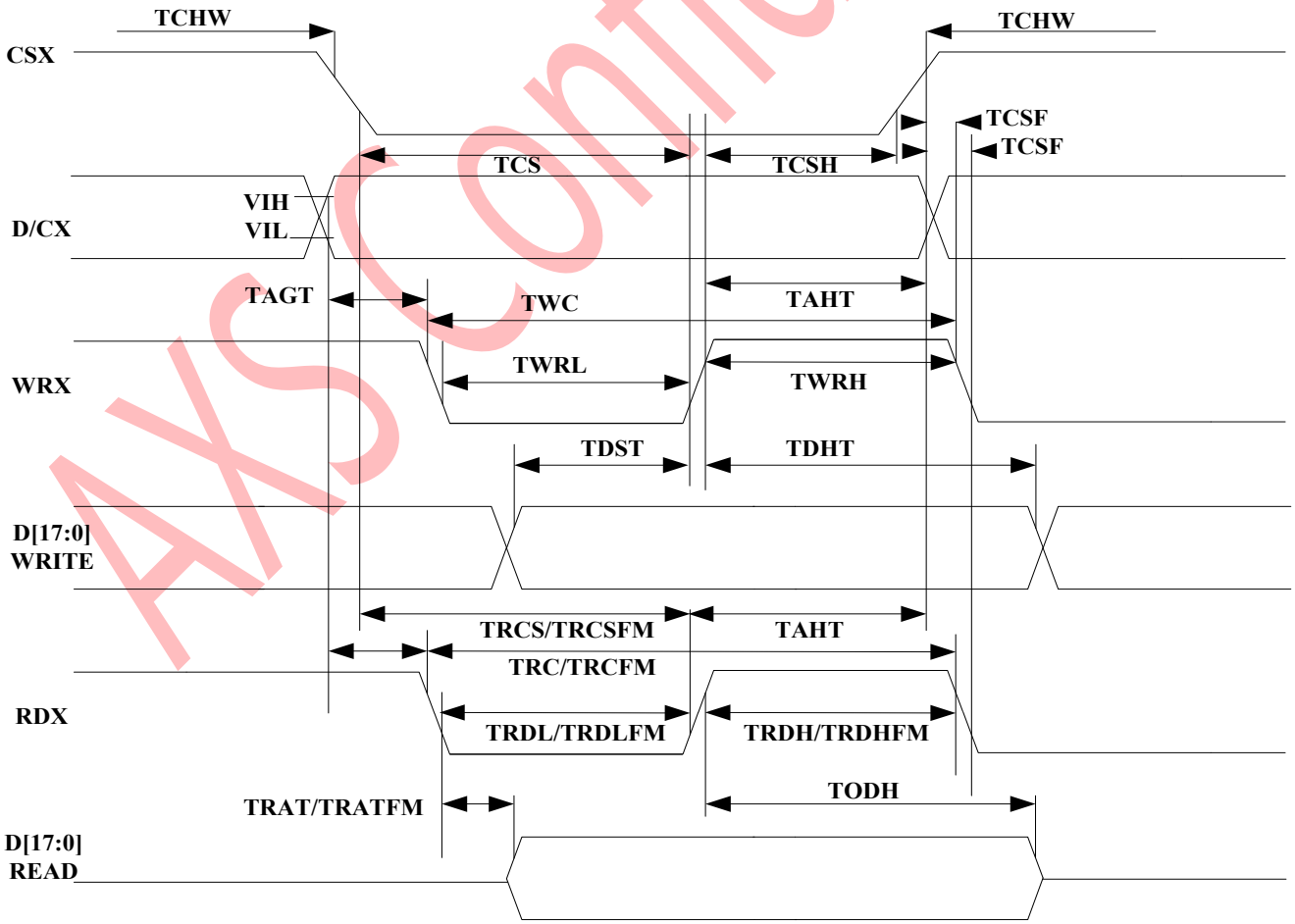

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Figure:8080 Series Interface Characteristics

Signal	Symbol	Parameter	min	max	Unit	Description
D/CX	tast	Address setup time	0	-	ns	
	taht	Address hold time(Write/Read)	10	-	ns	
CSX	tchw	CSX "H" pulse width	0	-	ns	
	tcs	Chip Select setup time(Write)	15	-	ns	
	trcs	Chip Select setup time(Read ID)	45	-	ns	
	trcsfm	Chip Select setup time(Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	twc	Write Cycle	32	-	ns	
	twrh	Write Control pulse H duration	32	-	ns	
	twrl	Write Control pulse L duration	32	-	ns	
RDX(FM)	trcfm	Read Cycle (FM)	450	-	ns	
	trdhfm	Read Control H duration(FM)	90	-	ns	
	trdlfm	Read Control L duration(FM)	355	-	ns	
RDX(ID)	trc	Read Cycle (ID)	160	-	ns	
	trdh	Read Control pulse H duration	90		ns	
	trdl	Read Control pulse L duration	45		ns	
D[17:0], D[17:10] &D[8:1], D[17:10] ,D[17:9]	tdst	Write data setup time	10		ns	For CL=30pF
	tdht	Write data hold time	10		ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

Note: Ta = -30 to 70 °C, VDDI=1.65V to 3.3 V, VDDB=2.5V to 3.3V, VSS=0V.

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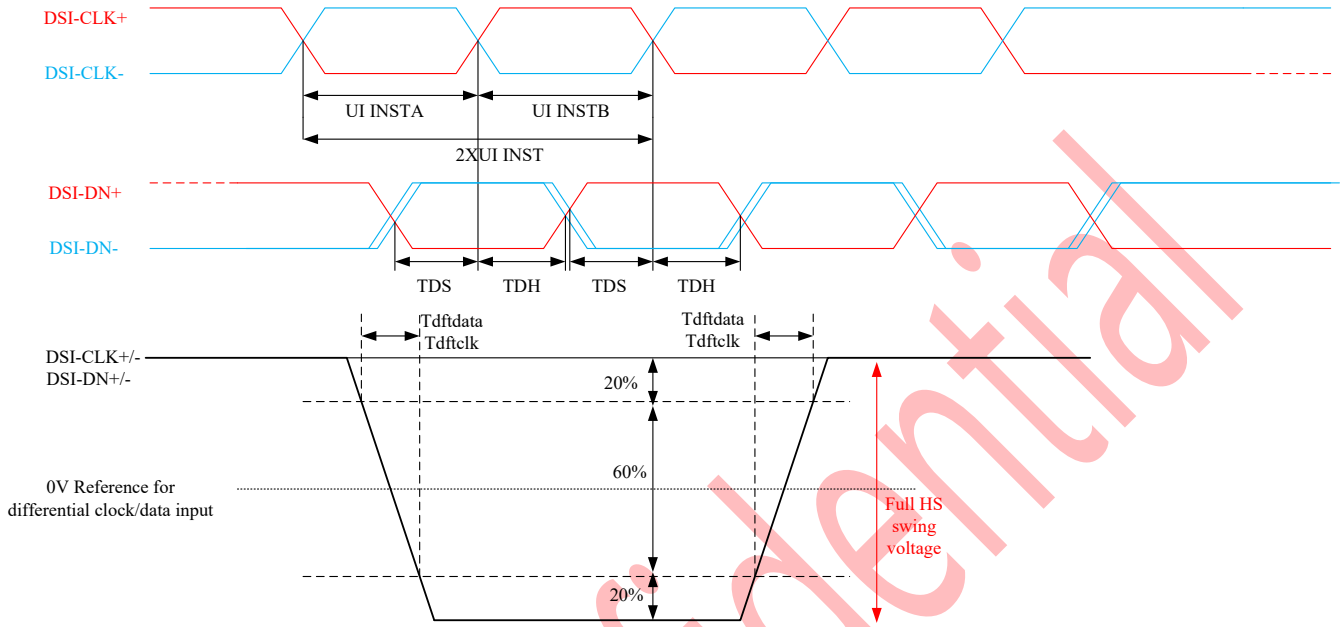
6.3.7. MIPI-DSI characteristics

6.3.7.1. High speed mode



Parameter	Symbol	Parameter	Specification			Unit	Description
			MIN	TYP	MAX		
DSI-CLK+/-	$2xUI_{INSTA}$	Double UI instantaneous	4		25	ns	
DSI-CLK+/-	UI_{INSTA} UI_{INSTB}	UI instantaneous halfs	2		12.5	ns	$UI=UI_{INSTA}=UI_{INSTB}$
DSI-D0+/-	T_{DS}	Data to clock setup time	0.15	-		UI	
DSI-D0+/-	T_{DH}	Data to clock hold time	0.15	-		UI	

Figure: AC characteristics for MIPI-DSI High speed mode

6.3.7.2. Low power mode

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
Low Power Mode						
DSI-D0+/-	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP -11 periods MPU Display Module	50	-	-	ns
DSI-D0+/-	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP -11 periods Display Module MPU	58	-	-	ns
DSI-D0+/-	$T_{TA-SURED}$	Time-out before the MPU start driving	T_{LPXD}	-	$2XT_{LPXD}$	ns

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DSI-D0+/-	$T_{TA-GETD}$	Time to driver LP-00 by display module	5XT LPXD	-	-	ns
DSI-D0+/-	T_{TA-GOD}	Time to driver LP-00 after turnaround request - MPU	4XT LPXD	-	-	ns
DSI-D0+/-	Ratio T_{LPX}	Ratio of T_{LPXM} / T_{LPXD} between MCU and display module	2/3	-	3/2	

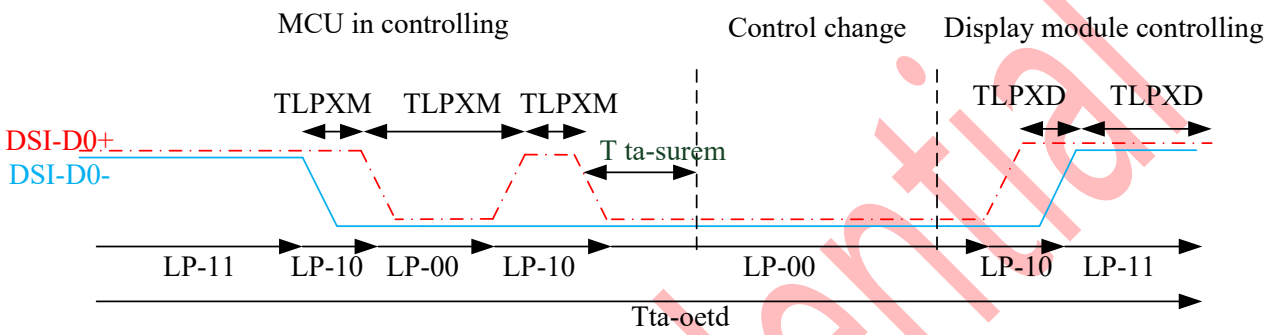

Figure: BTA from the MCU to the Display Module

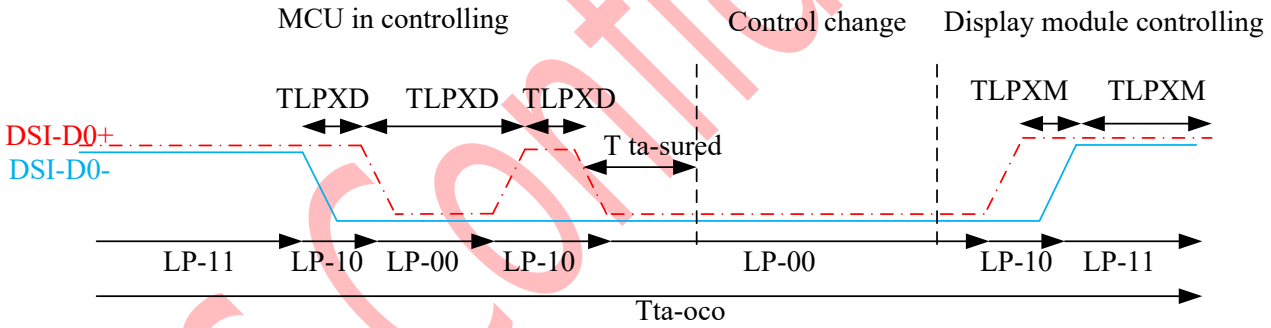

Figure: BTA from the Display Module to the MCU

6.3.7.3. Bursts

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
High Speed Data Transmission Bursts						
DSI-Dn+/-	T_{LPX}	Length of any low-power state period	50	-	-	ns
DSI-Dn+/-	$T_{HS-PREPARE}$	Time to driver LP-00 to prepare for HS transmission	40ns + 4UI	-	85ns + 6UI	ns
DSI-Dn+/-	$T_{HS-PREPARE}$ +$T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time to driver HS-0 before the sync sequence	145ns + 10UI	-	-	ns

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DSI-Dn+/-	$T_{D\text{-}TERM\text{-}EN}$	Time to enable Data Lanereceiver line termination measured from when Dn crosses $V_{IL(max)}$	Time for Dn to reach $V_{TERM\text{-}EN}$	-	35ns + 4UI	ns
DSI-Dn+/-	$T_{HS\text{-}SKIP}$	Time-out at RX to ignore transition period of EoT	40	-	55ns + 4UI	ns
DSI-Dn+/-	$T_{HS\text{-}TRAIL}$	Time to driver flipped differential state after last payload data bit of a HS transmission burst	max (8UI, 60ns+4UI)	-	-	ns
DSI-Dn+/-	$T_{HS\text{-}EXIT}$	Time to driver LP-11 after HS burst	100	-	-	ns
DSI-Dn+/-	T_{EoT}	Time from start of $T_{HS\text{-}TRAIL}$ Period to start of LP-11 state	-	-	105ns +12UI	ns

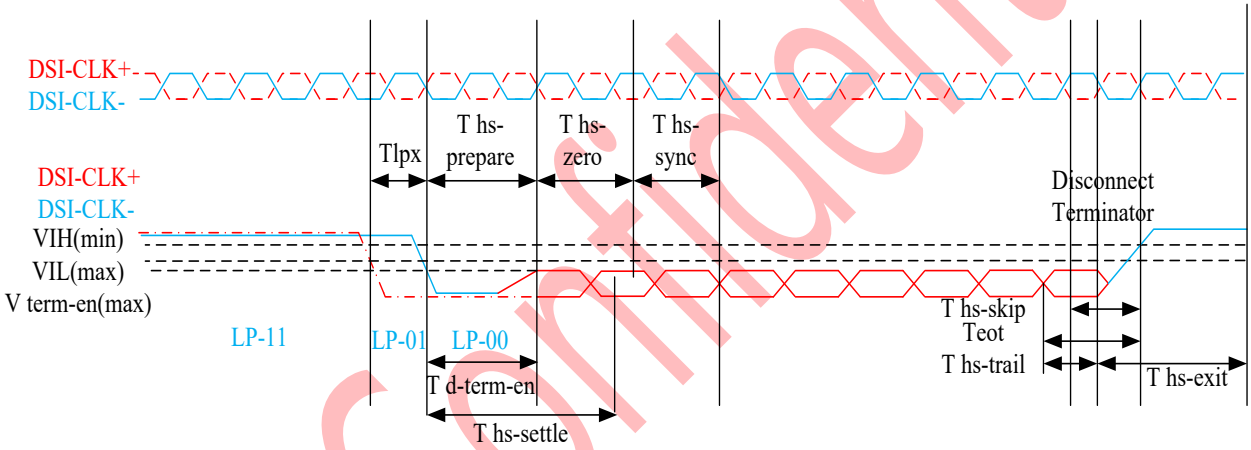

Figure: High Speed Data Transmission Bursts

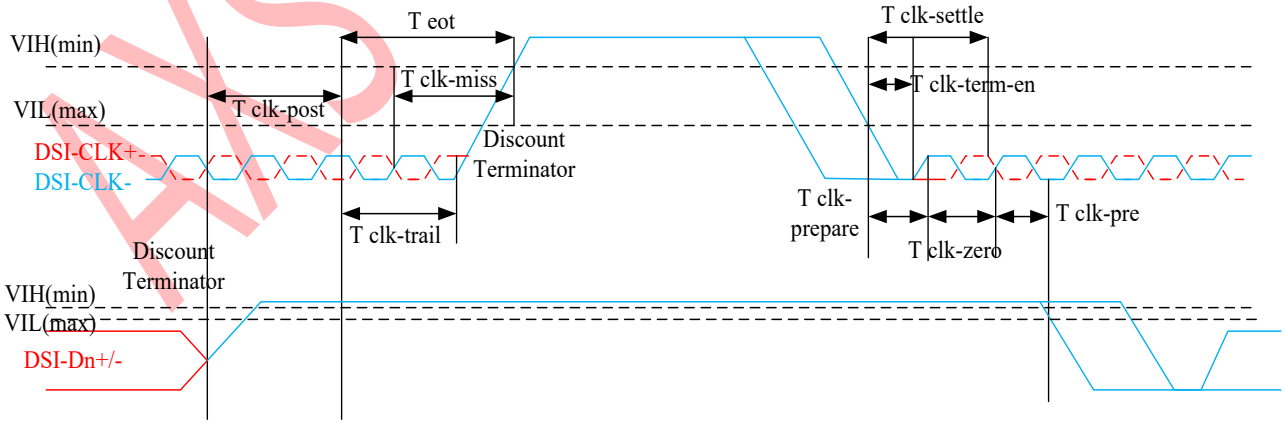

Figure: Switching the clock Lane between clock Transmission and Low Power Mode

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Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
Switching the clock Lane between clock Transmission and Low Power Mode						
DSI-CLK+/-	$T_{CLK-POST}$	Time that the transmitter shall continue sending HS clock after the last associated Data Lanehas transitioned to LP mode	60ns + 52UI	-	-	ns
DSI-CLK+/-	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lanebeginning the transition from LP to HS mode	8	-	-	UI
DSI-CLK+/-	$T_{CLK-PREPARE}$	Time to driver LP-00 to prepare for HS clock transmission	38	-	95	ns
DSI-CLK+/-	$T_{CLK-TERM-EN}$	Time to enable Clock Lanereceiver line termination measured from when Dn crosses $V_{IL(max)}$	Time for Dn to reach $V_{TERM-EN}$	-	38	ns
DSI-CLK+/-	$T_{CLK-PREPARE}$ +$T_{CLK-ZERO}$	$T_{CLK-PREPARE}$+ time for lead HS-0 driver period before starting Clock	300	-	-	ns
DSI-CLK+/-	$T_{CLK-TRAIL}$	Time to driver HS differential state after last payload clock bit of a HS transmission burst	60	-	-	ns
DSI-CLK+/-	T_{EoT}	Time from start of $T_{CLK-TRAIL}$ periodto start of LP-11 state	-	-	105ns + 12UI	ns

6.3.7.4. LP-11 between High Speed and Low Power Modes

DSI-D0 High Speed or Low Power modes are starting or finishing from/to Stop State (SS, LP-11) when

different combinations, what are listed below, are possible:

1. High Speed Mode => Stop State (SS, LP-11) => High Speed Mode
2. High Speed Mode => Stop State (SS, LP-11) => Low Power Mode
3. Low Power Mode => Stop State (SS, LP-11) => High Speed Mode
4. Low Power Mode => Stop State (SS, LP-11) => Low Power Mode

The Low Power Mode is also including 2 different functions:

1. Escape
2. Bus Turnaround (BTA)

Stop State (SS, LP-11) Timings from Previous mode to Next mode

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Previous \ Next	Escape mode		HSDT		BTA	
	Min	Max	Min	Max	Min	Max
Escape mode	100ns	-	100ns	-	100ns	-
HSDT	60ns+52UI	-	60ns+52UI	-	60ns+52UI	-
BTA	100ns	-	100ns	-	100ns	-

7. Power Definition

7.1. Normal Power On/Off Sequence

VDDI and VCI can be applied in any order. VDDIand VCI can be powered down in any order. In a MCU system, VDDI is typically generated from VCI by a DC-DC or LDO converter. So generally speaking, VDDI is powered up after the VCI.

During power off, if LCD is in the Sleep Out mode, VDDI and VCI must be powered down minimum 120msec after RESX has been released.

During power off, if LCD is in the Sleep In mode, VDDI or VCI can be powered down minimum 0msec after RESX has been released.

CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

Note 1: There will be no damage to the display module if the power sequences are not met.

Note 2: There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.

Note 3: There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command.

Also, between receiving Sleep In command and Power Off Sequence. If RESX line is not held stable by host during Power On Sequence, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise, function is not guaranteed.

The power on/off sequence is illustrated below:

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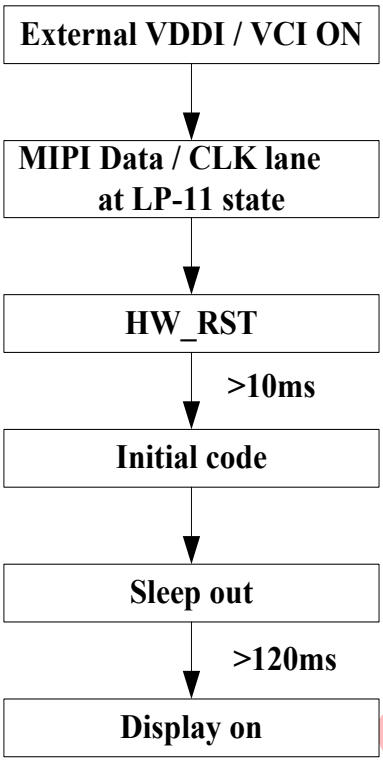

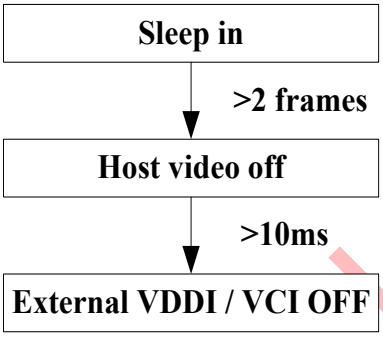

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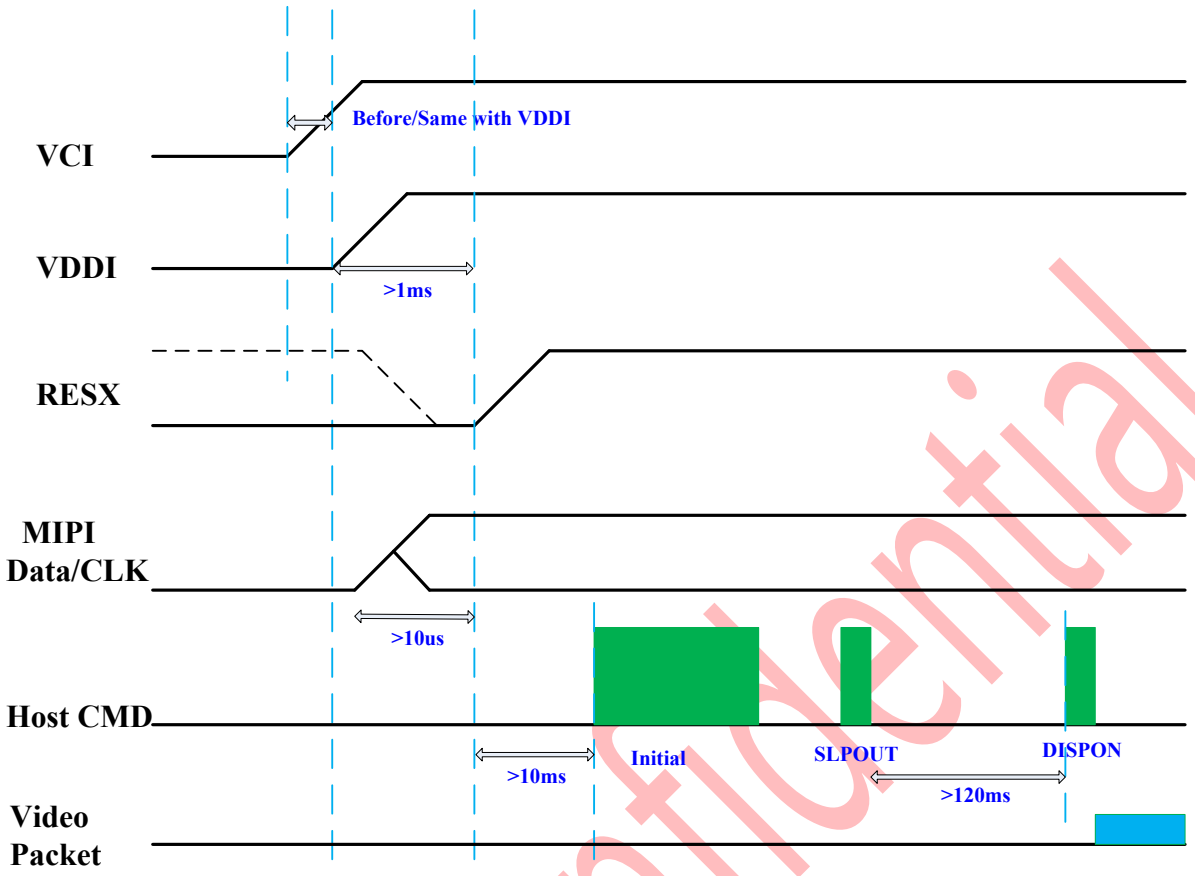

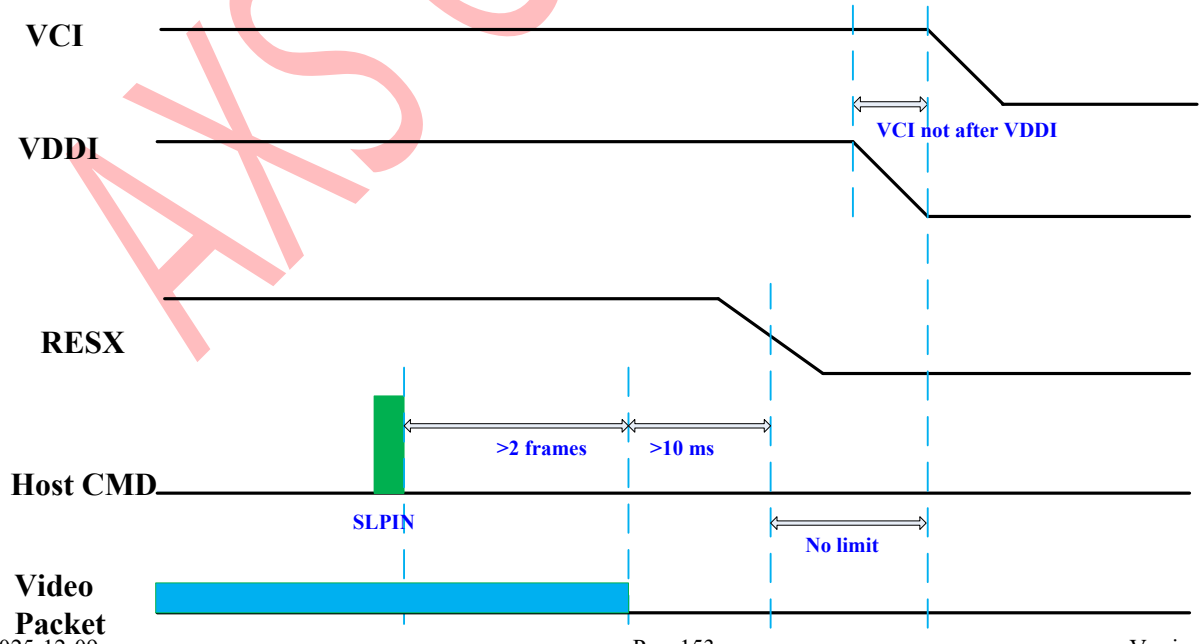

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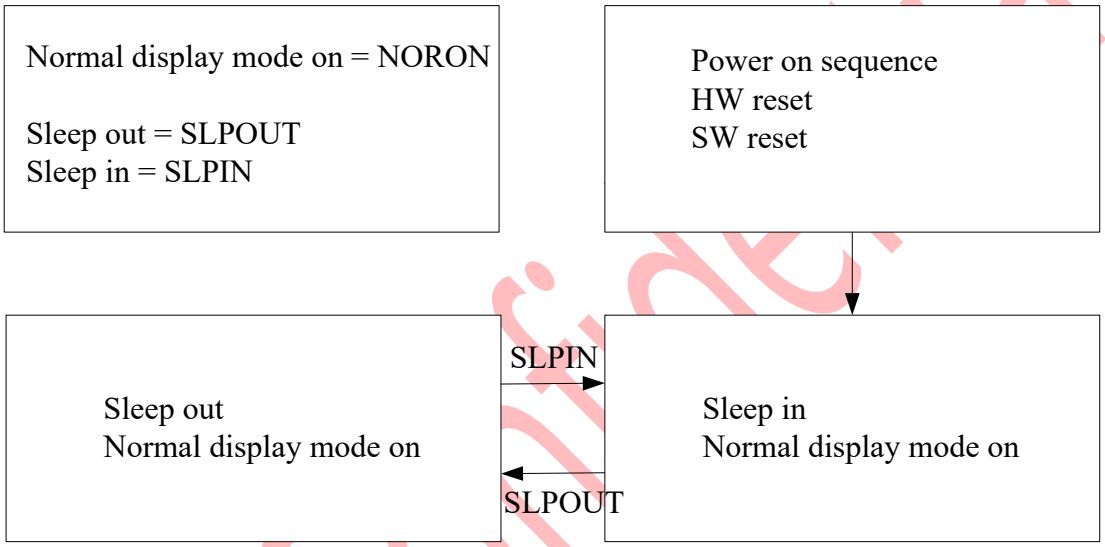
7.2. Abnormal Power Off

The uncontrolled power off means a situation when e.g. there is removed a battery without the controlled power off sequence. There will not be any damage for the display module or the display module will not cause any damage to the host or lines of the interface. At an uncontrolled power off event, the display will go blank and there will not be any visible effects within (TBD) second on the display (blank display) and remains blank until "Power On Sequence" powers it up.

7.3. Power flow chart



Note 1: There is not any abnormal visual effect when there is changing from one power mode to another power mode.

Note 2: There is not any limitation, which is not specified by this spec, when there is changing from one power mode to another power mode.

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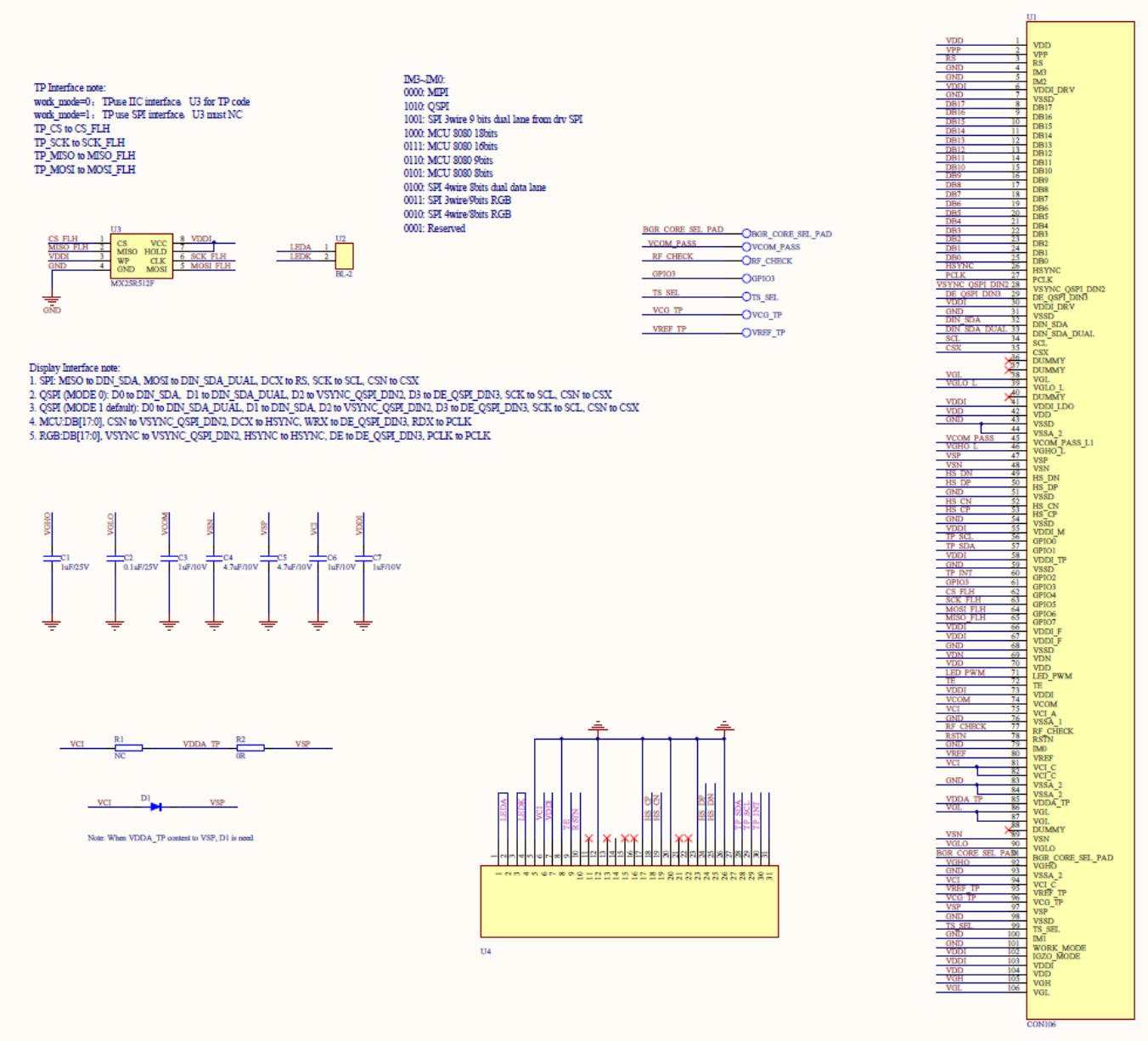
8. APPLICATION CIRCUIT



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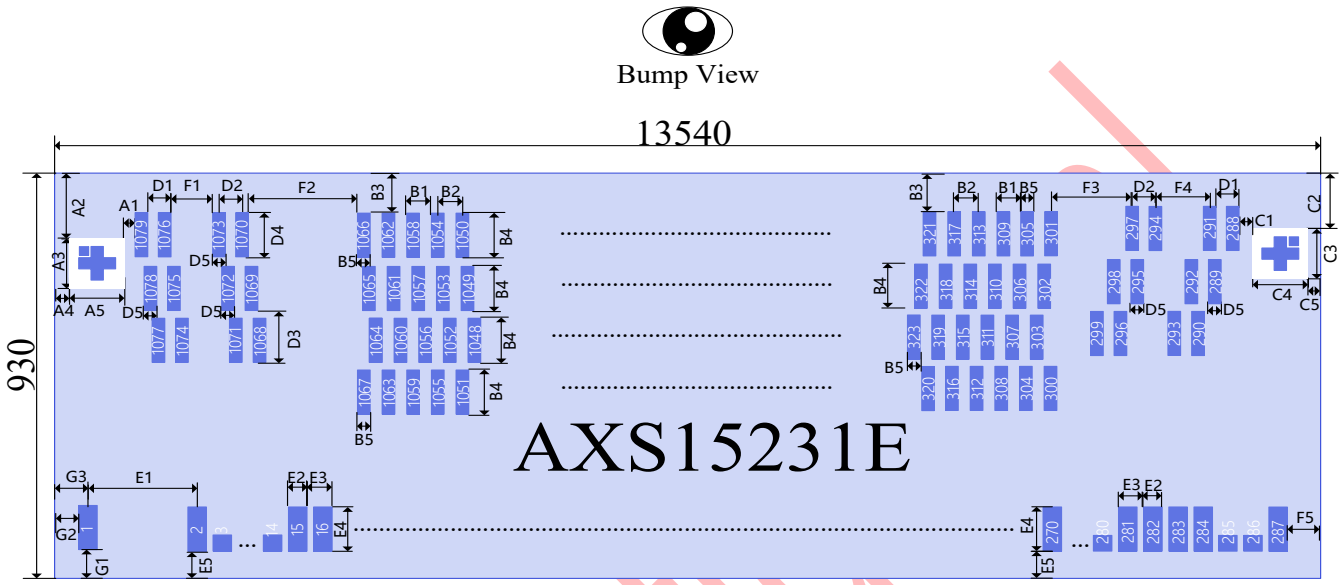
9. CHIP IMFORMATION

9.1. PAD Assignment



Symbol	Size	Symbol	Size	Symbol	Size	Symbol	Size	Symbol	Size
A1	43	A2	73	A3	80	A4	40	A5	80
B1	33	B2	33	B3	33	B4	75	B5	15
C1	43	C2	73	C3	80	C4	80	C5	40
D1	33	D2	33	D3	100	D4	75	D5	15
E1	553．5	E2	30	E3	45	E4	75	E5	33
F1	2112．5	F2	1432．5	F3	1247．5	F4	1320	F5	67．5
G1	33	G2	64	G3	79				
								Unit=um	

9.2. PAD Dimension

Item	PAD No.	Size		Unit
		X	Y	
Chip Size	-	13540	930	um
Chip thickness	-	200		
Pad Size	1 - 287	30	75	
	288 - 1097	15	75	
Pad Pitch	1 - 287	45		
	288 - 1097	11		

Note1: Chip size didn't include scribe line.

Note2: Have no Temperature compensation design.

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9.3. PAD CENTER COORDINATE

PAD No.	X	Y	PAD NAME
1	-7191	-394.5	DUMMY
2	-6637.5	-394.5	DUMMY
3	-6592.5	-394.5	
4	-6547.5	-394.5	
5	-6502.5	-394.5	
6	-6457.5	-394.5	
7	-6412.5	-394.5	
8	-6367.5	-394.5	
9	-6322.5	-394.5	
10	-6277.5	-394.5	
11	-6232.5	-394.5	
12	-6187.5	-394.5	
13	-6142.5	-394.5	
14	-6097.5	-394.5	
15	-6052.5	-394.5	DUMMY
16	-6007.5	-394.5	SCAN_MODE
17	-5962.5	-394.5	SCAN_EN
18	-5917.5	-394.5	VSSD
19	-5872.5	-394.5	VSSD
20	-5827.5	-394.5	VDD
21	-5782.5	-394.5	VDD
22	-5737.5	-394.5	VDD
23	-5692.5	-394.5	VDD
24	-5647.5	-394.5	VPP
25	-5602.5	-394.5	VPP
26	-5557.5	-394.5	RS
27	-5512.5	-394.5	IM<3>
28	-5467.5	-394.5	IM<2>
29	-5422.5	-394.5	SCAN_IN<0>
30	-5377.5	-394.5	SCAN_IN<1>
31	-5332.5	-394.5	SCAN_IN<2>
32	-5287.5	-394.5	SCAN_OUT<0>
33	-5242.5	-394.5	SCAN_OUT<1>
34	-5197.5	-394.5	SCAN_OUT<2>
35	-5152.5	-394.5	VDDI_DRV
36	-5107.5	-394.5	VDDI_DRV
37	-5062.5	-394.5	VSSD
38	-5017.5	-394.5	VSSD
39	-4972.5	-394.5	DB<17>

PAD No.	X	Y	PAD NAME
541	1317	394.5	S<377>
542	1306	294.5	S<376>
543	1295	194.5	S<375>
544	1284	94.5	SX<68>
545	1284	394.5	S<374>
546	1273	294.5	S<373>
547	1262	194.5	S<372>
548	1251	94.5	DUMMY
549	1251	394.5	S<371>
550	1240	294.5	S<370>
551	1229	194.5	S<369>
552	1218	94.5	SX<67>
553	1218	394.5	S<368>
554	1207	294.5	S<367>
555	1196	194.5	S<366>
556	1185	94.5	DUMMY
557	1185	394.5	S<365>
558	1174	294.5	S<364>
559	1163	194.5	S<363>
560	1152	94.5	SX<66>
561	1152	394.5	S<362>
562	1141	294.5	S<361>
563	1130	194.5	S<360>
564	1119	94.5	DUMMY
565	1119	394.5	S<359>
566	1108	294.5	S<358>
567	1097	194.5	S<357>
568	1086	94.5	SX<65>
569	1086	394.5	S<356>
570	1075	294.5	S<355>
571	1064	194.5	S<354>
572	1053	94.5	DUMMY
573	1053	394.5	S<353>
574	1042	294.5	S<352>
575	1031	194.5	S<351>
576	1020	94.5	SX<64>
577	1020	394.5	S<350>
578	1009	294.5	S<349>
579	998	194.5	S<348>

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40	-4927.5	-394.5	DB<16>
41	-4882.5	-394.5	DB<15>
42	-4837.5	-394.5	DB<14>
43	-4792.5	-394.5	DB<13>
44	-4747.5	-394.5	DB<12>
45	-4702.5	-394.5	DB<11>
46	-4657.5	-394.5	DB<10>
47	-4612.5	-394.5	DB<9>
48	-4567.5	-394.5	DB<8>
49	-4522.5	-394.5	DB<7>
50	-4477.5	-394.5	DB<6>
51	-4432.5	-394.5	DB<5>
52	-4387.5	-394.5	DB<4>
53	-4342.5	-394.5	DB<3>
54	-4297.5	-394.5	DB<2>
55	-4252.5	-394.5	DB<1>
56	-4207.5	-394.5	DB<0>
57	-4162.5	-394.5	HSYNC
58	-4117.5	-394.5	PCLK
59	-4072.5	-394.5	VSYNC_QSPI_DIN2
60	-4027.5	-394.5	DE_QSPI_DIN3
61	-3982.5	-394.5	VDDI_DRV
62	-3937.5	-394.5	VDDI_DRV
63	-3892.5	-394.5	VSSD
64	-3847.5	-394.5	VSSD
65	-3802.5	-394.5	DIN_SDA
66	-3757.5	-394.5	DIN_SDA_DUAL
67	-3712.5	-394.5	SCL
68	-3667.5	-394.5	CSX
69	-3622.5	-394.5	DUMMY
70	-3577.5	-394.5	DUMMY
71	-3532.5	-394.5	DUMMY
72	-3487.5	-394.5	CGOUT1_L<1>
73	-3442.5	-394.5	CGOUT1_L<2>
74	-3397.5	-394.5	CGOUT1_L<3>
75	-3352.5	-394.5	CGOUT1_L<4>
76	-3307.5	-394.5	CGOUT1_L<5>
77	-3262.5	-394.5	CGOUT1_L<6>
78	-3217.5	-394.5	CGOUT1_L<7>
79	-3172.5	-394.5	CGOUT1_L<8>
80	-3127.5	-394.5	CGOUT1_L<9>
81	-3082.5	-394.5	CGOUT1_L<10>

580	987	94.5	DUMMY
581	987	394.5	S<347>
582	976	294.5	S<346>
583	965	194.5	S<345>
584	954	94.5	SX<63>
585	954	394.5	S<344>
586	943	294.5	S<343>
587	932	194.5	S<342>
588	921	94.5	DUMMY
589	921	394.5	S<341>
590	910	294.5	S<340>
591	899	194.5	S<339>
592	888	94.5	SX<62>
593	888	394.5	S<338>
594	877	294.5	S<337>
595	866	194.5	S<336>
596	855	94.5	DUMMY
597	855	394.5	S<335>
598	844	294.5	S<334>
599	833	194.5	S<333>
600	822	94.5	SX<61>
601	822	394.5	S<332>
602	811	294.5	S<331>
603	800	194.5	S<330>
604	789	94.5	DUMMY
605	789	394.5	S<329>
606	778	294.5	S<328>
607	767	194.5	S<327>
608	756	94.5	SX<60>
609	756	394.5	S<326>
610	745	294.5	S<325>
611	734	194.5	S<324>
612	723	94.5	DUMMY
613	723	394.5	S<323>
614	712	294.5	S<322>
615	701	194.5	S<321>
616	690	94.5	SX<59>
617	690	394.5	S<320>
618	679	294.5	S<319>
619	668	194.5	S<318>
620	657	94.5	DUMMY
621	657	394.5	S<317>

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82	-3037.5	-394.5	CGOUT1_L<11>
83	-2992.5	-394.5	CGOUT1_L<12>
84	-2947.5	-394.5	DUMMY
85	-2902.5	-394.5	DUMMY
86	-2857.5	-394.5	VGL
87	-2812.5	-394.5	VGL
88	-2767.5	-394.5	VGL
89	-2722.5	-394.5	VGLO_L
90	-2677.5	-394.5	VGLO_L
91	-2632.5	-394.5	VGLO_L
92	-2587.5	-394.5	VDDI_LDO
93	-2542.5	-394.5	VDDI_LDO
94	-2497.5	-394.5	VDDI_LDO
95	-2452.5	-394.5	VDD
96	-2407.5	-394.5	VDD
97	-2362.5	-394.5	VDD
98	-2317.5	-394.5	VDD
99	-2272.5	-394.5	VSSD
100	-2227.5	-394.5	VSSD
101	-2182.5	-394.5	VSSA_2
102	-2137.5	-394.5	VSSA_2
103	-2092.5	-394.5	VCOM_PASS_L1
104	-2047.5	-394.5	VCOM_PASS_L1
105	-2002.5	-394.5	VGHO_L
106	-1957.5	-394.5	VGHO_L
107	-1912.5	-394.5	VSP
108	-1867.5	-394.5	VSP
109	-1822.5	-394.5	VSN
110	-1777.5	-394.5	VSN
111	-1732.5	-394.5	HS_DN
112	-1687.5	-394.5	HS_DN
113	-1642.5	-394.5	HS_DP
114	-1597.5	-394.5	HS_DP
115	-1552.5	-394.5	VSSD
116	-1507.5	-394.5	HS_CN
117	-1462.5	-394.5	HS_CN
118	-1417.5	-394.5	HS_CP
119	-1372.5	-394.5	HS_CP
120	-1327.5	-394.5	VSSD
121	-1282.5	-394.5	VSSD
122	-1237.5	-394.5	VSSD
123	-1192.5	-394.5	VDDI_M

622	646	294.5	S<316>
623	635	194.5	S<315>
624	624	94.5	SX<58>
625	624	394.5	S<314>
626	613	294.5	S<313>
627	602	194.5	S<312>
628	591	94.5	DUMMY
629	591	394.5	S<311>
630	580	294.5	S<310>
631	569	194.5	S<309>
632	558	94.5	SX<57>
633	558	394.5	S<308>
634	547	294.5	S<307>
635	536	194.5	S<306>
636	525	94.5	DUMMY
637	525	394.5	S<305>
638	514	294.5	S<304>
639	503	194.5	S<303>
640	492	94.5	SX<56>
641	492	394.5	S<302>
642	481	294.5	S<301>
643	470	194.5	S<300>
644	459	94.5	DUMMY
645	459	394.5	S<299>
646	448	294.5	S<298>
647	437	194.5	S<297>
648	426	94.5	SX<55>
649	426	394.5	S<296>
650	415	294.5	S<295>
651	404	194.5	S<294>
652	393	94.5	DUMMY
653	393	394.5	S<293>
654	382	294.5	S<292>
655	371	194.5	S<291>
656	360	94.5	SX<54>
657	360	394.5	S<290>
658	349	294.5	S<289>
659	338	194.5	S<288>
660	327	94.5	DUMMY
661	327	394.5	S<287>
662	316	294.5	S<286>
663	305	194.5	S<285>

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124	-1147.5	-394.5	VDDI_M
125	-1102.5	-394.5	VDDI_M
126	-1057.5	-394.5	VDDI_M
127	-1012.5	-394.5	POCN_VCI_PAD
128	-967.5	-394.5	POCN_VCI_PAD
129	-922.5	-394.5	POCN_VCI_PAD
130	-877.5	-394.5	OSC_IN
131	-832.5	-394.5	OSC_TE
132	-787.5	-394.5	GPIO<0>
133	-742.5	-394.5	GPIO<1>
134	-697.5	-394.5	VDDI_TP
135	-652.5	-394.5	VDDI_TP
136	-607.5	-394.5	VSSD
137	-562.5	-394.5	VSSD
138	-517.5	-394.5	GPIO<2>
139	-472.5	-394.5	GPIO<3>
140	-427.5	-394.5	DUMMY
141	-382.5	-394.5	GPIO<4>
142	-337.5	-394.5	GPIO<5>
143	-292.5	-394.5	GPIO<6>
144	-247.5	-394.5	GPIO<7>
145	-202.5	-394.5	VDDI_F
146	-157.5	-394.5	VDDI_F
147	-112.5	-394.5	VDDI_F
148	-67.5	-394.5	VDDI_F
149	-22.5	-394.5	ATEST5
150	22.5	-394.5	VSSD
151	67.5	-394.5	VSSD
152	112.5	-394.5	VSSD
153	157.5	-394.5	VDN
154	202.5	-394.5	VDN
155	247.5	-394.5	VDD
156	292.5	-394.5	VDD
157	337.5	-394.5	VDD
158	382.5	-394.5	VDD
159	427.5	-394.5	LED_PWM
160	472.5	-394.5	TE
161	517.5	-394.5	VDDI
162	562.5	-394.5	VDDI
163	607.5	-394.5	VDDI
164	652.5	-394.5	VDDI
165	697.5	-394.5	VCOM

664	294	94.5	SX<53>
665	294	394.5	S<284>
666	283	294.5	S<283>
667	272	194.5	S<282>
668	261	94.5	DUMMY
669	261	394.5	S<281>
670	250	294.5	S<280>
671	239	194.5	S<279>
672	228	94.5	SX<52>
673	228	394.5	S<278>
674	217	294.5	S<277>
675	206	194.5	S<276>
676	195	94.5	DUMMY
677	195	394.5	S<275>
678	184	294.5	S<274>
679	173	194.5	S<273>
680	162	94.5	SX<51>
681	162	394.5	S<272>
682	151	294.5	S<271>
683	140	194.5	DUMMY
684	-140	194.5	DUMMY
685	-151	294.5	S<270>
686	-162	394.5	S<269>
687	-162	94.5	SX<50>
688	-173	194.5	S<268>
689	-184	294.5	S<267>
690	-195	394.5	S<266>
691	-195	94.5	DUMMY
692	-206	194.5	S<265>
693	-217	294.5	S<264>
694	-228	394.5	S<263>
695	-228	94.5	SX<49>
696	-239	194.5	S<262>
697	-250	294.5	S<261>
698	-261	394.5	S<260>
699	-261	94.5	DUMMY
700	-272	194.5	S<259>
701	-283	294.5	S<258>
702	-294	394.5	S<257>
703	-294	94.5	SX<48>
704	-305	194.5	S<256>
705	-316	294.5	S<255>

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166	742.5	-394.5	VCOM
167	787.5	-394.5	VCOM
168	832.5	-394.5	VCOM
169	877.5	-394.5	VCI_A
170	922.5	-394.5	VCI_A
171	967.5	-394.5	VCI_A
172	1012.5	-394.5	VSSA_1
173	1057.5	-394.5	VSSA_1
174	1102.5	-394.5	VSSA_1
175	1147.5	-394.5	VBG_PAD
176	1192.5	-394.5	RF_CHECK
177	1237.5	-394.5	ATEST2
178	1282.5	-394.5	RSTN
179	1327.5	-394.5	IM<0>
180	1372.5	-394.5	VREF
181	1417.5	-394.5	VCI_C
182	1462.5	-394.5	VCI_C
183	1507.5	-394.5	VCI_C
184	1552.5	-394.5	VCI_C
185	1597.5	-394.5	VCI_C
186	1642.5	-394.5	VCI_C
187	1687.5	-394.5	VSSA_2
188	1732.5	-394.5	VSSA_2
189	1777.5	-394.5	VSSA_C
190	1822.5	-394.5	VSSA_C
191	1867.5	-394.5	VSSA_C
192	1912.5	-394.5	VSSA_C
193	1957.5	-394.5	VDDA_TP
194	2002.5	-394.5	VDDA_TP
195	2047.5	-394.5	VDDA_TP
196	2092.5	-394.5	ATEST3
197	2137.5	-394.5	ATEST3
198	2182.5	-394.5	ATEST3
199	2227.5	-394.5	VGL
200	2272.5	-394.5	VGL
201	2317.5	-394.5	VGL
202	2362.5	-394.5	VGL
203	2407.5	-394.5	VGL
204	2452.5	-394.5	VGL
205	2497.5	-394.5	VSN
206	2542.5	-394.5	VSN
207	2587.5	-394.5	VSN

706	-327	394.5	S<254>
707	-327	94.5	DUMMY
708	-338	194.5	S<253>
709	-349	294.5	S<252>
710	-360	394.5	S<251>
711	-360	94.5	SX<47>
712	-371	194.5	S<250>
713	-382	294.5	S<249>
714	-393	394.5	S<248>
715	-393	94.5	DUMMY
716	-404	194.5	S<247>
717	-415	294.5	S<246>
718	-426	394.5	S<245>
719	-426	94.5	SX<46>
720	-437	194.5	S<244>
721	-448	294.5	S<243>
722	-459	394.5	S<242>
723	-459	94.5	DUMMY
724	-470	194.5	S<241>
725	-481	294.5	S<240>
726	-492	394.5	S<239>
727	-492	94.5	SX<45>
728	-503	194.5	S<238>
729	-514	294.5	S<237>
730	-525	394.5	S<236>
731	-525	94.5	DUMMY
732	-536	194.5	S<235>
733	-547	294.5	S<234>
734	-558	394.5	S<233>
735	-558	94.5	SX<44>
736	-569	194.5	S<232>
737	-580	294.5	S<231>
738	-591	394.5	S<230>
739	-591	94.5	DUMMY
740	-602	194.5	S<229>
741	-613	294.5	S<228>
742	-624	394.5	S<227>
743	-624	94.5	SX<43>
744	-635	194.5	S<226>
745	-646	294.5	S<225>
746	-657	394.5	S<224>
747	-657	94.5	DUMMY

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208	2632.5	-394.5	VGLO
209	2677.5	-394.5	VGLO
210	2722.5	-394.5	POR_MODE_SEL_PAD
211	2767.5	-394.5	BGR_CORE_SEL_PAD
212	2812.5	-394.5	BGR_CORE_SEL_PAD
213	2857.5	-394.5	BGR_CORE_SEL_PAD
214	2902.5	-394.5	BGR_CORE_NPN_SEL_PAD
215	2947.5	-394.5	DUMMY
216	2992.5	-394.5	CGOUT_R<12>
217	3037.5	-394.5	CGOUT_R<11>
218	3082.5	-394.5	CGOUT_R<10>
219	3127.5	-394.5	CGOUT_R<9>
220	3172.5	-394.5	CGOUT_R<8>
221	3217.5	-394.5	CGOUT_R<7>
222	3262.5	-394.5	CGOUT_R<6>
223	3307.5	-394.5	CGOUT_R<5>
224	3352.5	-394.5	CGOUT_R<4>
225	3397.5	-394.5	CGOUT_R<3>
226	3442.5	-394.5	CGOUT_R<2>
227	3487.5	-394.5	CGOUT_R<1>
228	3532.5	-394.5	VGHO
229	3577.5	-394.5	VGHO
230	3622.5	-394.5	VGHO
231	3667.5	-394.5	VSSA_2
232	3712.5	-394.5	VSSA_2
233	3757.5	-394.5	VSSA_C
234	3802.5	-394.5	VSSA_C
235	3847.5	-394.5	VCI_C
236	3892.5	-394.5	VCI_C
237	3937.5	-394.5	VCI_C
238	3982.5	-394.5	VCI_C
239	4027.5	-394.5	VREF_TP
240	4072.5	-394.5	VREF_TP
241	4117.5	-394.5	VCG_TP
242	4162.5	-394.5	VCG_TP
243	4207.5	-394.5	ATEST1
244	4252.5	-394.5	ATEST0
245	4297.5	-394.5	VSP
246	4342.5	-394.5	VSP
247	4387.5	-394.5	VSP
248	4432.5	-394.5	VSP
249	4477.5	-394.5	VSSD

748	-668	194.5	S<223>
749	-679	294.5	S<222>
750	-690	394.5	S<221>
751	-690	94.5	SX<42>
752	-701	194.5	S<220>
753	-712	294.5	S<219>
754	-723	394.5	S<218>
755	-723	94.5	DUMMY
756	-734	194.5	S<217>
757	-745	294.5	S<216>
758	-756	394.5	S<215>
759	-756	94.5	SX<41>
760	-767	194.5	S<214>
761	-778	294.5	S<213>
762	-789	394.5	S<212>
763	-789	94.5	DUMMY
764	-800	194.5	S<211>
765	-811	294.5	S<210>
766	-822	394.5	S<209>
767	-822	94.5	SX<40>
768	-833	194.5	S<208>
769	-844	294.5	S<207>
770	-855	394.5	S<206>
771	-855	94.5	DUMMY
772	-866	194.5	S<205>
773	-877	294.5	S<204>
774	-888	394.5	S<203>
775	-888	94.5	SX<39>
776	-899	194.5	S<202>
777	-910	294.5	S<201>
778	-921	394.5	S<200>
779	-921	94.5	DUMMY
780	-932	194.5	S<199>
781	-943	294.5	S<198>
782	-954	394.5	S<197>
783	-954	94.5	SX<38>
784	-965	194.5	S<196>
785	-976	294.5	S<195>
786	-987	394.5	S<194>
787	-987	94.5	DUMMY
788	-998	194.5	S<193>
789	-1009	294.5	S<192>

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250	4522.5	-394.5	VSSD
251	4567.5	-394.5	VSSD
252	4612.5	-394.5	VSSD
253	4657.5	-394.5	TS_SEL
254	4702.5	-394.5	IM<1>
255	4747.5	-394.5	WORK_MODE
256	4792.5	-394.5	DUMMY
257	4837.5	-394.5	S_TEST0
258	4882.5	-394.5	S_TEST1
259	4927.5	-394.5	S_TEST2
260	4972.5	-394.5	S_TEST3
261	5017.5	-394.5	DUMMY
262	5062.5	-394.5	IGZO_MODE
263	5107.5	-394.5	DUMMY
264	5152.5	-394.5	DUMMY
265	5197.5	-394.5	VDDI
266	5242.5	-394.5	VDDI
267	5287.5	-394.5	VDDI
268	5332.5	-394.5	VDD
269	5377.5	-394.5	VDD
270	5422.5	-394.5	VDD
271	5467.5	-394.5	
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279	5827.5	-394.5	
280	5872.5	-394.5	
281	5917.5	-394.5	VGH
282	5962.5	-394.5	VGH
283	6007.5	-394.5	VGL
284	6052.5	-394.5	VGL
285	6097.5	-394.5	
286	6142.5	-394.5	
287	6187.5	-394.5	DUMMY
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290	6077.5	194.5	DUMMY
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831	-1350	94.5	SX<32>

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297	4713.5	394.5	DUMMY
298	4702.5	294.5	DUMMY
299	4691.5	194.5	DUMMY
300	3466	94.5	DUMMY
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303	3444	194.5	DUMMY
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308	3400	94.5	DUMMY
309	3400	394.5	VCOM_PASS_R
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312	3367	94.5	SX<97>
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873	-1702	294.5	S<129>

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514	1537	294.5	S<397>
515	1526	194.5	S<396>
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517	1515	394.5	S<395>
518	1504	294.5	S<394>
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520	1482	94.5	SX<71>
521	1482	394.5	S<392>
522	1471	294.5	S<391>
523	1460	194.5	S<390>
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526	1438	294.5	S<388>
527	1427	194.5	S<387>
528	1416	94.5	SX<70>
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530	1405	294.5	S<385>
531	1394	194.5	S<384>
532	1383	94.5	DUMMY
533	1383	394.5	S<383>
534	1372	294.5	S<382>
535	1361	194.5	S<381>
536	1350	94.5	SX<69>
537	1350	394.5	S<380>
538	1339	294.5	S<379>
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540	1317	94.5	DUMMY

1042	-3268	394.5	S<7>
1043	-3268	94.5	DUMMY
1044	-3279	194.5	S<6>
1045	-3290	294.5	S<5>
1046	-3301	394.5	S<4>
1047	-3301	94.5	SX<5>
1048	-3312	194.5	S<3>
1049	-3323	294.5	S<2>
1050	-3334	394.5	S<1>
1051	-3334	94.5	SX<4>
1052	-3345	194.5	DUMMY
1053	-3356	294.5	DUMMY
1054	-3367	394.5	DUMMY
1055	-3367	94.5	SX<4>
1056	-3378	194.5	VCOM_PASS_L
1057	-3389	294.5	VCOM_PASS_L
1058	-3400	394.5	VCOM_PASS_L
1059	-3400	94.5	DUMMY
1060	-3411	194.5	DUMMY
1061	-3422	294.5	DUMMY
1062	-3433	394.5	DUMMY
1063	-3433	94.5	SX<3>
1064	-3444	194.5	DUMMY
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1066	-3466	394.5	DUMMY
1067	-3466	94.5	DUMMY
1068	-4884	194.5	DUMMY
1069	-4895	294.5	DUMMY
1070	-4906	394.5	DUMMY
1071	-4917	194.5	DUMMY
1072	-4928	294.5	DUMMY
1073	-4939	394.5	DUMMY
1074	-7044.5	194.5	DUMMY
1075	-7055.5	294.5	DUMMY
1076	-7066.5	394.5	DUMMY
1077	-7077.5	194.5	DUMMY
1078	-7088.5	294.5	DUMMY
1079	-7099.5	394.5	DUMMY

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