HD44102

(Dot Matrix Liquid Crystal Graphic Display Column Driver)

Description

The HD44102CH is a column (segment) driver for dot matrix liquid crystal graphic display systems, storing the display data transferred from a 4-bit or 8-bit microcomputer in the internal display RAM and generating dot matrix liquid crystal driving signals.

Each bit data of display RAM corresponds to on/off state of each dot of a liquid crystal display to provide more flexible than character display.

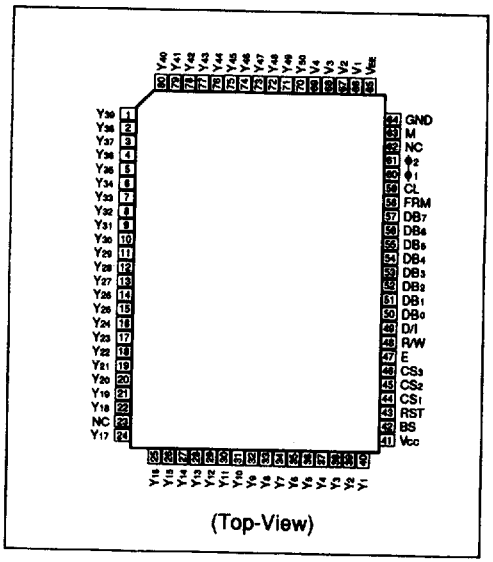
The HD44102CH is produced by the CMOS process. Therefore, the combination of HD44102CH with a CMOS microcontroller can complete portable battery-driven unit ntilizing the liquid crystal display's low power dissipation.

The combination of HD44102CH with the row (common) driver HD44103CH facilitates dot matrix liquid crystal graphic display system configuration.

Features

- Dot matrix liquid crystal graphic display column driver incorporating display RAM
- Interfaces with 4-bit or 8-bit MPU
- RAM data directly displayed by internal display RAM
  - RAM bit data 1: On
  - RAM bit data 0: Off
- Display RAM capacity: 50 × 8 × 4 (1600 bits)
- Internal liquid crystal display driver circuit (segment output): 50 segment signal drivers
- Duty factor (can be controlled by external input waveform)
  - Selectable duty factors: 1/8, 1/12, 1/16, 1/24, 1/32
- Wide range of instruction functions
  - Display Data Read/Write, Display On/Off, Set Address, Set Display
  - Start Page, Set Up/Down, Read Status
- Low power dissipation
- Power supplies: V_{CC} 5 V ± 10%, V_{EE} 0 to –5 V
- CMOS process

Pin Arrangement



(Top-View)

Ordering Information

Type No.	Package
HD44102CH	80-pin plastic QFP(FP-80)
HD44102D	chip

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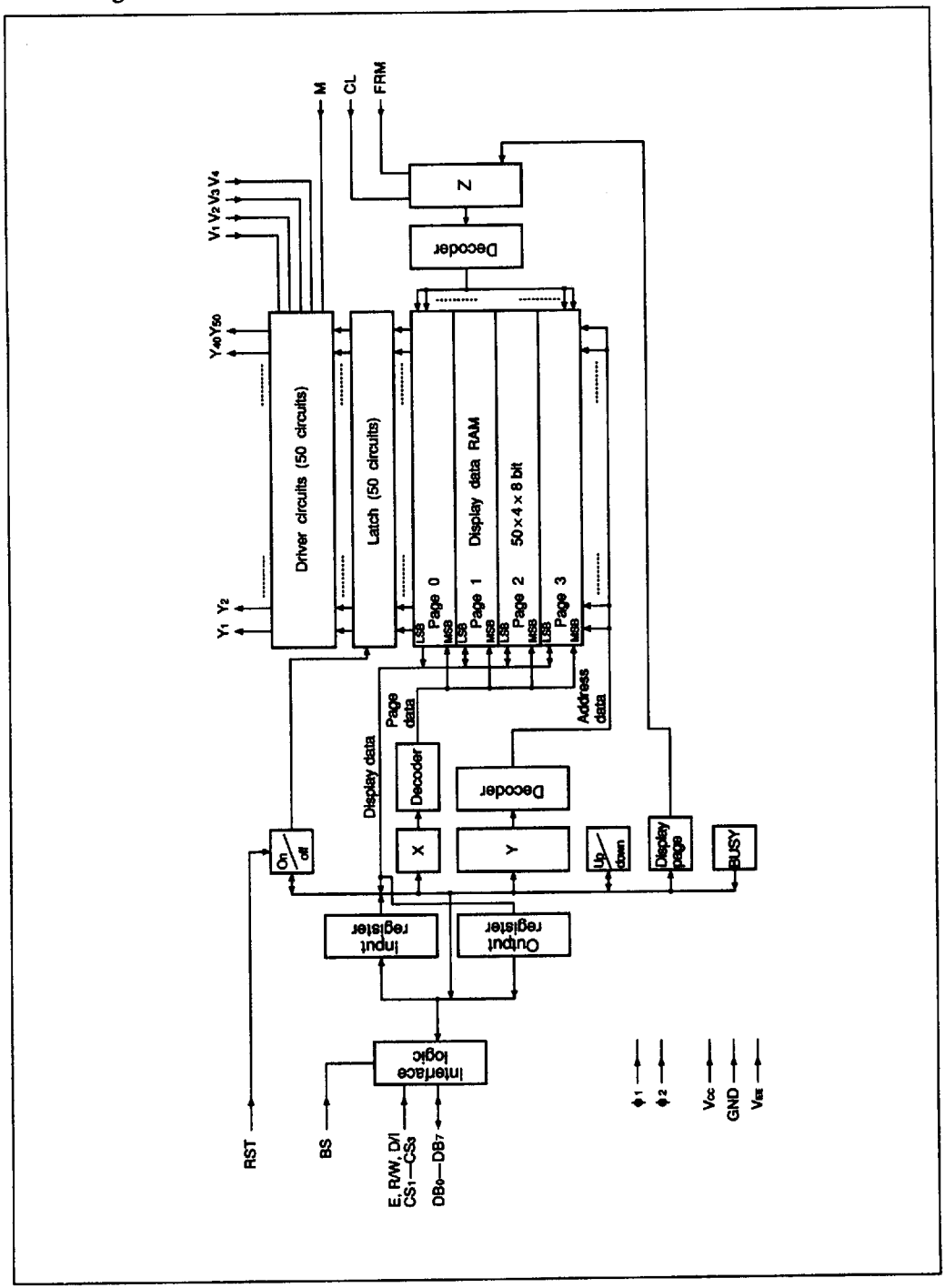
Block Diagram



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Absolute Maximum Ratings

Item	Symbol	Value	Unit	Notes
Supply voltage (1)	V_{CC}	−0.3 to +7.0	V	1
Supply voltage (2)	V_{EE}	V_{CC} −13.5 to V_{CC} + 0.3	V	
Input voltage (1)	V_{T1}	−0.3 to V_{CC} + 0.3	V	1, 2
Input voltage (2)	V_{T2}	V_{EE} −0.3 to V_{CC} + 0.3	V	3
Operating temperature	T_{opr}	−20 to +75	°C	
Storage temperature	T_{stg}	−55 to +125	°C	

Notes: 1. Referenced to GND = 0.
2. Applied to input terminals (except V1, V2, V3, and V4), and I/O common terminals.
3. Applied to terminals V1, V2, V3, and V4.

Electrical Characteristics

(V_{CC} = +5 V ±10%, GND = 0 V, V_{EE} = 0 to −5.5 V, Ta = −20 to 75 °C) (Note 4)

Item	Symbol	Min	Typ	Max	Unit	Test condition	Notes
Input high voltage (CMOS)	V_{IHC}	0.7 × V_{CC}	–	V_{CC}	V		5
Input low voltage (CMOS)	V_{ILC}	0	–	0.3 × V_{CC}	V		5
Input high voltage (TTL)	V_{IHT}	2.0	–	V_{CC}	V		6
Input low voltage (TTL)	V_{ILT}	0	–	+0.8	V		6
Output high voltage	V_{OH}	+3.5	–	–	V	I_{OH} = −250 µA	7
Output low voltage	V_{OL}	–	–	+0.4	V	I_{OL} = +1.6 mA	7
Vi-Xj ON resistance	R_{ON}	–	–	7.5	kΩ	V_{EE} = −5 V ± 10%, Load current 100 µA	
Input leakage current (1)	I_{IL1}	−1	–	1	µA	V_{IN} = V_{CC} to GND	8
Input leakage current (2)	I_{IL2}	−2	–	2	µA	V_{IN} = V_{CC} to V_{EE}	9
Operating frequency	f_{CLK}	25	–	280	kHz	φ1, φ2 frequency	10
Dissipation current (1)	I_{CC1}	–	–	100	µA	f_{clk} = 200 kHz frame = 65 Hz during display	11
Dissipation current (2)	I_{CC2}	–	–	500	µA	Access cycle 1 MHz at access	12

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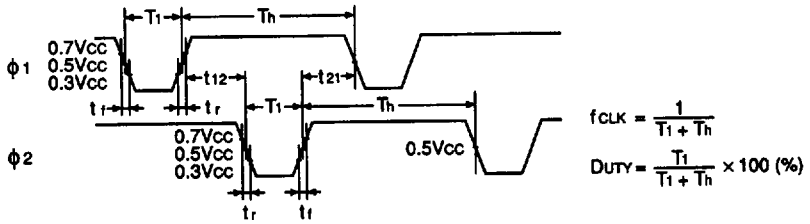
Notes: 4. Specified within this range unless otherwise noted.
5. Applied to M, FRM, CL, BS, RST,ϕ1, ϕ2.
6. Applied to CS1 to CS3, E, D/I, R/W and DBO to DB7.
7. Applied to DB0 to DB7.
8. Applied to input terminals, M, FRM,CL, BS, RST, ϕ1, ϕ2, CS1 to CS3, E, D/I and R/W, and I/O common terminals DB0 to DB7 at high impedance.
9. Applied to V1, V2, V3, and V4.
10. ϕ1 and ϕ2 AC characteristics.

	Symbol	Min	Typ	Max	Unit
Duty factor	Duty	20	25	30	%
Fall time	t_f	–	–	100	ns
Rise time	t_r	–	–	100	ns
Phase difference time	t_{12}	0.8	–	–	µs
Phase difference time	t_{21}	0.8	–	–	µs
$T_1 + T_h$		–	–	40	µs



11. Measured by V_{cc} terminal at no output load, at 1/32 dury factor, and frame frequency of 65 Hz, in checker pattern display. Access from the CPU is stopped.
12. Measured by V_{cc} terminal at no output load, 1/32 duty factor and frame frequency of 65 Hz.

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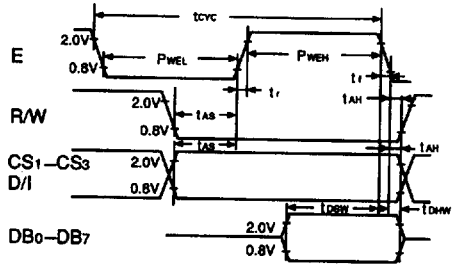
Interface AC Characteristics

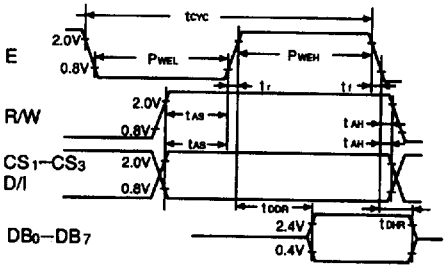
Item	Symbol	Min	Typ	Max	Unit	Notes
E cycle time	t_{CYC}	1000	–	–	ns	13, 14
E high level width	P_{WEH}	450	–	–	ns	13, 14
E low level width	P_{WEL}	450	–	–	ns	13, 14
E rise time	t_r	–	–	25	ns	13, 14
E fall time	t_f	–	–	25	ns	13, 14
Address setup time	t_{AS}	140	–	–	ns	13, 14
Address hold time	t_{AH}	10	–	–	ns	13, 14
Data setup time	t_{DSW}	200	–	–	ns	13
Data delay time	t_{DDR}	–	–	320	ns	14, 15
Data hold time at write	t_{DHW}	10	–	–	ns	13
Data hold time at read	t_{DHR}	20	–	–	ns	14

Notes:

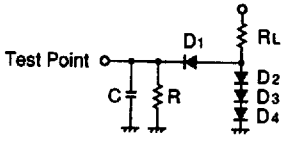
13. At CPU write



14. At CPU read



15. DB0 to DB7 load circuits



R_L = 2.4 kΩ
R = 11 kΩ
C = 130 pF (including jig capacitance)
Diodes D_1 to D_4 are all 1S2074 Ⓗ

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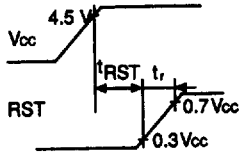
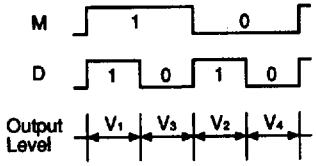
Notes: 16. Display off at initial power up.
The HD44102CH can be placed in the display off state by setting terminal RST to low at initial power up.
No instruction other than the Read Status can be accepted while the RST is at the low level.

	Symbol	Min	Typ	Max	Unit
Reset time	t_{RST}	1.0	–	–	µs
Rise time	t_r	–	–	200	ns



Pin Description

Pin Name	Pin Number	I/O	Function
Y1 – Y50	50	O	Liquid crystal display drive output. Relationship among output level, M and display data (D):



CS1 – CS3	3	I	Chip select

CS1	CS2	CS3	State
L	L	L	Non-selected
L	L	H	Non-selected
L	H	L	Non-selected
L	H	H	Selected read/write enable
H	L	L	Selected write enable only
H	L	H	Selected write enable only
H	H	L	Selected write enable only
H	H	H	Selected read/write enable

E	1	I	Enable At write (R/W = Low): Data of DB0 to DB7 is latched at the fall of E. At read (R/W = High): Data appears at DB0 to DB7 while E is at high level.

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Pin Name	Pin Number	I/O	Function
R/W	1	I	Read/Write R/W = High: Data appears at DB0 to DB7 and can be read by the CPU when E = high and CS2, CS3 = high. R/W = Low: DB0 to DB7 can accept input when CS2, CS3 = high or CS1 = high.
D/I	1	I	Data/Instruction D/I = High: Indicates that the data of DB0 to DB7 is display data. D/I = Low: Indicates that the data of DB0 to DB7 is display control data.
DB0–DB7	8	I/O	Data bus, three-state I/O common terminal

E	R/W	CS1	CS2	CS3	State of DB0 to DB7
H	H	*	H	H	Output state
*	L	H	*	*	Input state,
*	L	*	H	H	High impedance
Others					High impedance

M	1	I	Signal to convert liquid crystal display drive output to AC.
CL	1	I	Display synchronous signal At the rise of CL signal, the liquid crystal display drive signal corresponding to display data appears.
FRM	1	I	Display synchronous signal (frame signal) This signal presets the 5-bit display line counter and synchronizes a common signal with the frame timing when the FRM signal becomes high.
$\phi 1$, $\phi 2$	2	I	2-phase clock signal for internal operation The $\phi 1$ and ϕ 2 clocks are used to perform the operations (input/output of display data and execution of instructions) other than display.
RST	1	I	Reset signal The display disappears and Y address counter is set in the up counter state by setting the RST signal to low level. After releasing reset, the display off state and up mode is held until the state is changed by the instruction.
BS	1	I	Bus select signal BS = Low: DB0 to DB7 operate for 8–bit length. BS = High: DB4 to DB7 are valid for 4–bit length only. 8–bit data is accessed twice in the high and low order.
V1, V2, V3, V4	4		Power supply for liquid crystal display drive V1 and V2: Selection voltage V3 and V4: Non-selection voltage

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Pin Name	Pin Number	I/O	Function
V_{CC}	3		Power supply
GND			V_{CC}–GND: Power supply for internal logic
V_{EE}			V_{CC}–V_{EE}: Power supply for liquid crystal display drive circuit logic

Function of Each Block

Interface Logic

The HD44102CH can use the data bus in 4-bit or 8-bit word length to enable interface to a 4-bit or 8-bit CPU.

1. 4 bit mode (BS = High)
   8-bit data is transferred twice for every 4 bits through the data bus when the BS signal is high.

The data bus uses the high order 4 bits (DB4 to DB7). First, the high order 4 bits (DB4 to DB7 in 8-bit data length) are transferred and then the low order 4 bits (DB0 to DB3 in 8-bit data length).

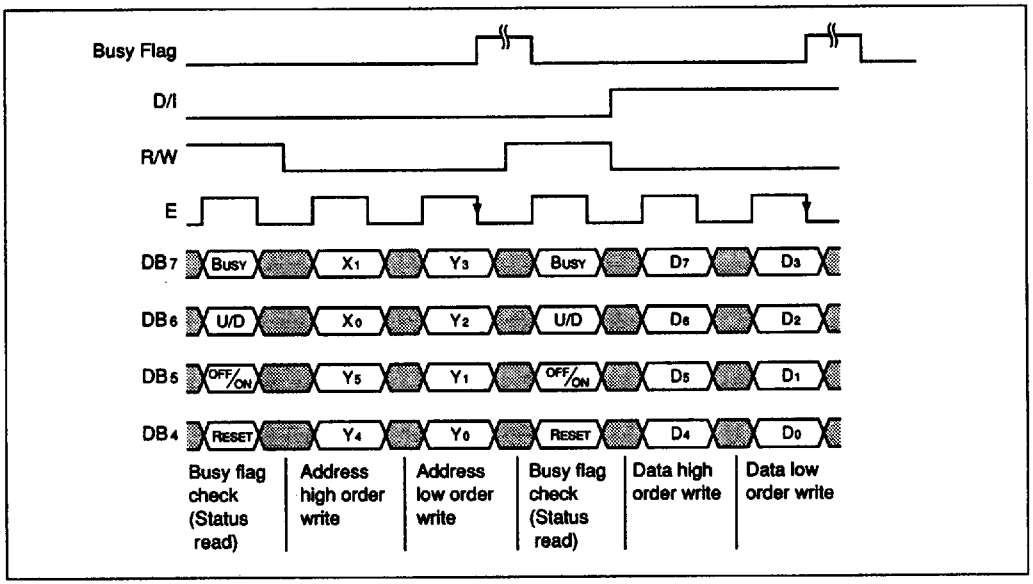

Figure 1 4-Bit Mode Timing

Note: Execute instructions other than status read in 4-bit length each. The busy flag is set at the fall of the second E signal. The status read is executed once. After the execution of the status read, the first 4 bits are considered the high order 4 bits. Therefore, if the busy flag is checked after the transfer of the high order 4 bits, retransfer data from the higher order bits. No busy check is required in the transfer between the high and low order bits.

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2. 8-bit mode (BS = Low)

If the BS signal is low, the 8 data bus lines (DB0 to DB7) are used for data transfer.

DB7: MSB (Most significant bit)

DB0: LSB (Least significant bit)

For AC timing, refer to note 12 to note 15 of "Electrical Characteristics".

Input Register

8-bit data is written into this register by the CPU. The instruction and display data are distinguished by the 8-bit data and D/I signal and then a given operation is performed. Data is received at the fall of the E signal when the CS is in the select state and R/W is in write state.

Output Register

The output register holds the data read from the display data RAM. After display data is read, the display data at the address now indicated is set in this output register. After that, the address is increased or decreased by 1. Therefore, when an address is set, the correct data doesn't appear at the read of the first display data. The data at a specified address appears at the second read of data (figure 2).

X, Y Address Counter

The X, Y address counter holds an address for reading/writing display data RAM. An address is set in it by the instruction. The Y address register is composed of a 50-bit up/down counter. The address is increased or decreased by 1 by the read/write operation of display data. The up/down mode can be determined by the instruction or RST signal. The Y address register counts by looping the values of 0 to 49. The X address register has no count function.

Display On/Off Flip/Flop

This flip/flop is set to on/off state by the instruction or RST signal. In the off state, the latch of display data RAM output is held reset and the display data output is set to 0. Therefore, display disappears. In the on state, the display data appears according to the data in the RAM and is displayed. The display data in the RAM is independent of the display on/off.

Up/Down Flip/Flop

This flip/flop determines the count mode of the Y address counter. In the up mode, the Y address register is increased by 1. 0 follows 49. In the down mode, the register is decreased by 1. 0 is followed by 49.

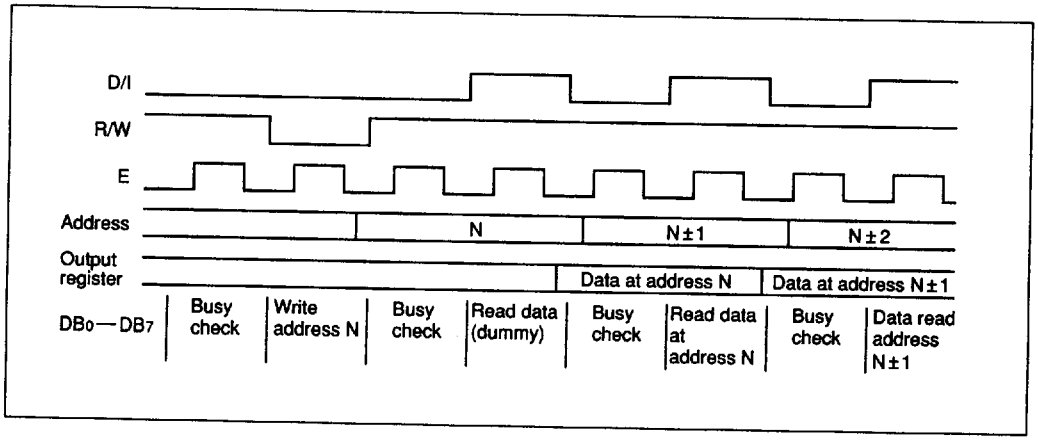

Figure 2 Data Output

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Display Page Register

The display page register holds the 2-bit data that indicates a display start page. This value is preset to the high order 2 bits of the Z address counter by the FRM signal. This value indicates the value of the display RAM page displayed at the top of the screen.

Busy Flag

After an instruction other than status read is accepted, the busy flag is set during its effective period, and reset when the instruction is not effective (figure 3). The value can be read out on DB7 by the status read instruction.
The HD44102CH cannot accept any other instructions than the status read in the busy state. Make sure the busy flag is reset before issuing an instruction.

Z Address Counter

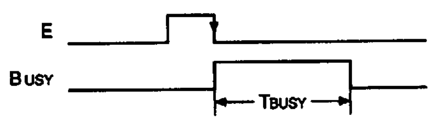
The Z address counter is a 5-bit counter that counts up at the fall of CL signal and generates an address for outputting the display data synchronized with the common signal. 0 is preset to the low order 3 bits and a display start page to the high order 2 bits by the FRM signal.

Latch

The display data from the display data RAM is latched at the rise of CL signal.

Liquid Crystal Driver Circuit

Each of 50 driver circuits is a multiplex circuit composed of 4 CMOS switches. The combination of display data from latchs and the M signal causes one of the 4 liquid crystal driver levels, V1, V2, V3 and V4 to be output.



$$\frac{1}{F\phi} \leq T_{BUSY} \leq \frac{3}{F\phi}$$

$F\phi$ is $\phi 1$, $\phi 2$ frequency (half of HD44103CH oscillation frequency)

Figure 3 Busy Flag

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Display RAM

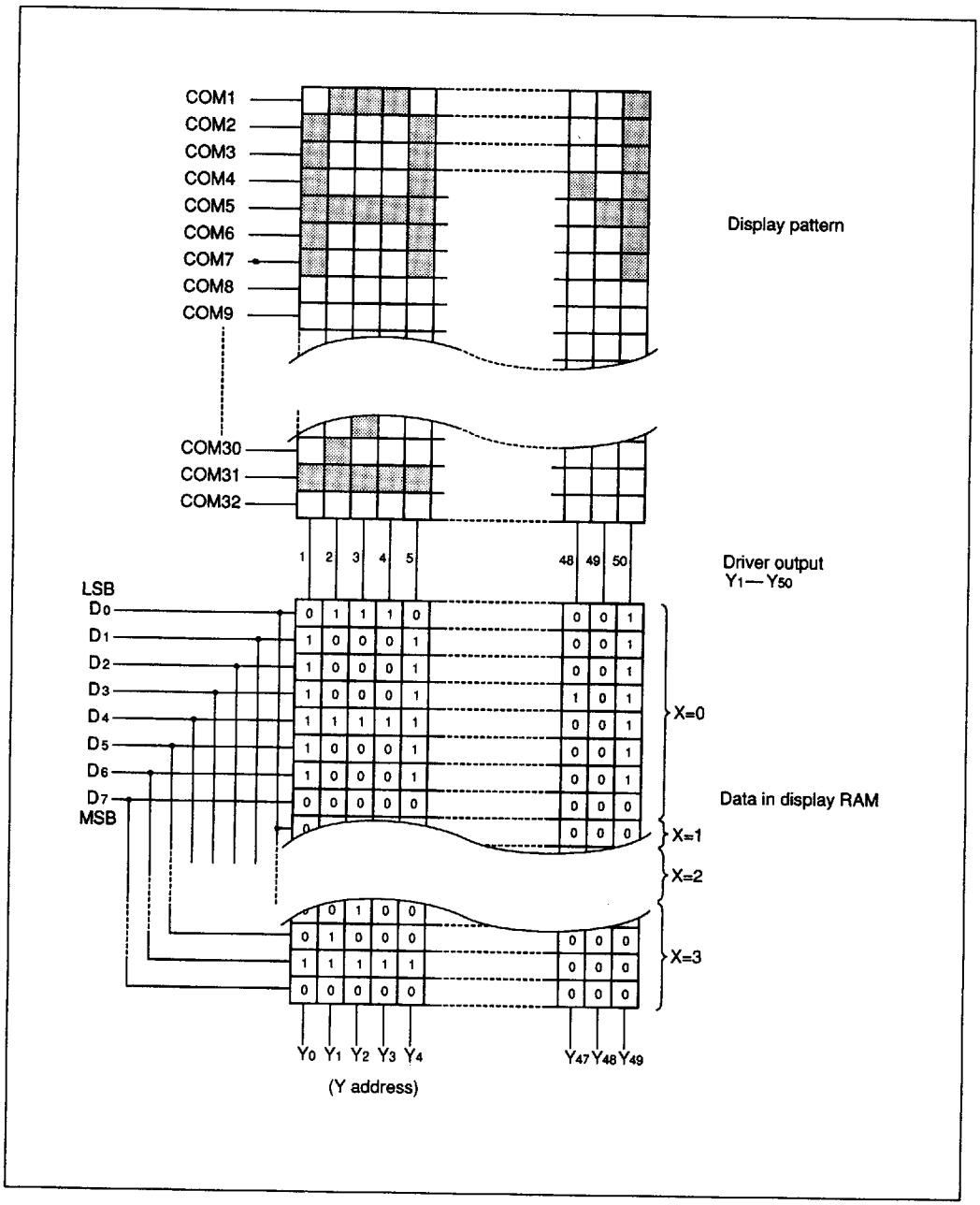

Figure 4 Relationship between Data in RAM and Display (Display start page 0, 1/32 duty)

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Display Control Instructions

Read/Write Display Data

		MSB			DB			LSB	
R/W	D/I	7	6	5	4	3	2	1	0
1	1	(Display data)							
		Read (CPU ← HD44102CH)							
0	1	(Display data)							
		Write (CPU →HD44102CH)							

Sends or receives data to or from the address of the display RAM specified in advance. However, a dummy read may be required for reading display data. Refer to the description of the output register in Function of Each Block.

Display On/Off

		MSB			DB			LSB	
R/W	D/I	7	6	5	4	3	2	1	0
0	0	0	0	1	1	1	0	0	1
0	0	0	0	1	1	1	0	0	0

Display on

Display off

Turns the display on/off. RAM data is not affected.

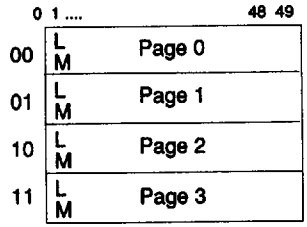
Set X/Y Address

		MSB			DB			LSB	
R/W	D/I	7	6	5	4	3	2	1	0
0	0	0	0						
0	0	0	1	Binary numbers of 0–49					
0	0	1	0						
0	0	1	1						

X address (page)

Y address (address)

Y address



Display Data RAM

Display Start Page

		MSB			DB			LSB	
R/W	D/I	7	6	5	4	3	2	1	0
0	0	0	0	1	1	1	1	1	0
		..... Refer to figure 5 (a)							
0	0	0	1	1	1	1	1	1	0
		..... Refer to figure 5 (b)							
0	0	1	0	1	1	1	1	1	0
		..... Refer to figure 5 (c)							
0	0	1	1	1	1	1	1	1	0
		Display start page							
		..... Refer to figure 5 (d)							

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Specifies the RAM page displayed at the top of the screen. Display is as shown in figure 4. When the display duty factor is more than 1/32 (For example, 1/24, 1/16), display begins at a page specified by the display start page only by the number of lines.

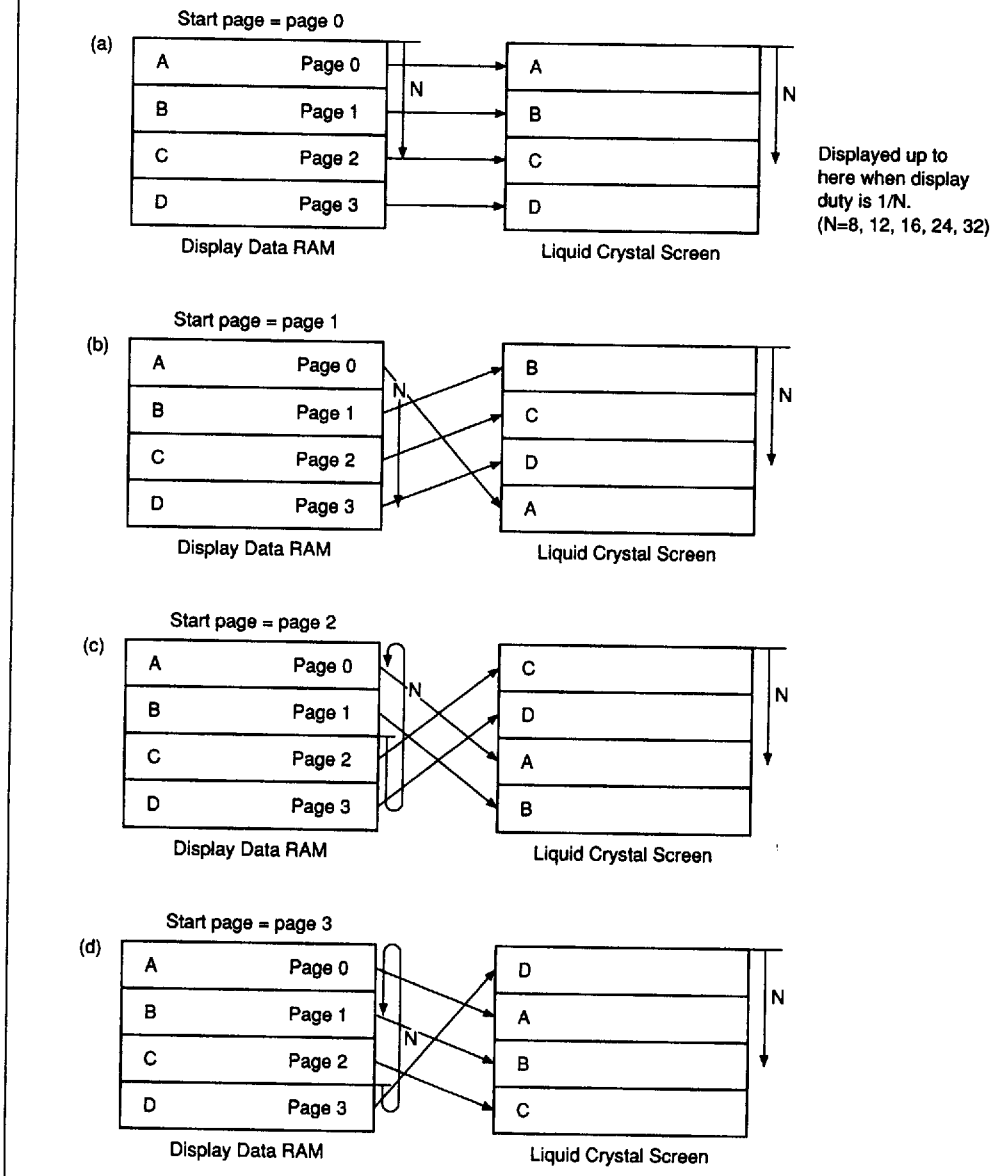

Figure 5 Display Start Page

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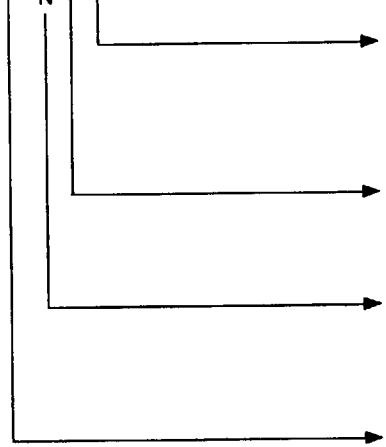
Up/Down Set

		MSB			DB			LSB	
R/W	D/I	7	6	5	4	3	2	1	0	
0	0	0	0	1	1	1	0	1	1	Up mode
0	0	0	0	1	1	1	0	1	0	Down mode

Sets Y address register in the up/down counter mode.

Status Read

		MSB			DB			LSB	
R/W	D/I	7	6	5	4	3	2	1	0
1	0	BUSY	UP/DOWN	OFF/ON	RESET	0	0	0	0



Goes to 1 when RST is in the reset state

(Busy also goes to 1).

Goes to 0 when RST is in the operating state.

Goes to 1 in the display off state.

Goes to 0 on the display on state.

Goes to 1 when address counter is in the up mode.

Goes to 0 when address counter is in the down mode.

Goes to 1 while all other instructions are being executed.

While 1, none of the other instructions are accepted.

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Connection Between LCD Drivers (Example of 1/32 Duty Factor)

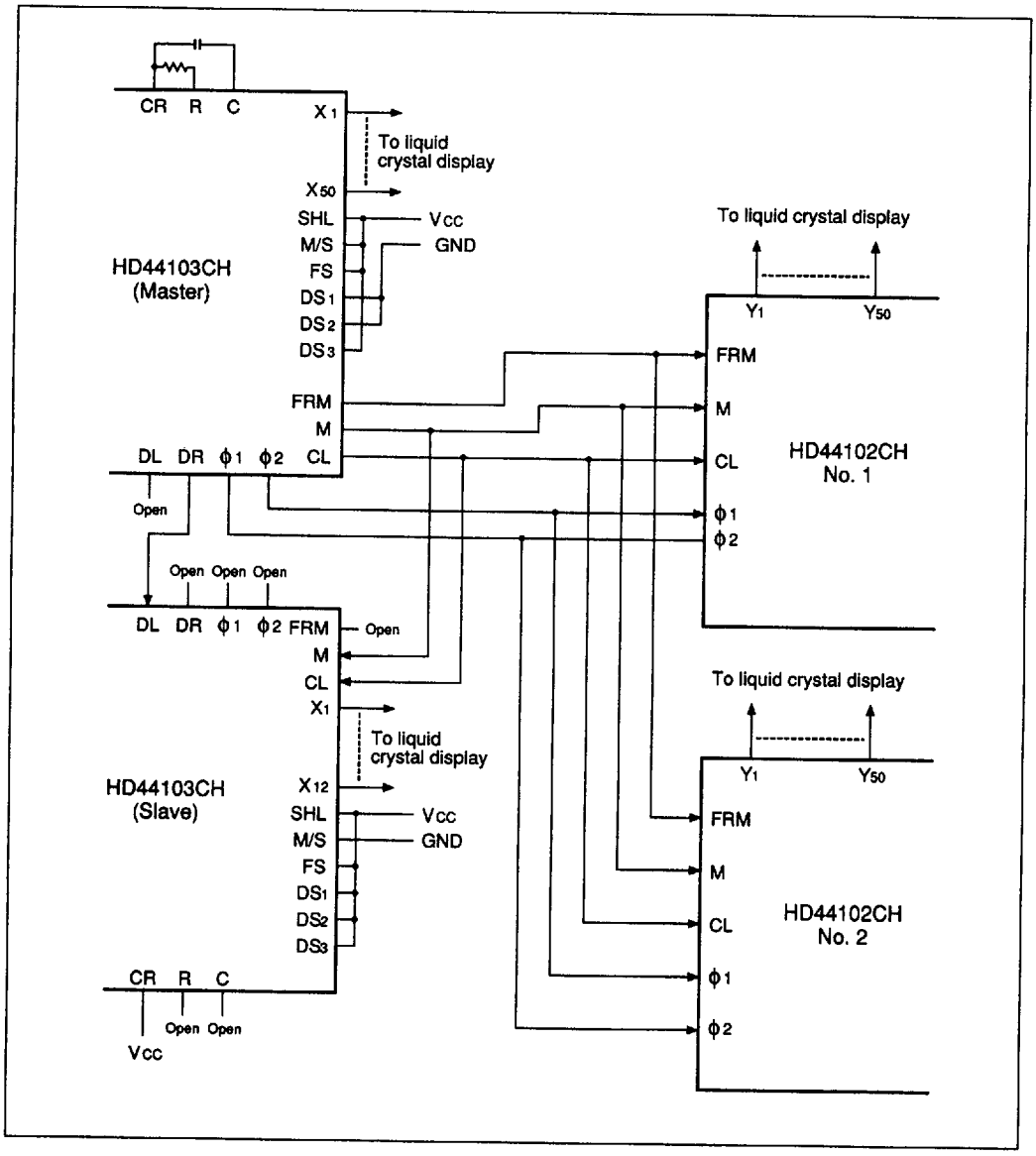

Figure 6 1/32 Duty Factor Connection Example

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Interface to CPU

1. Example of connection to HD6800

In the decoder given in this example, the addresses of HD44102CH in the address space of HD6800 are:
Read/write of display data: $'FFFF'
Write of display instruction: $'FFFE'
Read of status: $'FFFE'

Thus, the HD44102CH can be controlled by reading/writing data at these addresses.

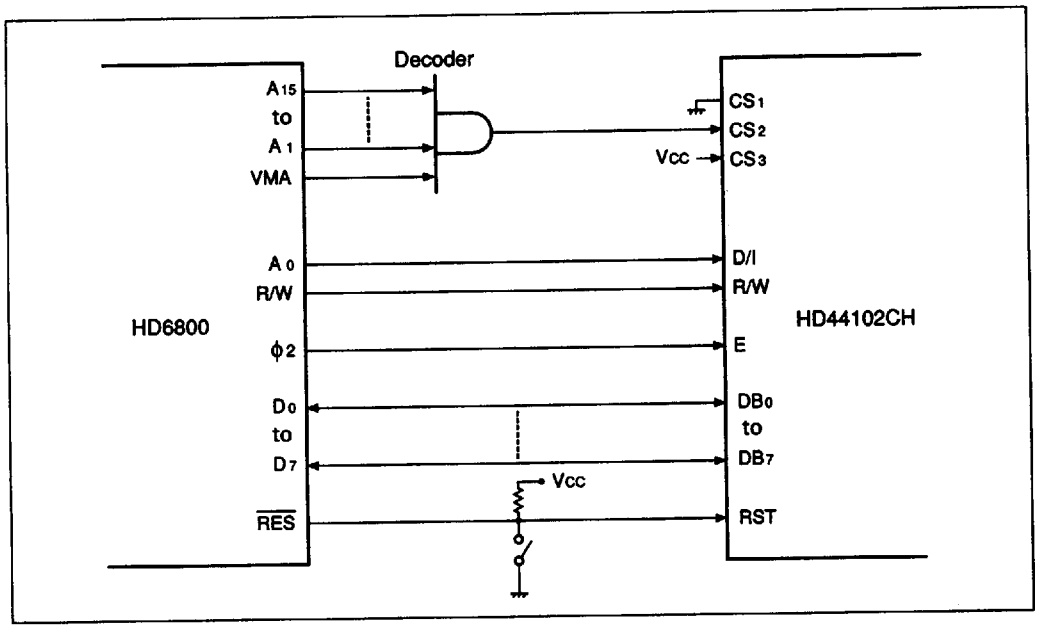

Figure 7 Example of Connection to HD6800 Series

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2. Example of connection to HD6801

- The HD6801 is set to mode 5. P10–P14 are used as output ports, and P30–P37 are used as the data bus.
- The 74LS154 is a 4–to–16 decoder that decodes 4 bits of P10–P13 to select the chips.
- Therefore, the HD44102CH can be controlled by selecting the chips through P10–P13 and specifying the D/I signal through P14 in advance, and later conducting memory read or write for external memory space $0100 to $01FF of HD6801. The IOS signal is output to SC1, and the R/W signal is output to SC2.
- For further details on HD6800 and HD6801, refer to their manuals.

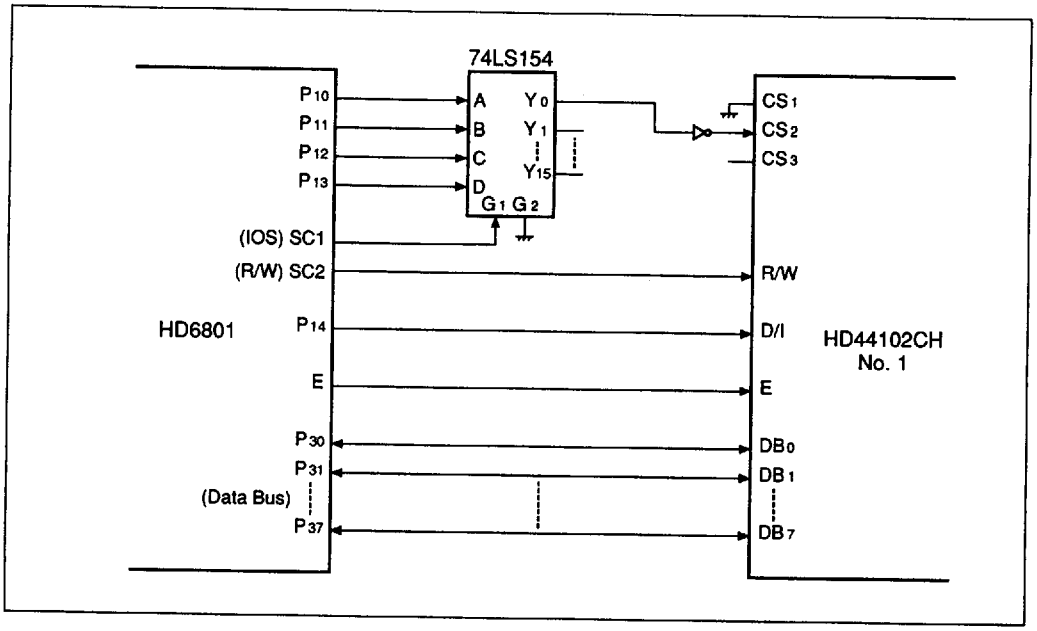

Figure 8 Example of Connection to HD6801

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Connection to Liquid Crystal Display

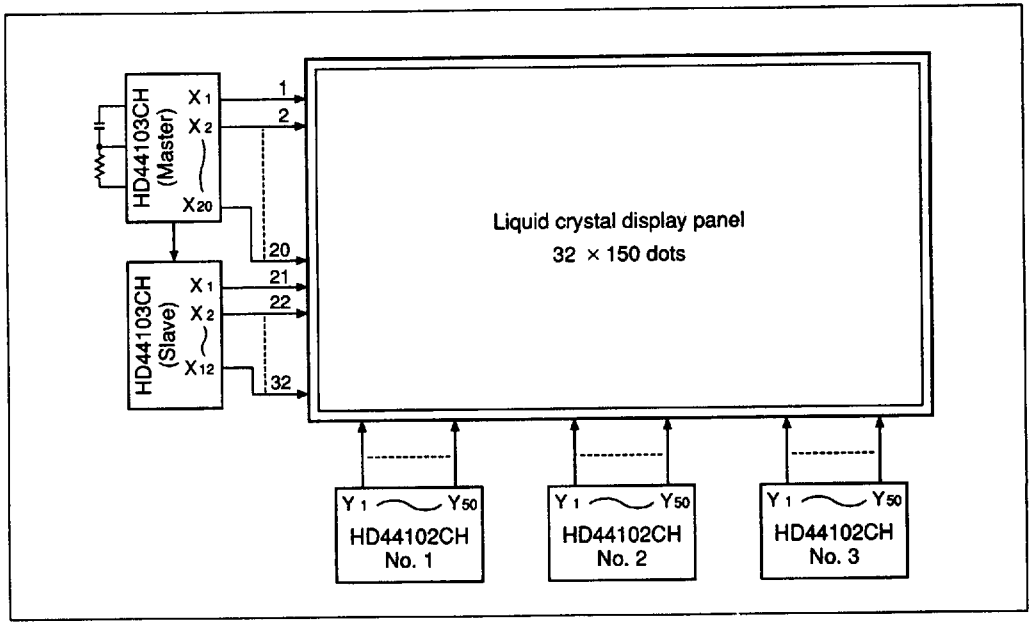

Figure 9 Example of Connection to 1/32 Duty Factor, 1-Screen Display

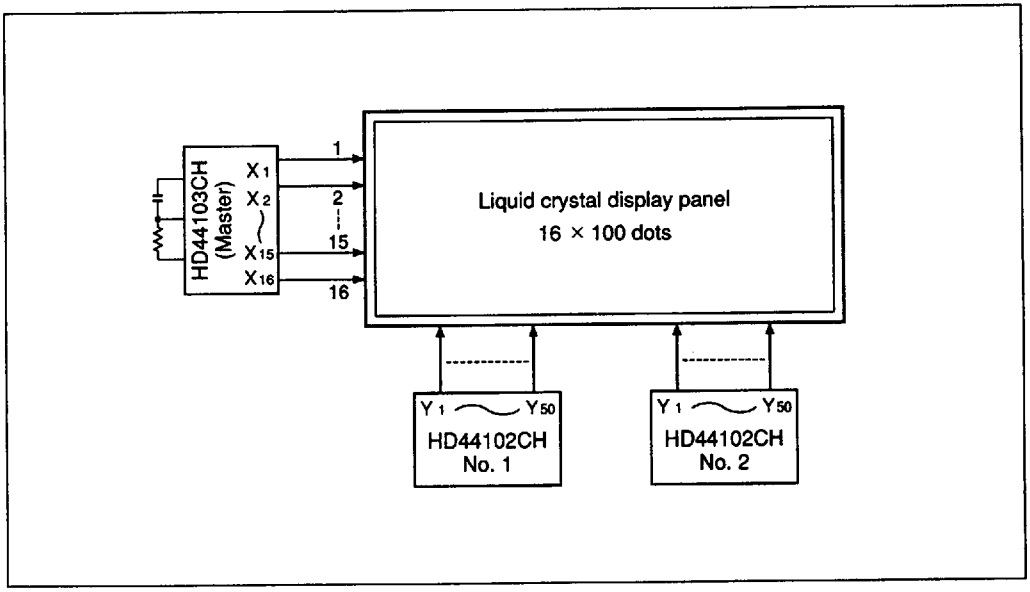

Figure 10 Example of Connection to 1/16 Duty Factor, 1–Screen Display

HITACHI
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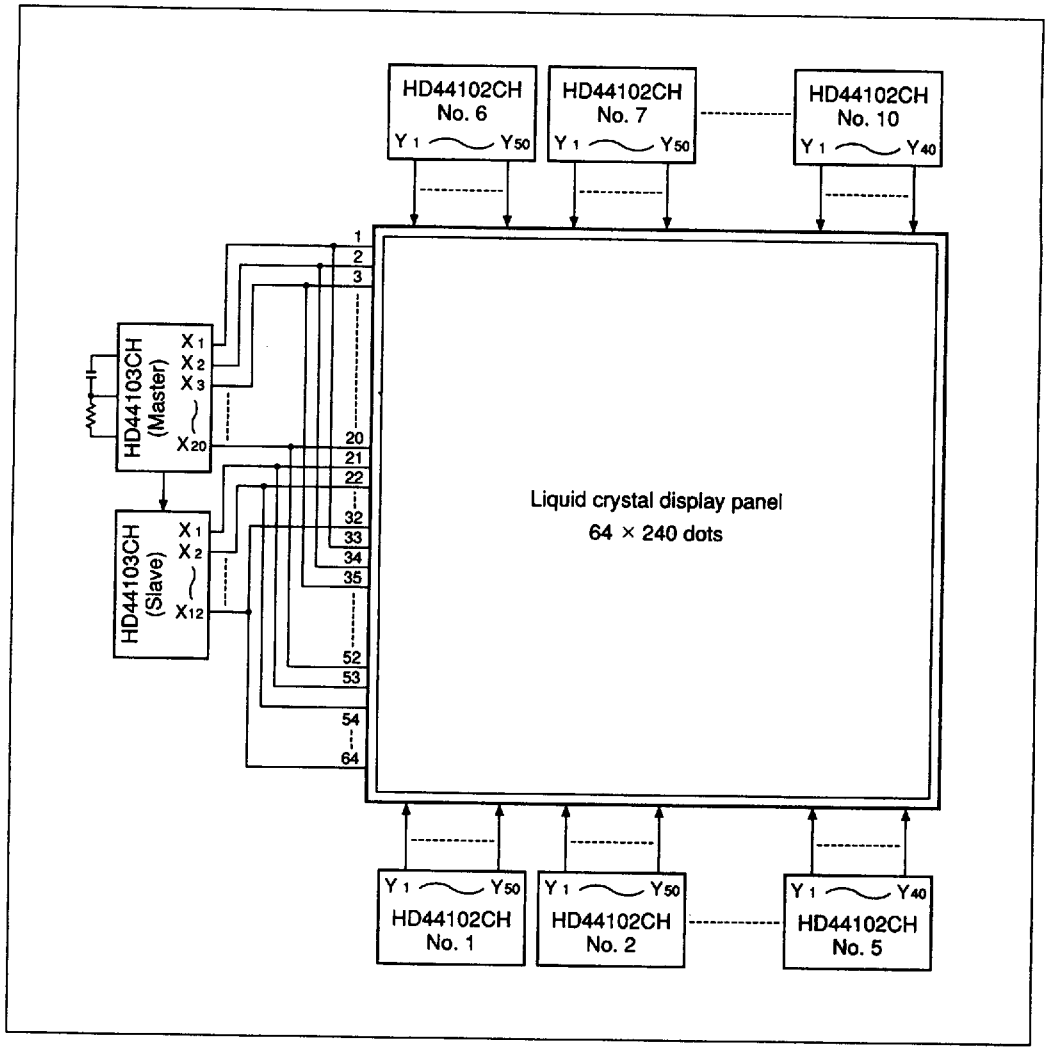

Figure 11 Example of Connection to 1/32 Duty Factor, 2-Screen Display

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Limitations on Using 4-Bit Interface Function

The HD44102 usuallly transfers display control data and display data via 8-bit data bus. It also has the 4-bit interface function in which the HD44102 transfers 8-bit data by dividing it into the high-order 4 bits and the low-order 4-bits in order to reduce the number of wires to be connected. You should take an extra care in using the application with the 4-bit interface function since it has the following limitations.

Limitations

The HD44102 is designed to transfer the high-order 4-bits and the low-order 4-bits of data in that order after busy check. The LSI does not work normally if the signals are in the following state for the time period (indicated with (*) in fifure 11) from when the high-order 4 bits are written (or read) to when the low-order 4 bits are written (or read); R/W = high and D/I = low while the chip is being selected (CS1 = high and CS2 = CS3 = don't care, or CS1 = low and CS2 = CS3 = high).

If the signals are in the limited state mentioned before for the time period indicated with (*) the LSI does not work normally. Please do not make the signals indicated with dotted lines simultaneously. As far as the time period indicated with (**), there is no problem.

The following explains how the malfunction is caused and gives the measures in application.

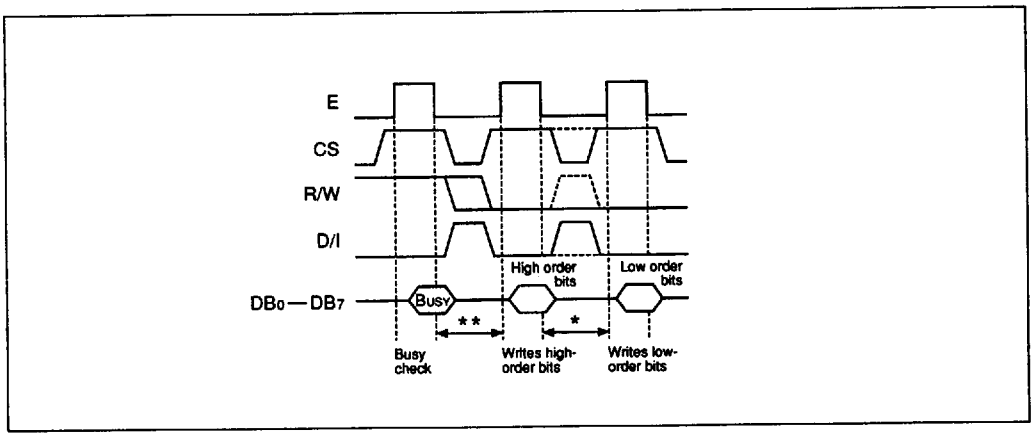

Figure 12 Example of Writing Display Control Instructions

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Cause

Busy check checks if the LSI is ready to accept the next instruction or display data by reading the status register to the HD44102. And at the same time, it resets the internal counter counting the order of high-order data and low-order data. This function makes the LSI ready to accept only the high-order data after busy check. Strictly speaking, if R/W = high and D/I = low while the chip is being selected, the internal counter is reset and the LSI gets ready to accept high-order bits. Therefore, the LSI takes low-order data for high-order data if the state mentioned above exist in the interval between transferring high-order data and transferring low-order data.

Measures in Application

1. HD44102 Controlled Via Port

When you control the HD44102 with the port of a single-chip microcomputer, you should take care of the software and observe the limitations strictly.

2. HD44102 Controlled Via Bus

a. Malfunction Caused by Hazard

Hazard of input signals may also cause the phenomenon mentioned before. The phase shift at transition of the input signals may cause the malfunction and so the AC characteristics must be carefully studied.

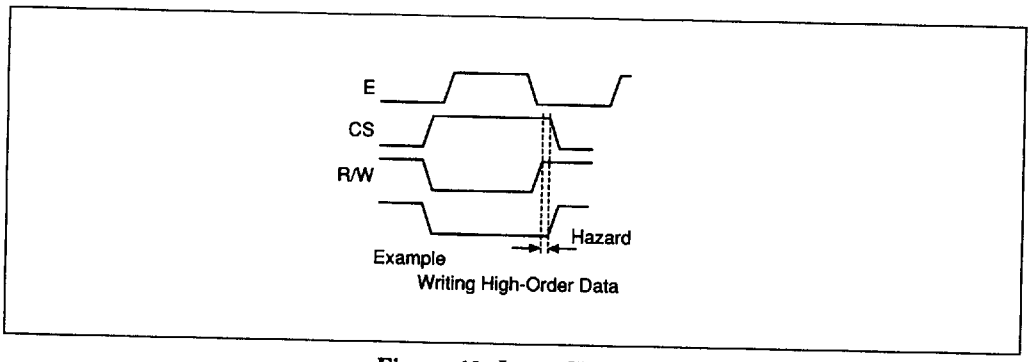

Figure 13 Input Hazard

b. Using 2-Byte Instruction

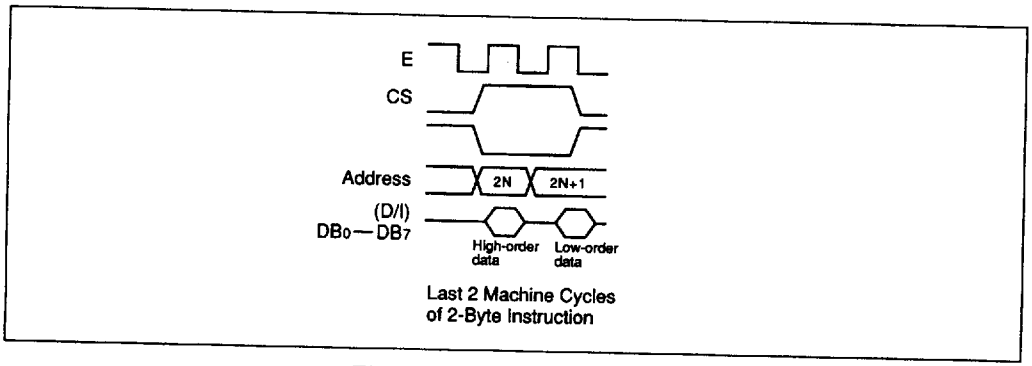

Figure 14 2-Byte Instruction

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In an application with the HD6303, you can prevent malfunction by using 2-byte instructions such as STD and STX. This is because the high-order and low-order data are accessed in that order without a break in the last machine cycle of the instruction and R/W and D/I do not change in the meantime. However, you cannot use the least significant bit of the address signals as the D/I signal since the address for the second byte has an added 1. Design the CS decoder so that the addresses for the HD44102 should be 2N and 2N + 1, and that those addresses should be accessed when using 2-byte instructions. For example, in figure 14 the address signal A_1 is used as D/I signal and A_2 –A_{15} are used for the CS decoder. Addresses 4N and 4N + 1 are for instruction access and addresses 4N + 2 and 4N + 3 are for display data access.

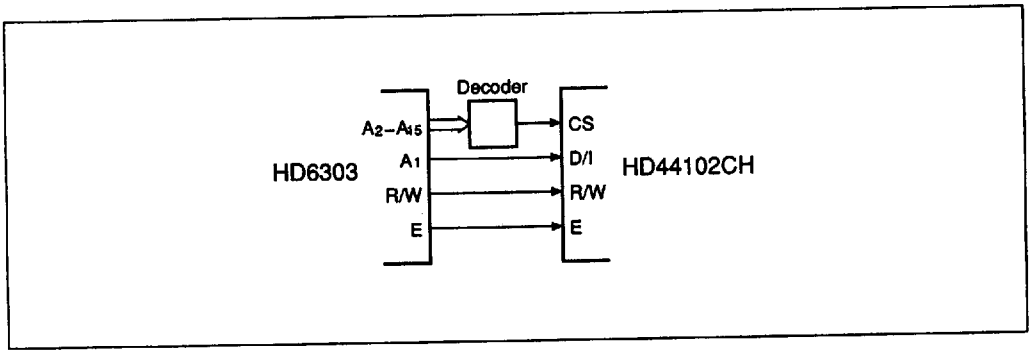

Figure 15 HD6303 Interface

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