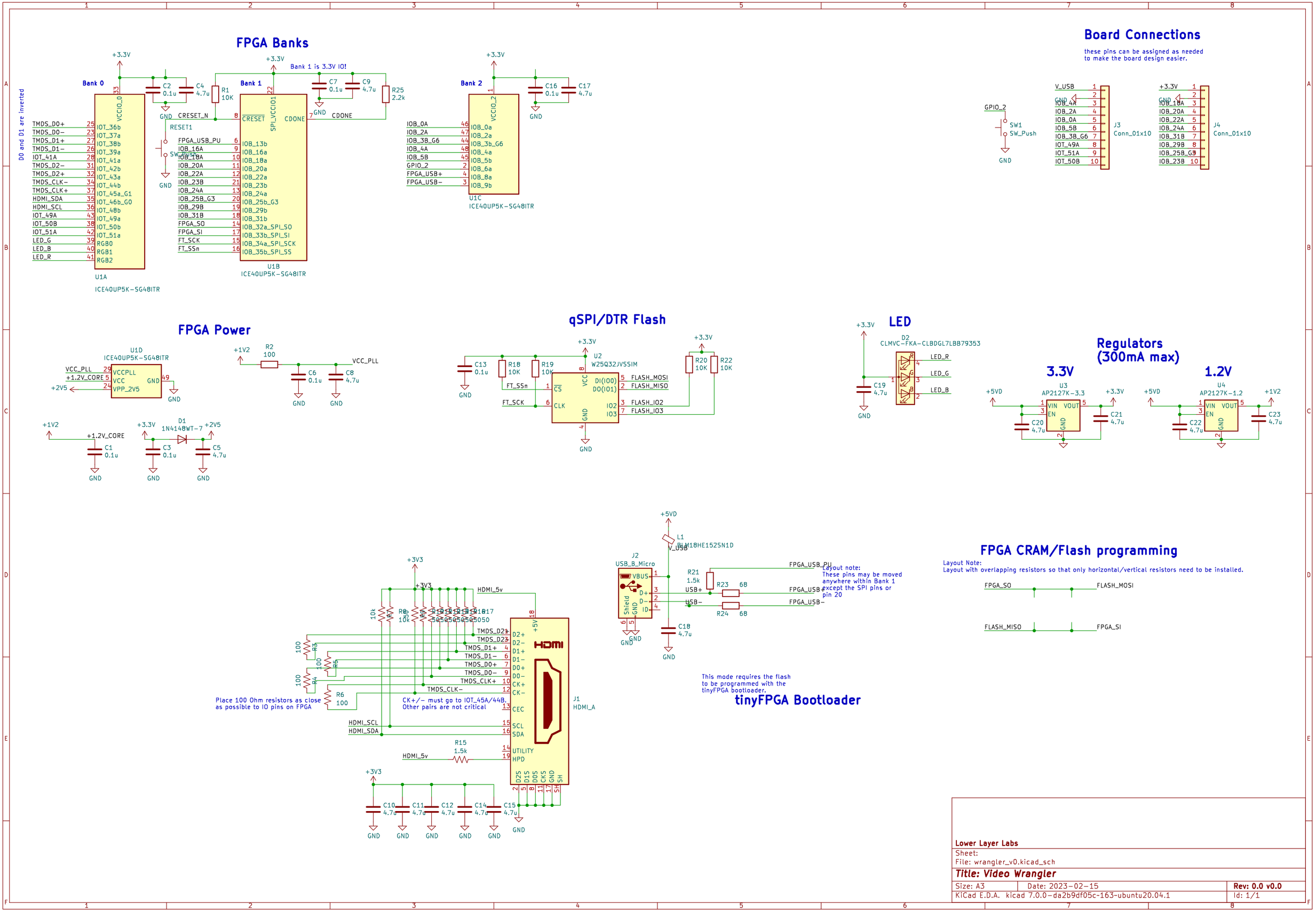
FPGA Banks
Bank 0
Bank 1
Bank 2
Bank 1 is 3.3V IO!
D0 and D1 are inverted
U1A
ICE40UP5K-SG48ITR
U1B
ICE40UP5K-SG48ITR
U1C
ICE40UP5K-SG48ITR
Board Connections
these pins can be assigned as needed
to make the board design easier.
J3
Conn_01x10
J4
Conn_01x10
FPGA Power
U1D
ICE40UP5K-SG48ITR
qSPI/DTR Flash
U2
W25Q32JVSSIM
LED
D2
CLMVC-FKA-CLBDGL7LBB79353
Regulators
(300mA max)
3.3V
U3
AP2127K-3.3
1.2V
U4
AP2127K-1.2
D1
1N4148WT-7
J1
HDMI_A
Place 100 Ohm resistors as close
as possible to IO pins on FPGA
CK+/- must go to IOT_45A/44B.
Other pairs are not critical
J2
USB_B_Micro
L1
BLM18HE152SN1D
Layout note:
These pins may be moved
anywhere within Bank 1
except the SPI pins or
pin 20
This mode requires the flash
to be programmed with the
tinyFPGA bootloader.
tinyFPGA Bootloader
FPGA CRAM/Flash programming
Layout Note:
Layout with overlapping resistors so that only horizontal/vertical resistors need to be installed.
Lower Layer Labs
Sheet:
File: wrangler_v0.kicad_sch
Title: Video Wrangler
Size: A3
Date: 2023-02-15
Rev: 0.0 v0.0
KiCad E.D.A. kicad 7.0.0-da2b9df05c-163~ubuntu20.04.1
Id: 1/1