OSTIVAL

Open Silicon Technology Integration For VLSI ASIC And LOGIC

figures/ostival-doc-cover.jpg

Team Ostival

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Preface

Welcome to the documentation for our open-source desktop GUI tool, **Ostival**, a comprehensive design environment built with Qt 6, inspired by the capabilities of industry-leading platforms.

As electronic design automation (EDA) is rapidly growing. Complex hardware system development is becoming increasingly challenging, and access to powerful, flexible, and accessible tools is paramount. This project was born from the vision of providing an open-source alternative that empowers students, researchers, and hobbyists to design, simulate, and analyze hardware implementation without the barriers of constantly proprietary software licenses.

This manual serves as your essential guide to navigating and harnessing the full potential of this GUI tool. Whether you are a seasoned professional transitioning from commercial EDA tools, a student learning the ropes of system design, or an enthusiast exploring new possibilities, this documentation will walk you through installation, core functionalities, advanced features, and customization options.

We believe that open-source software has the power to democratize technology and accelerate innovation. We encourage you to explore, experiment, and contribute to making this tool an indispensable asset for the global design community. Your participation is vital to its continued growth and success.

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Purpose Of The Manual

This manual serves as a comprehensive guide for users of the Ostival open-source tool, which enables the simulation of Verilog designs from high-level synthesis down to physical GDS-II layout.

The primary goal of this documentation is to empower you to:

Understand the Tool's Capabilities: Gain a clear insight into what Ostival can do, its core features, and the underlying open-source technologies it leverages (e.g., Icarus iVerilog, Yosys).

Navigate the Design Flow: Learn the step-by-step process of converting your Verilog Register-Transfer Level (RTL) code into a manufacturable GDS-II layout, including logic synthesis, place and route, and layout generation.

Effectively Use the Tool: Follow practical examples, tutorials, and command references to run your designs through the entire flow successfully.

Debug and Troubleshoot: Stuck somewhere? No problem! This document can help you identify common issues, understand error messages, and find solutions to ensure a smooth design experience.

Contribute to the Project (Optional): For advanced users and developers, this manual provides a comprehensive guide to every detail of the tool's architecture, allowing you to contribute to its ongoing development and improvement.

By providing detailed explanations, we aim to give the hardware development community a powerful open-source ASIC design flow tool, accessible to everyone, including students, researchers, hobbyists, and even professionals.

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Vision and Philosophy

Our vision for Ostival is to democratize ASIC design, making the journey from Verilog code to a physical chip layout accessible to everyone. We believe that robust, open-source tools are fundamental to fostering innovation, education, and collaboration in the world of silicon.

We are building this tool on the following core philosophies:

- **Openness and Accessibility:** We are committed to an entirely open-source approach, from the underlying design kits (like SkyWater SKY130) to every component of our toolchain. This ensures transparency, encourages scrutiny, and lowers the barrier to entry for individuals and small teams who might otherwise be excluded from chip design due to proprietary tool costs.
- **Integration and Cohesion:** Rather than developing every module from scratch, we strategically integrate and orchestrate best-in-class open-source EDA tools (such as Yosys, components of OpenRoad, Magic, and KLayout). Our philosophy is to provide a seamless, unified experience that simplifies the complex interactions between these powerful but disparate tools.
- **Usability and Documentation:** A powerful tool is only valuable if it can be used effectively. We prioritize clear, comprehensive documentation, intuitive workflows, and practical examples to ensure that users—from beginners to seasoned professionals—can quickly get started and achieve their design goals.
- **Community-Driven Development:** We believe in the power of collective effort. Ostival is a community project, and we welcome contributions, feedback, and ideas from users and developers worldwide. Together, we can build a tool that evolves with the needs of the open-source hardware community.
- **Reliability and Reproducibility:** We strive for a toolchain that produces consistent, reliable, and foundry-ready GDS-II outputs. Our aim is to provide a flow that you can trust for both learning and practical application, ensuring that what you simulate closely matches what can be fabricated.

Through these principles, Ostival aims to be more than just a piece of software; it aspires to be a catalyst for a new era of open hardware innovation.

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Target Audience

This manual is designed for anyone interested in exploring or engaging with the exciting field of open-source Application-Specific Integrated Circuit (ASIC) design. While our aims to simplify the complex process of chip layout, some foundational understanding of digital logic and hardware description languages (Verilog), and Python 3 programming language will be beneficial.

Specifically, this manual caters to:

- S**tudents and Educators:** Those learning digital design, VLSI concepts, or exploring the practical aspects of chip fabrication. The tool provides a hands-on platform to apply theoretical knowledge.
- **Hobbyists and Makers:** Individuals eager to design their custom silicon, prototype unique hardware ideas, or simply delve deeper into how chips are made without the prohibitive costs of commercial EDA tools.
- **Researchers:** Academics and industry researchers looking for an open, flexible, and reproducible flow for experimental chip designs, custom hardware acceleration, or exploring novel architectures.
- **Open-Source Hardware Developers:** Contributors to the broader open-source hardware ecosystem who wish to design, verify, and potentially fabricate their own integrated circuits using a transparent and accessible toolchain.
- **Digital Design Engineers:** Professionals with experience in FPGA or traditional ASIC design who are curious about open-source methodologies, seeking to port existing designs, or looking for an alternative flow for specific projects.

While we strive to make the process as intuitive as possible, this manual assumes a basic familiarity with command-line interfaces and fundamental digital logic concepts. No prior experience with GDS-II or specific EDA tools is required, as the manual will guide you through the entire process.

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Acknowledgments

This tool, Ostival, is the result of dedicated individual effort. However, its creation would not have been possible without the immense contributions of the broader open-source hardware and Electronic Design Automation (EDA) communities.

I extend my sincerest gratitude to:

- **The Developers and Communities Behind Core Open-Source EDA Tools:** A profound thank you to the creators and maintainers of indispensable projects such as iVerilog, Yosys, Netgen, Magic VLSI Layout Tool, KLayout, and others. These pioneering tools form the very backbone of Ostival, and their existence is a testament to the power of open collaboration.
- **The Qt Project and Community:** For providing the robust and versatile Qt cross-platform application framework. Its powerful libraries and tools have been instrumental in developing the user interface, facilitating the visualization components, and building the foundational utilities of this tool.
- **The SkyWater Technology and Google Teams, and the Open-Source PDK Community:** For their groundbreaking work in open-sourcing the SkyWater SKY130 Process Design Kit (PDK). This initiative has revolutionized accessibility to chip fabrication and provides the essential physical data that enables our synthesis-to-GDS-II flow.
- **The Entire Open-Source Hardware Ecosystem:** To the countless individuals, researchers, and organizations who contribute to open standards, share knowledge, and foster a spirit of innovation in hardware design. Your collective efforts inspire and empower projects like this one.

While I have undertaken the development of Ostival independently, the spirit of open collaboration and the availability of these incredible resources have been invaluable. Thank you for making this project possible.

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Chapter 1

Introduction