# Sadržaj

1	Power rails		
	1.1	Capacitance multiplier	
2	Offset results		
	2.1	10x gain enabled	
	2.2	1x gain enabled	
	2.3	solving	
3	Sources of offset		
	3.1	Input buffer	
		3.1.1 Input bias current offset	
		3.1.2 Input voltage offset	
	3.2	Output buffer	
		3.2.1 Input bias current offset	
		3.2.2 Input voltage offset	
4	Noise		
	4.1	Resistor noise	
	4.2	Input buffer noise	
	4.3	Output buffer noise	

# 1 Power rails

# 1.1 Capacitance multiplier

The goal is regulating the noisy 9V input to roughly 5V using a capacitance multiplier.

BD679 has minimal  $\beta_{hfe}$  of 750. If we assume the worst case current consumption of 20 mA, required base current is 27 uA. At this current, there is no eccessive  $V_{be}$  drop, so we can assume it is around 1.4 V.

Selecting resistors to overshadow the base current, means selecting their current to be 100x the base current, or 2.7 mA. At the 9V input, total resistance should be 3k.

Voltage divider should output 5 V + 1.4 V = 6.4V. 1 kOhm and 2.5 kOhm split generates 6.43V, perfect for our usecase.

## 2 Offset results

# 2.1 10x gain enabled

 $\text{-}8.5~\mathrm{mV}$ 

## 2.2 1x gain enabled

 $9.2~\mathrm{mV}$ 

## 2.3 solving

$$V_{off\_10} = 10 \cdot (2V_{in\_off} + V_{curr\_off}) + V_{out\_off}$$

$$\tag{1}$$

$$V_{off\_1} = 2V_{in\_off} + V_{curr\_off} + V_{out\_off}$$
 (2)

$$V_{off\_10} - V_{off\_1} = 9 \cdot (2V_{in\_off} + V_{curr\_off}) = -17.7 \text{mV}$$
 (3)

Total input offset is -2 mV. Total output offset is 11.2 mV.

## 3 Sources of offset

#### 3.1 Input buffer

## 3.1.1 Input bias current offset

AD8039 has an input bias current offset of 25nA, across the 20 k $\Omega$  input impedance, generates 0.5 mV of offset. Taking into account the second input buffer, maximimum offset is 1 mV.

#### 3.1.2 Input voltage offset

AD8039 has an max input voltage offset of 3mV. Worst case total offset is 6mV.

## 3.2 Output buffer

## 3.2.1 Input bias current offset

AD8009 has an max input current offset of 150 $\mu$ A. With an input impedance of 100  $\Omega$ , total offset is 15 mV. If both inputs have oposing offsets, the total offset is 30 mV

#### 3.2.2 Input voltage offset

AD8009 has an max input voltage offset of 5mV.

## 4 Noise

#### 4.1 Resistor noise

$$V_{rms} = \sqrt{4k_B T R \Delta f} \tag{4}$$

At the bandwidth of 100 MHz and temperature of 25  $^{\circ}$ C, noise is

$$V_{rms} = 3.63 \text{mV}_{RMS} \tag{5}$$

## 4.2 Input buffer noise

AD8039 has an input noise level of  $8 \text{nV} / \sqrt{\text{Hz}}$  meaning that total input noise rms at 100 MHz bandwidth is 80  $\mu V_{\text{RMS}}$ .

## 4.3 Output buffer noise

AD8009 has an input noise level of  $1.9 nV/\sqrt{Hz}$  meaning that total input noise rms at 100 MHz bandwidth is 19  $\mu V_{RMS}$ .