DS100M06VL

27. oktobar 2024.

Sadržaj

1 Power supply

Power is received via a USB C connector and negociated to 5V at 3A using 5.1k resistors on CC lines.

This voltage is boosted to 20V and all other voltage levels derive form this one.

15 V rail is loosely regulated using a capacitance multiplier. 5V rail is generated using a 7805 IC.

-20 V are generated by inverting the aforementioned 20 V rail. -15 V and -5V rails are obtained the same way as their positive counterparts.

1.1 Expected load

Worst case load is 10V into 50 ohms, yielding 200 mA of current. This current is however limited by the output buffer to 150 mA.

Say 50 mA for all operational amplifiers, and 50 mA for the MCU and the display. Total current capacity of the capacitance multiplier BJTs has to be 250 mA.

At 5V drop, this results ing 1.25W of waste heat. That's too much.

1.2 Revision 1

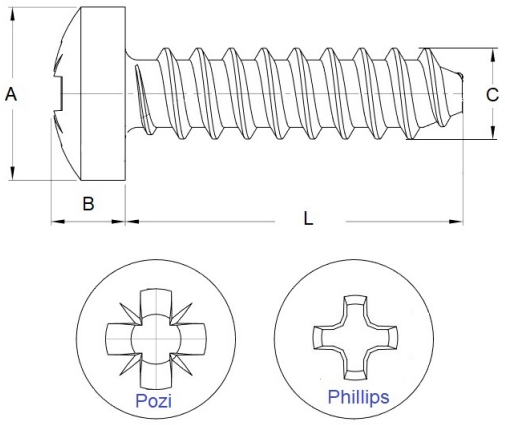
150 mA is fixed, but there is no need to power the LCD and the MCU with clean power. Only the AD DDS chip.

Further reducing the voltage drop to around 3V, yields a loss of 0.45 W. Bordering on manageable, considering this is an edge case only occurring on one voltage multiplier at a time.

5V still gets generated by 7x05 family, while the MCU and LCD get direct VBUS power.

2 Mounting holes

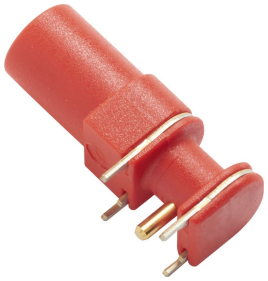
4 mounting posts are spaced in a 80 mm by 40 mm rectangle. Plastic post hole width is about 2.5 mm, but to allow for a self tapping screw, the PCB hole must be M3.



Apropriate screw is has a B of 2 mm, L of 6 mm, A of 5 mm and C of 3 mm.

3 Input connectors

3.1 PCB mount connector



Pomona connector cost around 8 EUR.

3.2 Panel mount

4 Charging connector

4.1 Panel mount USB C

Aliexpress panel mount USB C connector cost around 1.2 EUR per 10 qty.

This connector may not have the required resistors in order to negociate current demand
Kupujemprodajem konektor

5 Input divider

5.1 Resistance divider

With single sided input impedance of 4 Meg and a required attenuation of 1:400, total impedance from opamp input to gnd must be:

$$R_{in} = \frac{4\ \mathrm{M\Omega}}{399} = 10.025\ \mathrm{k\Omega} \tag{1}$$

Total resistance to ground is a parallel connection of the dividing resistor, 10 MΩ input offset trim pot and 10 MΩ opamp input resistance.

Dividing resistor value should then equal:

$$R_{div} = \frac{5\mathrm{M\Omega} \cdot 10.025\mathrm{k\Omega}}{5\mathrm{M\Omega} - 10.025\mathrm{k\Omega}} = 10.045\Omega \tag{2}$$

Placing a 0.1% resistor (10.010 kΩ max), trim pot should be around 50 Ω.

5.2 Capacitance divider

4 series 10 pF capacitors yield total 2.5 pF with a tolerance of 5%. In order to achieve 1:400 attenuation, total capacitance on the buffers input pin should be 997.5 pF. If we account for the 5% tolerance, total capacitance should be trimmable in the range for 947.62 pF to 1047.4 pF.

AD8039 features a typical input capacitance of 2 pF and thus should not significantly impact the total capacitance.

5.2.1 Trim potenciometers

Available trimmable capacitor has a capacitance range from 8 pF to 50 pF, not enough to account for the 5% capacitor tolerance.

These trim capacitors are expensive (5 EUR per 1 qty) and are only single turn, limiting trim accuracy.

5.2.2 Varicap trimming

In order to allow for auto-calibration, input capacitance needs to be control voltage dependant. To achieve this, a varicap diode may be used.

This component can be trimmed manually, using a trim potentiometer.

Since varicap add a voltage dependant capacitance value, total capacitance before the adding the varicap needs to be less then the total capacitance required.

As 5% capacitors are used, fixed capacitors used should equal:

$$C_{placed} = \frac{C_{req}}{1.05} - C_{varicap\ min} \tag{3}$$

Parallel connection of 2 470 pF yield capacitance in the range of 893 pF to 987 pF.

Since the capacitance change required is 10% of required capacitance, varicap capacitance change in the available control voltage range (0 V to 5V) must be around 100 pF.

Diode selection:

- Cheaper varicap diode is toshibas at 0.26 EUR per 10 qty.
- Better documented varicap diode is skyworks at 0.51 EUR per 10 qty.

PCB needs to support both of these diode footprints.

6 Offset results

6.1 10x gain enabled

-8.5 mV

6.2 1x gain enabled

9.2 mV

6.3 solving

$$V_{off\_10} = 10 \cdot (2V_{in\_off} + V_{curr\_off}) + V_{out\_off} \tag{4}$$

$$V_{off\_1} = 2V_{in\_off} + V_{curr\_off} + V_{out\_off} \tag{5}$$

$$V_{off\_10} - V_{off\_1} = 9 \cdot (2V_{in\_off} + V_{curr\_off}) = -17.7\text{mV} \tag{6}$$

Total input offset is -2 mV. Total output offset is 11.2 mV.

7 Sources of offset

7.1 Input buffer

7.1.1 Input bias current offset

AD8039 has an input bias current offset of 25nA, across the 20 kΩ input impedance, generates 0.5 mV of offset. Taking into account the second input buffer, maximum offset is 1 mV.

7.1.2 Input voltage offset

AD8039 has an max input voltage offset of 3mV. Worst case total offset is 6mV.

7.2 Output buffer

7.2.1 Input bias current offset

AD8009 has an max input current offset of 150µA. With an input impedance of 100 Ω, total offset is 15 mV. If both inputs have opposing offsets, the total offset is 30 mV

7.2.2 Input voltage offset

AD8009 has an max input voltage offset of 5mV.

8 Output diff amp

AD8039 load resistor is it's outputs series resistor.

9 Noise

9.1 Resistor noise

$$V_{rms} = \sqrt{4k_B T R \Delta f} \tag{7}$$

At the bandwidth of 100 MHz and temperature of 25 °C, noise is

$$V_{rms} = 3.63\text{mV}_{\text{RMS}} \tag{8}$$

9.2 Input buffer noise

AD8039 has an input noise level of $8\text{nV}/\sqrt{\text{Hz}}$ meaning that total input noise rms at 100 MHz bandwidth is 80 μV_{RMS}.

9.3 Output buffer noise

AD8009 has an input noise level of $1.9\text{nV}/\sqrt{\text{Hz}}$ meaning that total input noise rms at 100 MHz bandwidth is 19 μV_{RMS}.