MCP3651 based voltmeter module

12. novembar 2024.

Sadržaj

1 Resolution

MCP3651 ADC has a resolution of 24 bits, however, the 7 ppm max INL limits this multimeters count to 146000, just shy of 5.5 digit.

Keeping drift in 1 PPM range, 3 uV drift is acceptable over the temperature range.

1.1 Input current noise limit

Since for input ranges greater then Vcc the input voltage is feed through a 10 MOhm divider, input currents noise contribution is:

2 Input amplifier

2.1 NCS21802 only

2.1.1 Input current noise at high voltage input

NCS21802 has 450 fA$\sqrt{\text{Hz}}$, meaning at input divider resistance (around 12 kOhm), voltage noise generated is 5.4nV/$\sqrt{\text{Hz}}$. At 1 kHz BW, peak to peak noise contribution of input current is 1.02 uVpp. At 1 Hz, input noise is 32 nVpp.

2.1.2 Input current noise at low voltage input

2.1.3 Input voltage noise

NCS has 400 nVpp below 10 Hz, while the 1 kHz noise spec of 42 nV/Hz would suggest 800 nVpp at that BW. If we use the 1 kHz figure, we can estimate 1 kHz BW noise is 8 uVpp. At 1 Hz, input voltage noise is 252 nVpp or less.

2.1.4 Total noise at high voltage input

Total noise is dominated by voltage noise, which is say 9 uVpp at 1 kHz, 260 nVpp at 1 Hz. Scaling to input range, 3V signal still has to go into the high voltage divider and is reduced to 4.5 mV.

2.1.5 IDK

If we want 500 updates a second, setting the bandwidth to 1000 Hz admits 1716 nVrms, or 10.3 uVpp of noise. Reducing the BW to 4 Hz, 0.6 uVpp.

With the proposed 10 Meg, 12.5 k divider, worst case scenario is 3V input voltage, yealding 3.75 mV across the input divider. In this case, noise reduces the voltmeter resolution to 500 counts.

Averaging may improve this noise, but this is garantied to

2.2 TL072 and NCS

TL072 has 80 fA$\sqrt{\text{Hz}}$, meaning at input divider resistance (around 100 kOhm), voltage noise generated is 8nV/$\sqrt{\text{Hz}}$. Noise is larger at 0.1 Hz, with peak to peak noise being 300 times larger then noise density at 1 kHz. Max pp noise is then 2.4 uVpp. The input voltage noise pp is 9.2 uVpp.

$$V_noise = \sqrt{9.2^2 + 2.4^2} uVpp = 9.51 uVpp \tag{1}$$

In order to retain the 5.5 digit resolution, input range cant go lower than 2V.

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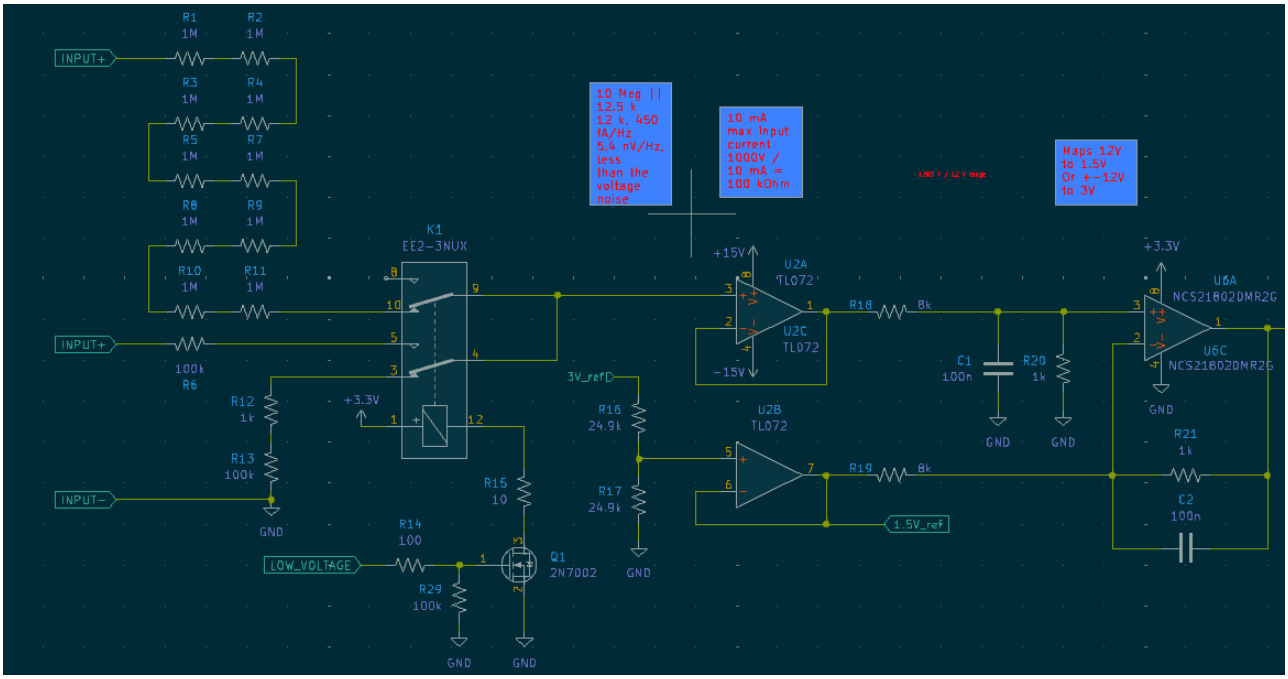
3 Calculating errors

3.1 Offset drift

The input stage is TL072 has typical of ±2 µV/°C and since the input stage features 2, one generating offset, total input drift is ±4 µV/°C.

This drift is lowered, as ±10V range gets mapped to 3.3 V range, meaning the offset drift contribution of TL072 is ±0.66µV/°C



The second stage consist of two opamps, component NCS21802, with input offset of ±5 nV/°C. First opamp contributes ±5 nV/°C, while second opamps contribution depends on the selected gain. In the worst case, gain of 100, the second opamps contribution is ±0.5 µV/°C.

The ADC has an input offset drift of ±4 nV/°C, meaning the total input offset drift is:

$$V_{os} = V_{tl072} + V_{NCS21802}(1 + 100) + V_{ADC} \tag{2}$$

$$V_{os} = \pm 1.169 \mu V/°C \tag{3}$$

Compared to full scale, drift is 0.35 PPM/°C, meaning for a 5.5 digit instrument, the drift is les than ±1 LSB for a temperature change of ±14 °C.

3.2 Gain drift

5.5 digit instruments have 5 PPM resolution.

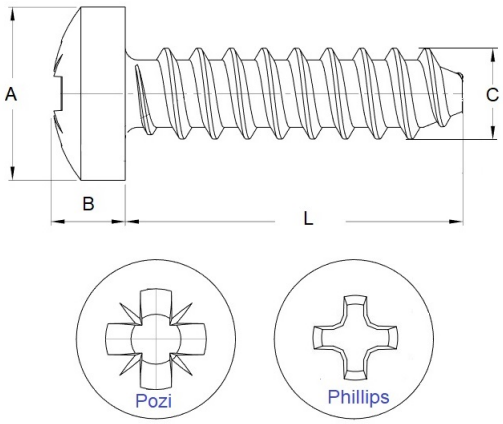
4 Power supply

4.1 Expected load

4.2 Revision 1

5 Mounting holes

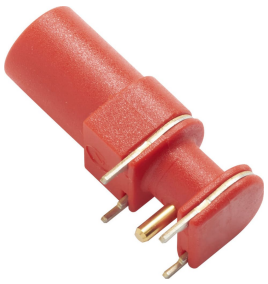
4 mounting posts are spaced in a 80 mm by 40 mm rectangle. Plastic post hole width is about 2.5 mm, but to allow for a self tapping screw, the PCB hole must be M3.



Apropriate screw is has a B of 2 mm, L of 6 mm, A of 5 mm and C of 3 mm.

6 Input connectors

6.1 PCB mount connector



Pomona connector cost around 8 EUR.

6.2 Panel mount

7 Charging connector

7.1 Panel mount USB C

Aliexpress panel mount USB C connector cost around 1.2 EUR per 10 qty.

This connector may not have the required resistors in order to negociate current demand
Kupujemprodajem konektor

8 Input divider

8.1 Resistance divider

With single sided input impedance of 4 Meg and a required attenuation of 1:400, total impedance from opamp input to gnd must be:

$$R_{in} = \frac{4\ \mathrm{M\Omega}}{399} = 10.025\ \mathrm{k\Omega} \tag{4}$$

Total resistance to ground is a parallel connection of the dividing resistor, 10 MΩ input offset trim pot and 10 MΩ opamp input resistance.

Dividing resistor value should then equal:

$$R_{div} = \frac{5\mathrm{M\Omega} \cdot 10.025\mathrm{k\Omega}}{5\mathrm{M\Omega} - 10.025\mathrm{k\Omega}} = 10.045\Omega \tag{5}$$

Placing a 0.1% resistor (10.010 kΩ max), trim pot should be around 50 Ω.

8.2 Capacitance divider

4 series 10 pF capacitors yield total 2.5 pF with a tolerance of 5%. In order to achieve 1:400 attenuation, total capacitance on the buffers input pin should be 997.5 pF. If we account for the 5% tolerance, total capacitance should be trimmable in the range for 947.62 pF to 1047.4 pF.

AD8039 features a typical input capacitance of 2 pF and thus should not significantly impact the total capacitance.

8.2.1 Trim potenciometers

Available trimmable capacitor has a capacitance range from 8 pF to 50 pF, not enough to account for the 5% capacitor tolerance.

These trim capacitors are expensive (5 EUR per 1 qty) and are only single turn, limiting trim accuracy.

8.2.2 Varicap trimming

In order to allow for auto-calibration, input capacitance needs to be control voltage dependant. To achieve this, a varicap diode may be used.

This component can be trimmed manually, using a trim potentiometer.

Since varicap add a voltage dependant capacitance value, total capacitance before the adding the varicap needs to be less then the total capacitance required.

As 5% capacitors are used, fixed capacitors used should equal:

$$C_{placed} = \frac{C_{req}}{1.05} - C_{varicap\ min} \tag{6}$$

Parallel connection of 2 470 pF yield capacitance in the range of 893 pF to 987 pF.

Since the capacitance change required is 10% of required capacitance, varicap capacitance change in the available control voltage range (0 V to 5V) must be around 100 pF.

Diode selection:

- Cheaper varicap diode is toshibas at 0.26 EUR per 10 qty.
- Better documented varicap diode is skyworks at 0.51 EUR per 10 qty.

PCB needs to support both of these diode footprints.

9 Offset results

9.1 10x gain enabled

-8.5 mV

9.2 1x gain enabled

9.2 mV

9.3 solving

$$V_{off\_10} = 10 \cdot (2V_{in\_off} + V_{curr\_off}) + V_{out\_off} \tag{7}$$

$$V_{off\_1} = 2V_{in\_off} + V_{curr\_off} + V_{out\_off} \tag{8}$$

$$V_{off\_10} - V_{off\_1} = 9 \cdot (2V_{in\_off} + V_{curr\_off}) = -17.7\text{mV} \tag{9}$$

Total input offset is -2 mV. Total output offset is 11.2 mV.

10 Sources of offset

10.1 Input buffer

10.1.1 Input bias current offset

AD8039 has an input bias current offset of 25nA, across the 20 kΩ input impedance, generates 0.5 mV of offset. Taking into account the second input buffer, maximum offset is 1 mV.

10.1.2 Input voltage offset

AD8039 has an max input voltage offset of 3mV. Worst case total offset is 6mV.

10.2 Output buffer

10.2.1 Input bias current offset

AD8009 has an max input current offset of 150µA. With an input impedance of 100 Ω, total offset is 15 mV. If both inputs have opposing offsets, the total offset is 30 mV

10.2.2 Input voltage offset

AD8009 has an max input voltage offset of 5mV.

11 Output diff amp

AD8039 load resistor is it's outputs series resistor.

12 Noise

12.1 Resistor noise

$$V_{rms} = \sqrt{4k_B T R \Delta f} \tag{10}$$

At the bandwidth of 100 MHz and temperature of 25 °C, noise is

$$V_{rms} = 3.63\text{mV}_{\text{RMS}} \tag{11}$$

12.2 Input buffer noise

AD8039 has an input noise level of $8\text{nV}/\sqrt{\text{Hz}}$ meaning that total input noise rms at 100 MHz bandwidth is 80 μV_{RMS}.

12.3 Output buffer noise

AD8009 has an input noise level of $1.9\text{nV}/\sqrt{\text{Hz}}$ meaning that total input noise rms at 100 MHz bandwidth is 19 μV_{RMS}.