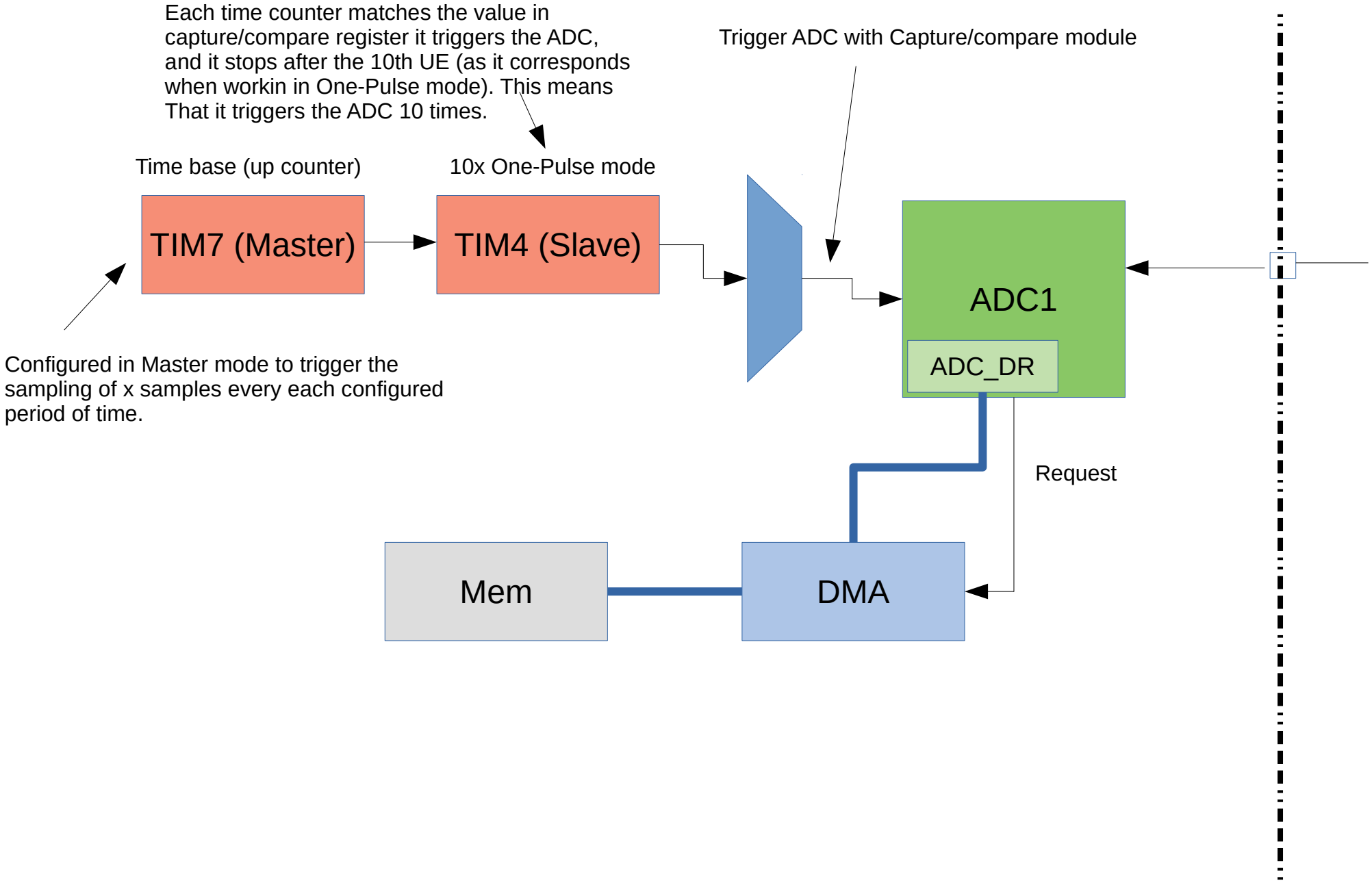
Each time counter matches the value in capture/compare register it triggers the ADC, and it stops after the 10th UE (as it corresponds when workin in One-Pulse mode). This means That it triggers the ADC 10 times.
Trigger ADC with Capture/compare module
Time base (up counter)
10x One-Pulse mode
TIM7 (Master)
TIM4 (Slave)
ADC1
ADC_DR
Configured in Master mode to trigger the sampling of x samples every each configured period of time.
Request
Mem
DMA