Application Note

EtherCAT® Slave Controller

PHY Selection Guide

Requirements to Ethernet PHYs used for EtherCAT
Ethernet PHY Examples

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BECKHOFF

DOCUMENT HISTORY

Version	Comment
1.1pre	First preliminary release
1.2	• Ethernet PHY requirements revised (e.g., link loss reaction time) • Added Micrel KSZ8001L • Added National Semiconductor DP83848, DP83849, and DP83640 • Editorial changes
1.3	• Added restriction to enhanced link configuration: RX_ER has to be asserted outside of frames (IEEE802 optional feature) • Removed National Semiconductor DP83848 and DP83849 temporarily for further examination
1.4	• Updated/clarified PHY requirements, PHY link loss reaction time is mandatory • Added National Semiconductor DP83848, DP83849 with comments • Added PHYs which require Enhanced Link detection to be activated • Editorial changes
1.5	• PHY startup should not rely on MDC clocking • Added Micrel KSZ8041NL/TL Rev. A4 to list of example Ethernet PHYs for EtherCAT with Enhanced Link Detection requirement • ESD tolerance and baseline wander compensation recommendations added • Editorial changes

1 Overview

An EtherCAT Slave Controller (ESC) takes care of the EtherCAT communication as an interface between the EtherCAT fieldbus (Ethernet) and the slave application.

EtherCAT uses standard Fast Ethernet. Transmission speed for EtherCAT is fixed to 100 Mbit/s with Full Duplex communication. EtherCAT Slave Controllers process Ethernet frames on the fly.

This application note provides an overview of the requirements to Ethernet PHYs used for EtherCAT devices. An example list of Ethernet PHYs currently expected to be suitable for EtherCAT is also provided.

This application note applies to the following Beckhoff EtherCAT Slave Controllers:

- ET1200
- ET1100
- EtherCAT IP Core for Altera/Xilinx FPGAs
- ESC10/20

Refer to the ESC data sheets for further information. The ESC data sheets are available from the Beckhoff homepage (http://www.beckhoff.com).

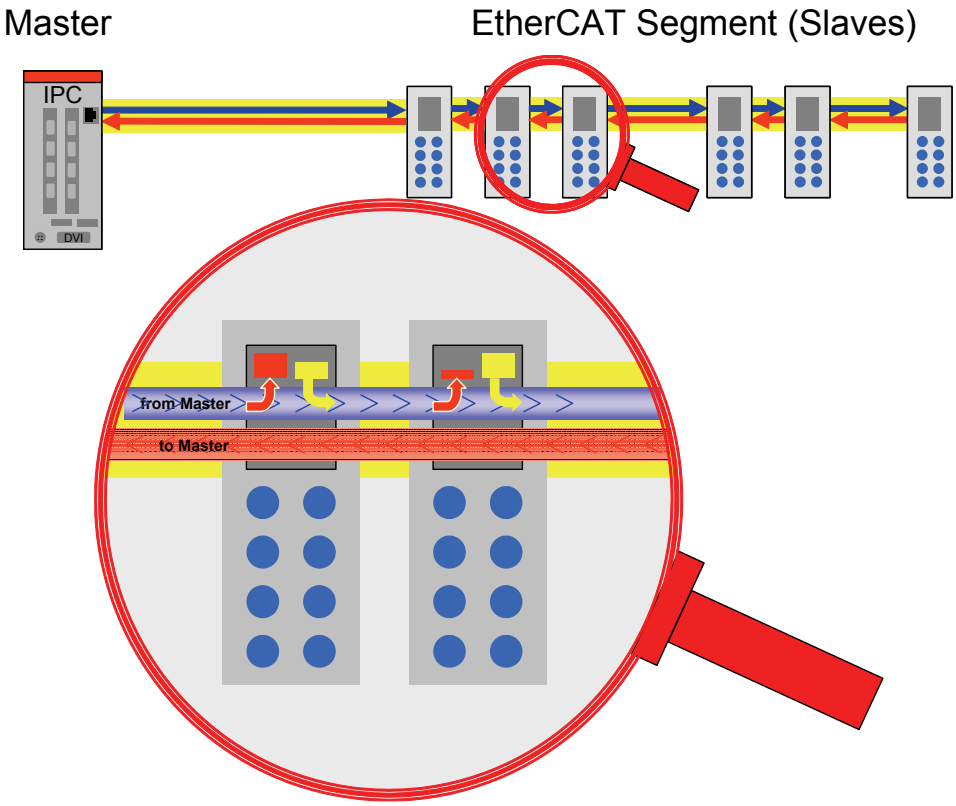

Figure 1: EtherCAT Segment

2 Ethernet PHY Requirements

ESCs which support Ethernet Physical Layer use MII interfaces, some do also support the RMII interface. Since RMII PHYs include TX FIFOs, they increase the forwarding delay of an EtherCAT slave device as well as the jitter. RMII is not recommended due to these reasons.

EtherCAT and Beckhoff ESCs have some general requirements to Ethernet PHYs, which are typically fulfilled by state-of-the-art Ethernet PHYs.

The MII interfaces of Beckhoff ESCs are optimized for low processing/forwarding delays by **omitting a transmit FIFO**. To allow this, the Beckhoff ESCs have additional requirements to Ethernet PHYs, which are easily accomplished by several PHY vendors.

Refer to Section III of the ESC documentation for ESC specific information about supported features.

Requirements to Ethernet PHYs used for EtherCAT:

- The PHYs have to comply with **IEEE 802.3 100BaseTX or 100BaseFX**.
- The PHYs have to support 100 Mbit/s Full Duplex links.
- The PHYs have to provide an **MII** (or RMII[1]) interface.
- The PHYs have to use autonegotiation.
- The PHYs have to support the MII management interface.
- The PHYs have to support **MDI/MDI-X auto-crossover**.
- PHY **link loss reaction time** (link loss to link signal/LED output change) has to be faster than 15 µs to enable redundancy operation[2].
- The PHYs must not modify the preamble length.

Additional requirements to Ethernet PHYs used with Beckhoff ESCs:

- The PHYs have to provide a **signal indicating a 100 Mbit/s (Full Duplex) link**[3], typically a configurable LED output. The signal polarity is active low or configurable for some ESCs.
- The **PHY addresses** should be equivalent to the **logical port number (0-3)**. Some ESCs also support a fixed offset (e.g. offset 16, PHY addresses are logical port number plus 16: 16-19), or even an arbitrary offset. If none of these possibilities can be used, the PHY address should be configured to logical port number plus 1 (1-4), although some features (e.g., Enhanced Link Detection) can not be used in this case, because apart from the optional configurable PHY address offset, the PHY addresses are hard-coded inside the ESCs.
- PHY configuration must not rely on configuration via the MII management interface, i.e., required features have to be enabled after power-on, e.g., by default or by **strapping options**. PHY startup should not rely on MII management interaction, i.e., MDC clocking, since many ESCs do not communicate with the PHY via management interface unless the EtherCAT master requests this (only the EtherCAT IP Core with MI Link detection and configuration will communicate without master interaction).

Additional requirements to Ethernet PHYs used with Beckhoff ESCs using the MII Interface:

- All PHYs connected to one ESC and the ESC itself must share the **same clock source**. This can be achieved by sourcing the PHYs from an ESC clock output or by sourcing the PHYs and the ESC from the same quartz oscillator. The ESC10/20 uses TX_CLK as a clock source, both PHYs have to share the same quartz oscillator.
- The **TX_CLK** signals of the PHYs must have a **fixed phase relation to the clock input** of the PHYs with a tolerance of ±5 ns, because a TX FIFO is omitted. During operation the phase

[1] RMII is only supported by the EtherCAT IP Core

[2] This can either be achieved by a PHY with such a link loss reaction time or by activating Enhanced link detection if the PHY asserts RX_ER both inside and outside of frames for each invalid symbol. Enhanced link detection requires proper PHY address configuration. Devices with one or more EBUS ports which do not support port-wise configuration can not be configured to use Enhanced link detection without sacrificing compatibility to older ESCs.

[3] If a combined signal (100 MBit/s link with Full Duplex) is not available, a signal indicating 100 Mbit/s speed might be used. Take care that the speed signal is inactive (10 Mbit/s) in case of no link. If only a Link signal is available, this might be used. Never use (combined) activity signals.

relation can not change since the PHYs and the ESC have to share the same clock source. The phase offset is compensated inside the ESC either manually by configuration or automatic:
Manual TX Shift compensation: ET1100, ET1200, and IP Core provide a TX Shift configuration option (configurable TX_EN/TXD signal delay by 0/10/20/30 ns) which is used for all MII ports. Thus, all PHYs connected to one ESC must have the same fixed phase relation between TX_CLK and their clock input. This is typically true if the same PHY model is used for all ports. The phase relation has to be the same each time the PHYs are powered on. As the ESC10/20 use TX_CLK as device clock source, configuration is not necessary, but the requirements for manual TX Shift compensation have to be fulfilled anyway.
Automatic TX Shift compensation: The IP Core supports automatic TX Shift compensation individually for each port. With automatic TX Shift compensation, the PHYs are not required to have the same fixed phase relation each time they are powered on.

Recommendations to Ethernet PHYs used for EtherCAT:

- Receive and transmit delays should be deterministic.
- Maximum cable length should be ≥ 120 m to maintain a safety margin if the standard maximum cable length of 100 m is used.
- ESD tolerance should be as high as possible (4kV or better)
- Baseline wander should be compensated (even at maximum cable length)
- MDC should not incorporate pull-up/pull-down resistors, as this signal is used as a configuration input signal by some ESCs.
- Restriction of Autonegotiation advertisement to 100 Mbit/s / Full Duplex is desirable (configured by hardware strapping options).
- Power consumption should be as low as possible.
- I/O voltage: 3.3V should be supported for current ASIC and FPGA ESCs, additional 2.5V I/O support is recommended for recent FPGA ESCs.
- Single power supply according to I/O voltage (3.3V or 2.5V).
- The PHY should use a 25 MHz clock source (quartz oscillator or ESC output).
- Industrial temperature range should be supported.

NOTE: The following requirements defined by IEEE802.3 have to be observed: a) The preamble length should be maintained. Accumulating preamble reduction below 2 bytes including Start-of-Frame-Delimiter/SFD (0x55 5D) must not occur for single or cascaded ESCs. ESCs can not regenerate preambles to 8 bytes including SFD because of the on-the-fly processing, received and transmitted preamble length is identical. b) Receive and transmit delays should comply with the standard (RX delay should be below ~320 ns, TX delay below ~140 ns).

3 PHY Connection

Figure 2 shows the principle connection between ESC[4] and PHY. The clock source of Ethernet PHYs and ESC has to be the same quartz or quartz oscillator. TX_CLK is usually not connected unless automatic TX Shift compensation is used, because the ESCs do not incorporate a TX FIFO. The TX signals can be delayed inside the ESC for TX_CLK phase shift compensation. LINK_STATUS is an LED output indicating a 100 Mbit/s (Full Duplex) link.

Refer to ESC data sheet Section III for details about Ethernet PHY connection of a specific ESC.

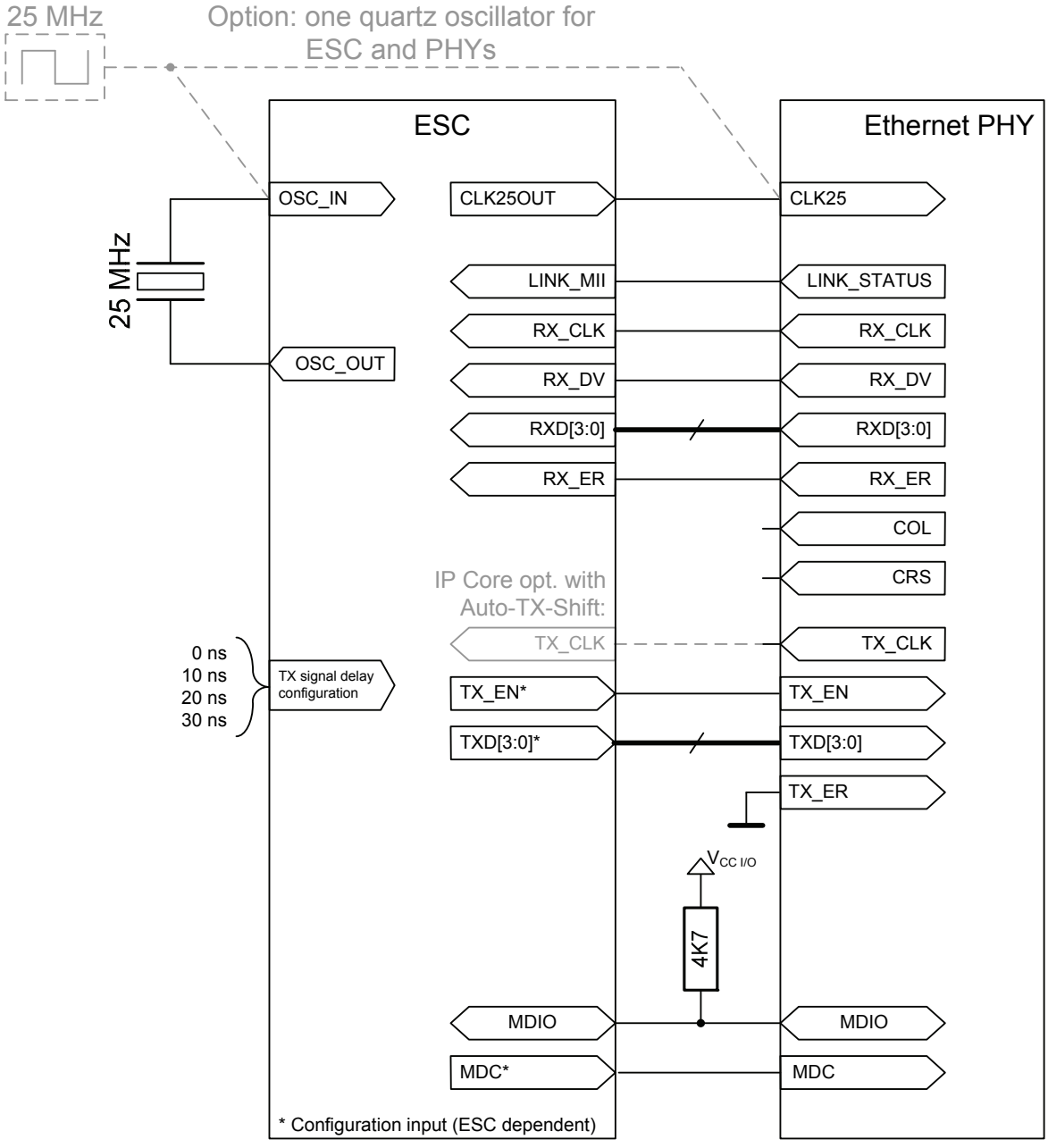

Figure 2: PHY Connection

[4] ESC10/20 uses TX_CLK of a PHY as the clock source of the ESC. FPGAs with IP Core only support the quartz oscillator alternative.

4 Example Ethernet PHYs

In this chapter, some example Ethernet PHYs which are assumed to fulfill the EtherCAT requirements are presented, as well as an overview of Ethernet PHYs which are assumed to not fulfill these requirements. These lists represent a current collection of information from data sheets, vendors, and basic hardware tests for some devices, and they represent the best of current knowledge. These lists do not imply any kind of certification for EtherCAT, since none of these PHYs has been tested thoroughly and step-by-step to fulfill each EtherCAT and IEEE802.3 requirement. These lists are only meant as a guide for developers seeking for information about Ethernet PHYs for EtherCAT.

The Ethernet PHYs were either judged by a **brief** overview of their data sheets or by additional **basic** hardware tests. Ethernet PHYs which have been tested in hardware are indicated.

The example Ethernet PHYs for EtherCAT shown in the following tables are sorted alphabetically by vendor name, not by preference. The selection of Ethernet PHYs was restricted to 1-4 port 10/100 Mbit/s Ethernet PHYs. These tables are incomplete in terms of Ethernet PHY vendors and Ethernet PHY devices – they just give some examples, and it is likely that other devices and devices from different vendors meet the requirements as well.

It can not be guaranteed that the mentioned Ethernet PHYs, future revisions of them, or product changes are or will be fully EtherCAT compatible or not, nor that they are compatible with all types of ESCs – because of ESC specific options (e.g., configurable link polarity, supported PHY address offsets, Enhanced Link detection, automatic TX Shift compensation). As far as known, restrictions and features of the PHYs impacting their EtherCAT usage are added to the tables.

4.1 Example Ethernet PHYs

Table 1: Example Ethernet PHYs assumed to fulfill EtherCAT requirements

Vendor / Device	Ports	HW tested[5]	TX_CLK fixed phase[6]	PHY addr.[7]	PHY addr. offset[8]	Link loss reaction time	Comments
Broadcom							
BCM5221	1	no	Data sheet[9]	0-31	0	1.3 µs	Quartz oscillator required. Internal pull-down at MDC.
BCM5222	2	no	Data sheet	0-31	0	1.3 µs	Quartz oscillator required. Internal pull-down at MDC.
BCM5241	1	yes	Data sheet	0-7, 8, 16, 24	0	1.3 µs	Quartz oscillator required. Internal pull-up at MDC. XTALI ≤ 1.8V
Micrel							
KSZ8001L	1	no	Vendor	1-31	16	ms	PHY addr. 0 = Broadcast
KSZ8721B KSZ8721BT	1	yes (BT)	Vendor	0-31	0	6 µs	Internal pull-up at MDC
KSZ8721BL KSZ8721SL	1	yes (BL)	Vendor	0-31	0	6 µs	Internal pull-up at MDC
KSZ8721CL	1	no	Vendor	0-31	0	6 µs	Internal pull-up at MDC

[5] The following requirements were not part of the basic hardware test: MDI/MDI-X auto-crossover, MII management interface, TX clock phase relation, and preamble length maintenance. The first three requirements are assumed to be fulfilled either according to the data sheet or vendor notice. The last requirement is only approved by Micrel for KS8721 and KS8001L. The other devices have not been tested.
[6] Information about fixed phase shift between TX_CLK and PHY clock source from data sheet or from vendor
[7] PHY address range supported by PHY. Special PHY addresses are excluded (Broadcast/Isolate).
[8] Suggested PHY address offset. ET1100 and ET1200 only support a PHY address offset of 0 or 16, otherwise Enhanced link detection has to be deactivated. A PHY address offset of 0 means PHY addresses 0-3 are used, an offset of 16 means PHY addresses 16-19 are used, etc..
[9] Only for XTALI, not approved for REF_CLK. According to Broadcom, a quartz oscillator can be connected to XTALI as well.

4.2 Example Ethernet PHYs: Enhanced Link Detection required

The following Ethernet PHYs require **Enhanced Link Detection** to be activated in order to achieve sufficient link loss reaction times. Please notice that Enhanced Link detection can not be activated if the ESC has one or more EBUS ports, because EBUS Enhanced Link detection is incompatible with some older ESCs.

Table 2: Example Ethernet PHYs assumed to fulfill EtherCAT requirements if Enhanced Link detection is activated

Vendor / Device	Ports	HW tested[5]	TX_CLK fixed phase[6]	PHY addr.[7]	PHY addr. offset[8]	Link loss reaction time	Comments
Restriction: Enhanced Link detection has to be activated for the following PHYs:							
Micrel							
KSZ8041TL Rev. A4 KSZ8041NL Rev. A4	1	no	Vendor	1-7	1	up to 1 ms	PHY addr. 0 = Broadcast Enable 8 byte preamble with CONFIG[2:0]=100
National Semiconductor							
DP83848	1	yes	Vendor	1-31	16	250 µs	PHY addr. 0 = Isolate, use LED_LINK for link detection
DP83849	2	no	Vendor	0-31	0	250 µs	do not use SCMII mode, use LED_LINK for link detection
DP83640	1	no	Vendor	1-31	16	250 µs (conf. to ~1.3 µs)	PHY addr. 0 = Isolate, do not use SCMII mode, use LED_LINK for link detection

4.3 Examples of Ethernet PHYs assumed to be incompatible with EtherCAT requirements

The following Ethernet PHYs are currently assumed or known to be **incompatible** with EtherCAT – because they do not support MDI/MDIX-auto-crossover which became state-of-the-art for many recent PHYs:

- AMD: Am79C874, Am79C875 (datasheet: no MDI/MDIX-auto-crossover)
- Broadcom: BCM5208R (datasheet: no MDI/MDIX-auto-crossover)
- Cortina Systems (formerly Intel): LXT970A, LXT971A, LXT972A, LXT972M, LXT974, LXT975 (datasheet: no MDI/MDIX-auto-crossover)
- Davicom Semiconductor: DM9761 (datasheet: no MDI/MDIX-auto-crossover)
- Micrel: KSZ8041 Rev. A3 (hardware test: no preamble maintenance) and maybe previous revisions
- SMSC: LAN83C185 (datasheet: no MDI/MDIX-auto-crossover)
- STMicroelectronics: STE100P (datasheet: no MDI/MDIX-auto-crossover)
- Teridian (formerly TDK): 78Q2120C (datasheet: no MDI/MDIX-auto-crossover)
- VIA Technology: VT6103F, VT6303L (datasheet: no MDI/MDIX-auto-crossover)

5 Appendix

5.1 Support and Service

Beckhoff and their partners around the world offer comprehensive support and service, making available fast and competent assistance with all questions related to Beckhoff products and system solutions.

5.1.1 Beckhoff's branch offices and representatives

Please contact your Beckhoff branch office or representative for local support and service on Beckhoff products!

The addresses of Beckhoff's branch offices and representatives round the world can be found on her internet pages: http://www.beckhoff.com

You will also find further documentation for Beckhoff components there.

5.2 Beckhoff Headquarters

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