ECE 212 DIGITAL CIRCUITS
Combined Time and Temperature Display

Lab 04 10/13/2023

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https://github.com/otienomaurice1/ece212_alex_maurice.git

Introduction:

In this lab we combined the designs of the digital clock and the temperature display we designed earlier. The lab involved displaying either time or temperature or both based on a given mode. The mode is determined by a switch operated by the user. We then synthesized our design in Vivado suite, implemented the design, routed the implemented design and generated write bitstream. We interfaced the design with the NEXY'S A7 100T FGA board available in the lab by programming the device with the generated bitstream.

Design:

Design specification:

1.The design shall display the time and temperature using four modes controlled by switches 15 and 14 of the NEXY'S A7 100T FGA board.

The current mode of display is determined by the two switches as follows:

SW15	SW14	DISPLAY OPTION
0	0	Display Time Only
0	1	Alternate between displaying time and Fahrenheit temperature every 2 seconds
1	0	Alternate between displaying time and Celsius temperature every 2 seconds
1	1	Alternate between displaying time, Fahrenheit temperature, and Celsius temperature every 2 seconds

2.All designs be synchronized and connected to a common clock signal i.e., the 100MHz clock signal from the FPGA board.

3. The following buttons are to be used for user input:

Button	Corresponding input
BTNL	adv_hr
BTNR	adv_min
BTNU	rst

4. The entire design is to be interfaced with the NEXY'SA7 100T FPGA.

Design implementation:

The overall design of the combined time and Temperature display utilized a module called time_temp_comb

This module has four one-bit inputs clk, rst, adv_min and adv_hr for the clock, reset, advance minutes and advance hour inputs respectively. The last two inputs are used to set the time as discussed in lab2.

There is a two-bit input named SW which delivers the input mode from the switches.

The module has four outputs an_n, segs_n, and dp_n to display the output on the seven-segment display.

The module is a connection of submodules dig_clock to generate time, period_enb for delay, sevenseg_ctl to display output and tdisplay to generate the desired temperature readings. All these modules have been discussed in the previous labs and this module's function is to bind them together to function as required.

In order to switch from one display mode to another, we use a multiplexer whose selector signal is SW. This multiplexer chooses one mode out of the four available modes. Inside each mode we need to know what is being displayed. Since we are shifting between displaying time, temperature in degrees Celsius and temperature in Fahrenheit every two seconds, we need some form of storage to remember what we displayed last. We utilize a finite state machine with three states each state representing either time, temperature in degrees Fahrenheit or temperature in degrees Celsius. pe_enb is initialized with the parameter 2000 to delay the change from one state to another by 2 seconds.

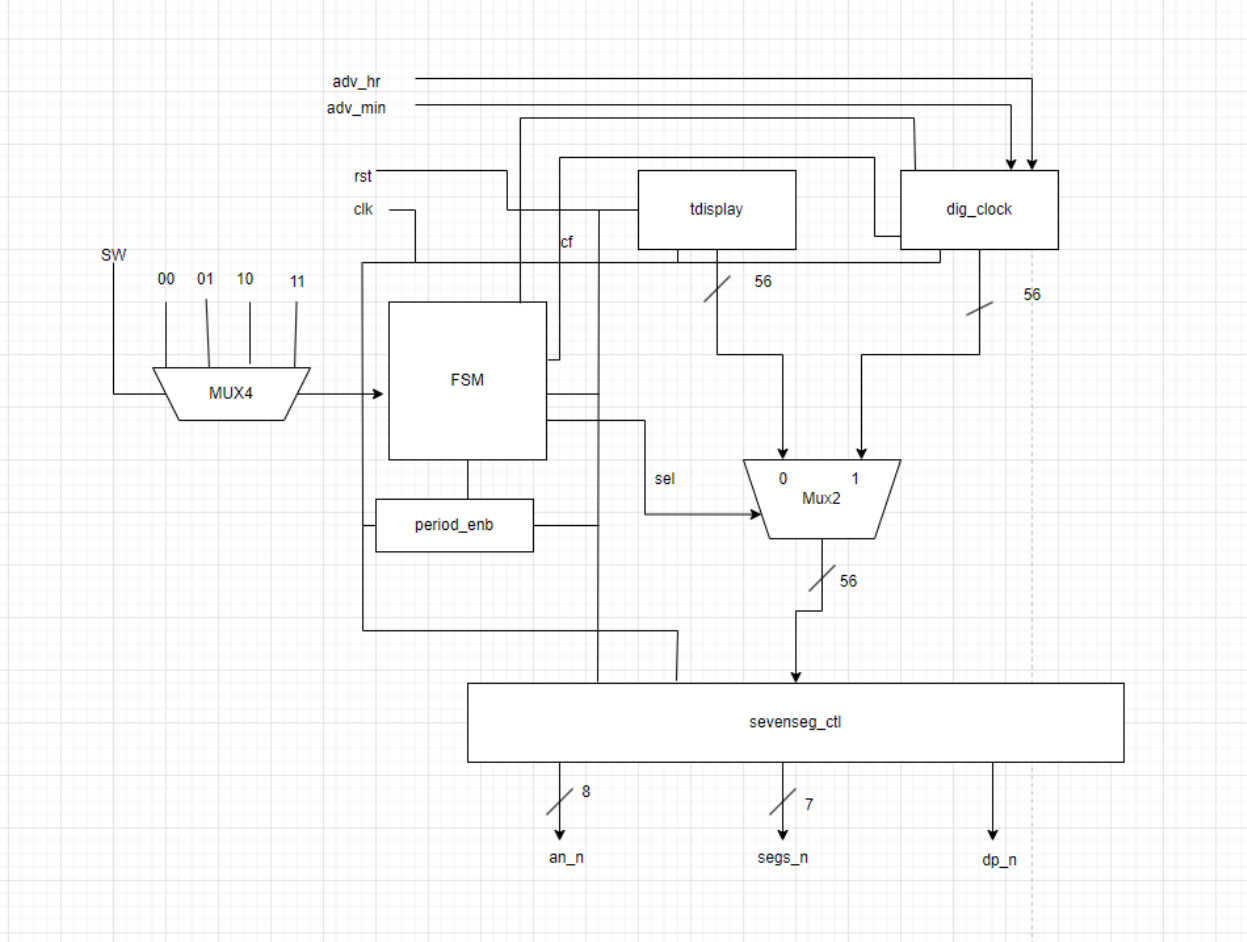


Figure 1 time_temp_comb top level diagram

The three states are TI for time, TF for temperature in Fahrenheit and TC for temperature in Celsius. The outputs sel and cf are to select between time and temperature, and select between Fahrenheit and Celsius respectively.

The default state is TI i.e., we should always display the time when the device is reset or first programmed.

The default outputs are: sel = 1; (display time)

cf = 0; (display temperature in Celsius)

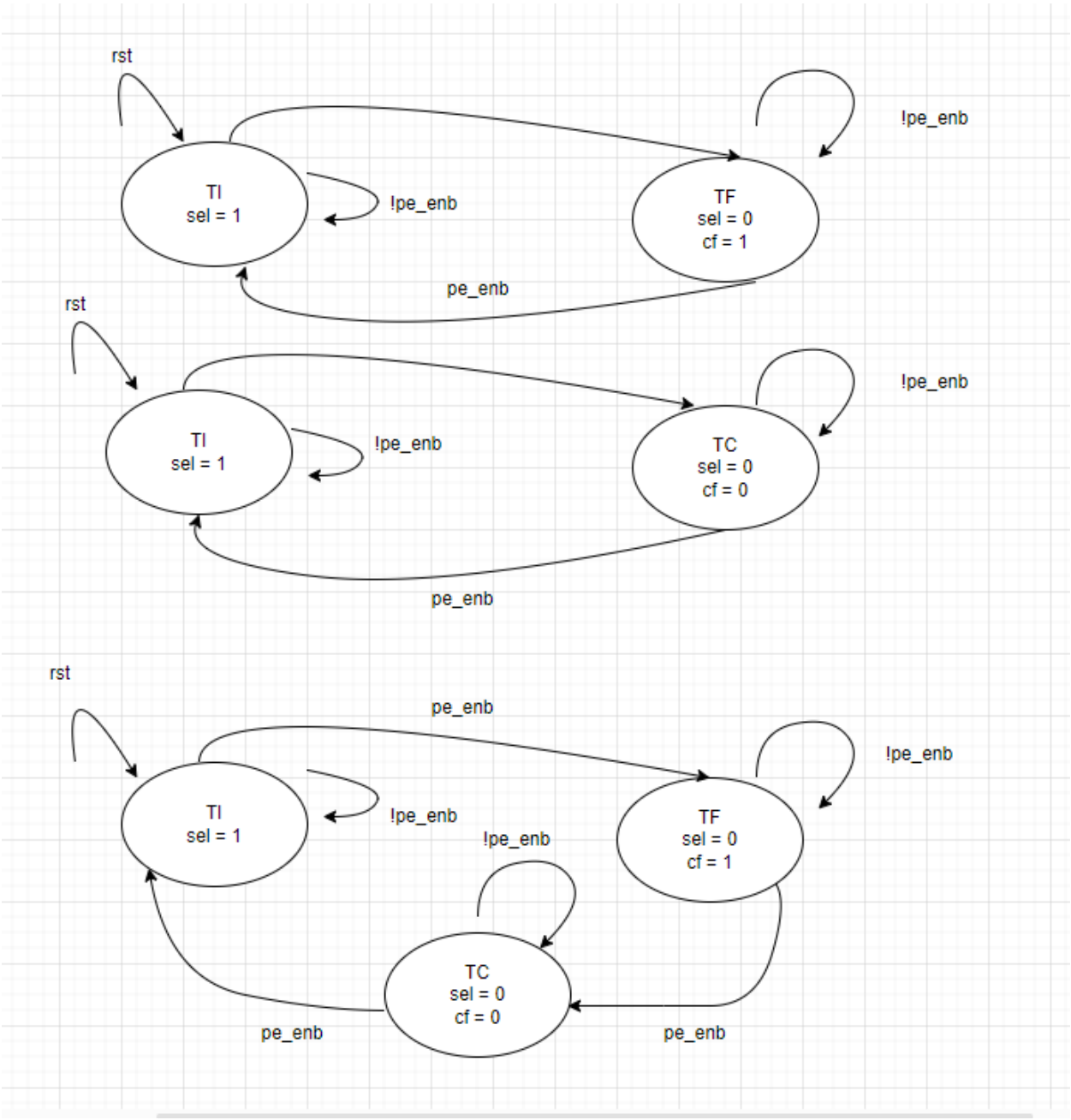
For the first case where only temperature is displayed, we do not need to shift from any state to another. The mode is 00 and the finite state machine outputs is sel = 1;

When we change the mode to 01; We should switch between time and temperature in Fahrenheit every two seconds. In the first case TI, when displaying time sel = 1; In the second case TF, sel = 0 and cf = 1. We only use two states of the finite state machine

When the mode is changed to 10, we now switch between displaying time and temperature in degrees Celsius. The outputs are sel = 0 in first case; The next case outputs sel = 1 and cf = 0. We only use two states again.

When the mode changes to 11, we use all the three states since we are now checking all the three states. In the first case TI, sel = 1. In the next case TF sel = 0 and cf = 1. In the next case TC sel = 0 and cf = 0;

The finite state machine diagrams are shown below. Notice that the first mode i.e., 00 is not represented because its output is always sel = 0. The other modes finite state machine diagrams are shown in the order in which they are discussed above.


rst
TI
sel = 1
!pe_enb
TF
sel = 0
cf = 1
!pe_enb
pe_enb
rst
TI
sel = 1
!pe_enb
TC
sel = 0
cf = 0
!pe_enb
pe_enb
rst
pe_enb
TI
sel = 1
!pe_enb
TF
sel = 0
cf = 1
!pe_enb
!pe_enb
TC
sel = 0
cf = 0
pe_enb
pe_enb

Results:

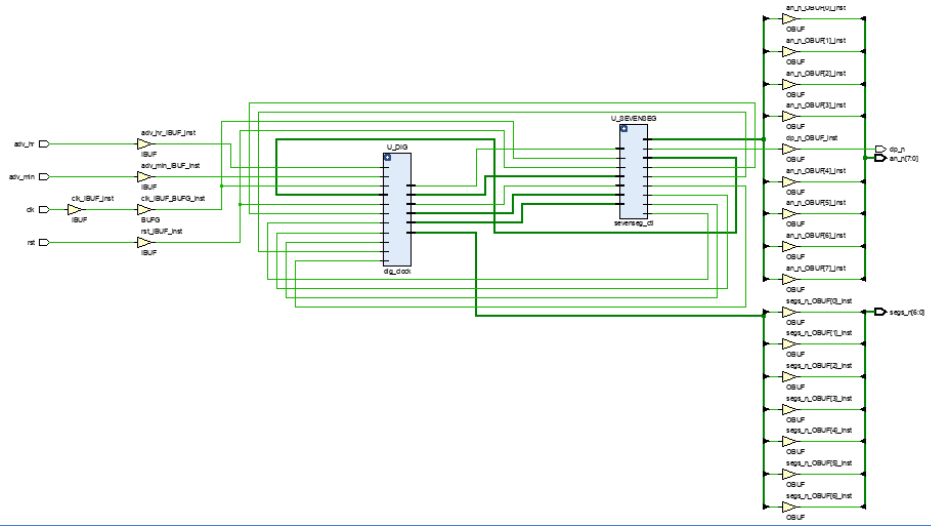


Figure 2time_temp_comb synthesized design schematic

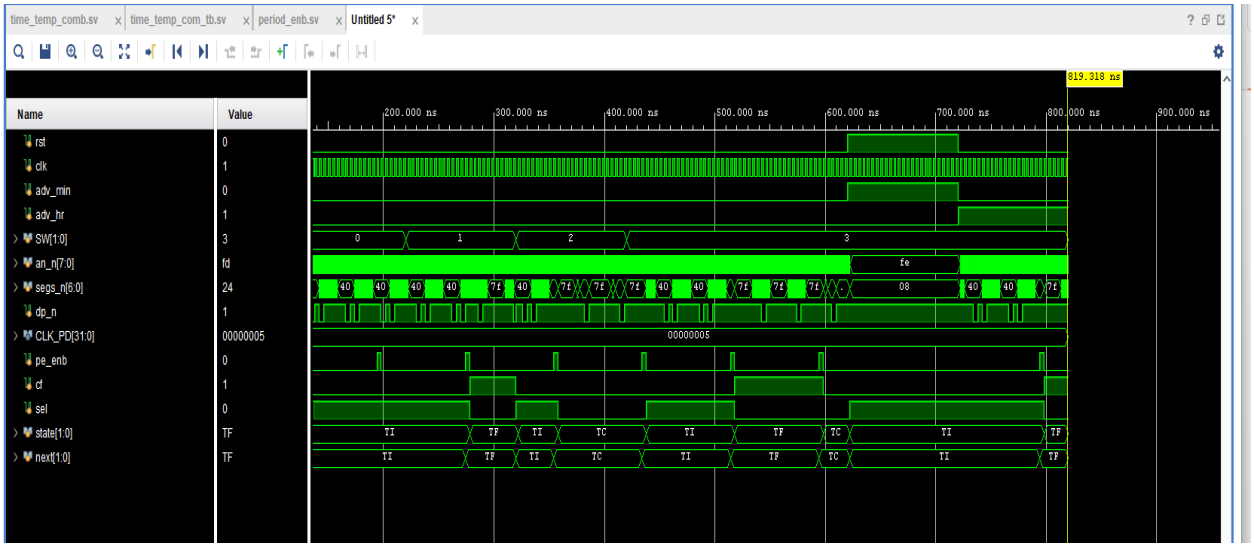


Figure 3simulation scope for time_temp_comb_tb.sv

```
141 ---------------------------------------------------------------------------------
142 Start RTL Component Statistics
143 ---------------------------------------------------------------------------------
144 Detailed RTL Component Info :
145 +---Adders :
146        2 Input    4 Bit       Adders := 14
147        2 Input    3 Bit       Adders := 1
148 +---Registers :
149                     4 Bit    Registers := 8
150                     3 Bit    Registers := 1
151                     1 Bit    Registers := 1
152 +---Muxes :
153        8 Input    8 Bit        Muxes := 1
154        2 Input    7 Bit        Muxes := 1
155       17 Input    7 Bit        Muxes := 1
156        2 Input    4 Bit        Muxes := 7
157        4 Input    4 Bit        Muxes := 1
158        2 Input    1 Bit        Muxes := 2
159        3 Input    1 Bit        Muxes := 1
160 ---------------------------------------------------------------------------------
161 Finished RTL Component Statistics
162 ---------------------------------------------------------------------------------
163 ---------------------------------------------------------------------------------
```

Figure 4synthesis report

Conclusion:

The lab involved connecting previously described modules so we did not experience many challenges except for wire connection errors

Time spent in lab

3hrs 30 min