ECE 212 – Digital Circuits II

Lab2 – Digital Clock

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https://github.com/otienomaurice1/ece212_alex_maurice.git

1. **Introduction:**

Digital clocks, unlike analog clocks enable us to read the time directly with the exact figures. Analog clocks require an awareness of the relative positions between clock arms and only give an approximation of the time.

In this lab we designed a digital clock by writing modules in system Verilog to describe the behavior of the clock. When first turned on, the digital clock was to display the time as from 12.00 am. The user should be able to set the time in accordance with his/her current time. The user could at any time also reset the clock back to 12.00 am. After twelve hrs. the clock would leave am and shift to p.m. After describing this behavior in system Verilog, we used AMD'S Xilinx Vivado CAD software to synthesize the design and implement it. We also wrote testbenches to test the functionality of some key modules. We interfaced the design with the seven-segment display on the NexysA7 -100T printed circuit board.

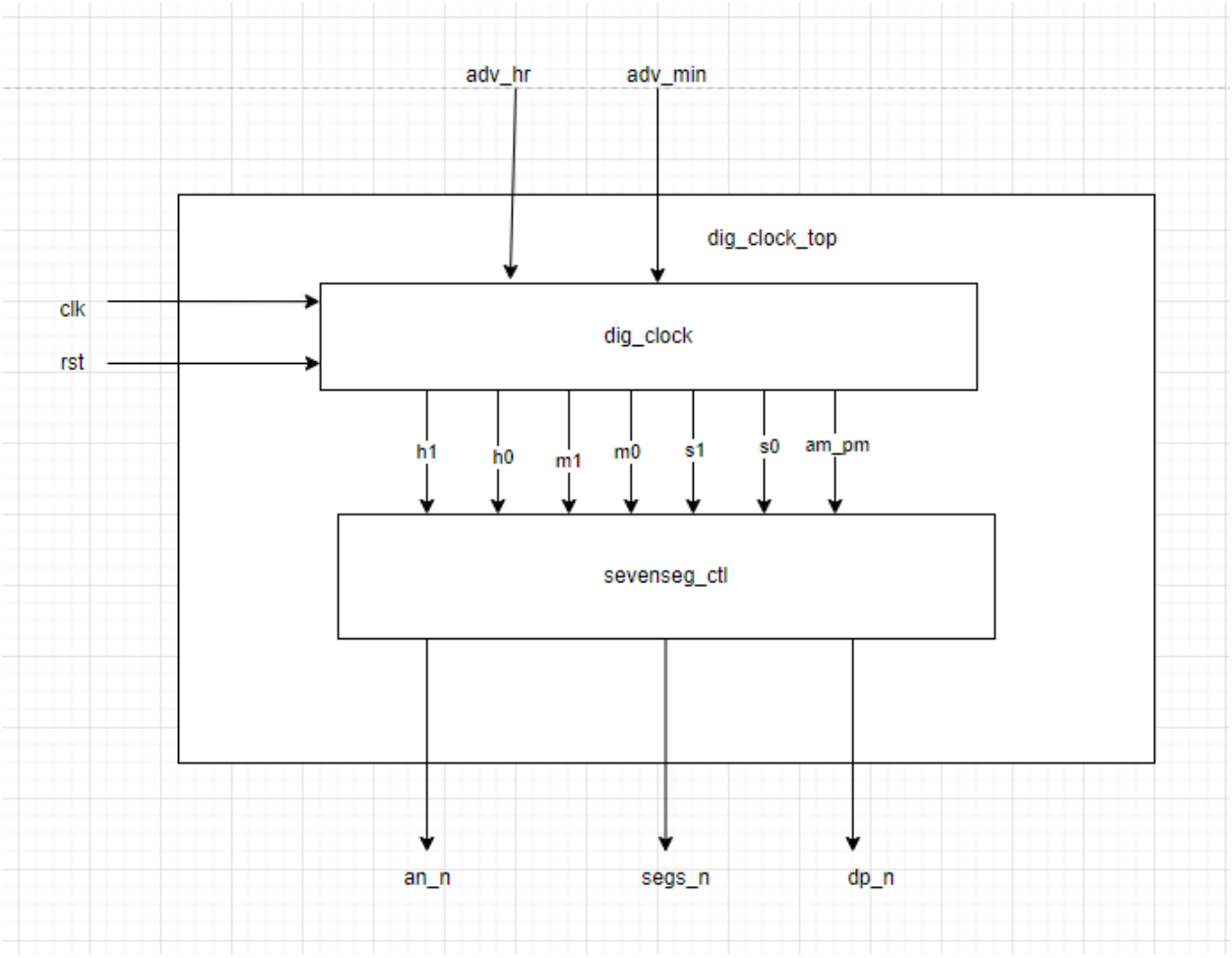
2. **Design:**

Design specifications

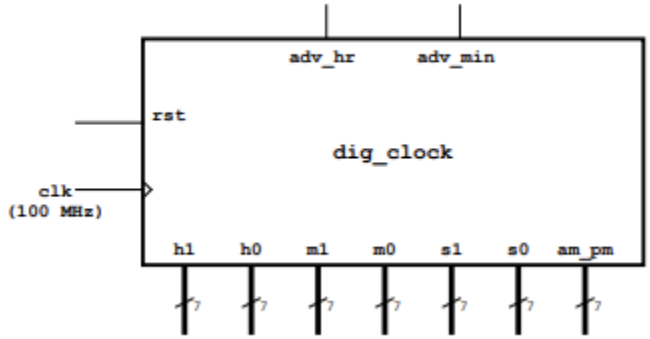
The specifications of the design of the clock were as follows:

- The last(right-most) digit of the seven-segment display was to display the mode in a.m. or p.m.
- There second-last digit would be blanked
- The next two digits would display the time in seconds
- The next two digits would display the time in minutes and the last two (most significant) digits would display the in hours. If the most significant digit of hrs has the value of zero, then it should be blanked
- There would be a decimal point between the hours and minutes, and between minutes and seconds.
- There would be two inputs to enable the user set the time. One input named adv_min would advance the minutes by one while keeping the current value of seconds while the second input adv_hr would advance the hour by one while keeping the values of minutes and seconds
- The design would be interfaced with the NEXY'SA7 100T such that the rst signal comes from the BTND button ,adv_min would come from BTNR, adv_hr would come from BTNL and the clock signal would come from the 100 MH clock on the board.

Design implementation



The overall design of the clock utilized a top module named dig_clock_top as shown above. This module contains two submodules named dig_clock and sevenseg_ctl which represent the functional design of the clock behavior and the seven-segment controller respectively.



-dig_clock takes in 4 inputs i.e., the clock and reset signals and two user control signals adv_min and adv_hr. It also has an instance of the time counter module time_ctr which is responsible for bringing in the time. The outputs of dig_clock is seven-bit values that represent the current time in am or pm. In

this module, we take the four-bit values of the time from the time counter and concatenate them with three-bit values that will determine whether the seven-segment decoder will display that value or not, display the decimal point. The outputs (h1,h0),(m1,m0),(s1,s0) and am_pm stand for hours, minutes, seconds and am or pm.

We need to see the decimal point after the least significant digit of the minute in the seven-segment display to differentiate minutes from seconds. Likewise, we need to see the decimal point after the least significant digit of the hour in the seven-segment display so we enable the decimal point. To enable the decimal, point our three-bit concatenation value will be 010 and to blank a digit of the seven-segment display our three-bit concatenation value is 100.

The time counter module time_ctr is the module that combines the hour, minutes and seconds. It contains two sub-modules min_sec and hr. min_sec computes the time in minutes and seconds and produces a carryout while hr computes the time in hrs. and the am and pm functionality.

Counting in minutes and seconds

The min_sec module contains four instances of the counter module counter_rc_mod. counter_rc_mod is a parametrized counting module with an enable that counts up to the parametrized value and then produces a carry output before restarting. We instantiate this module and override its parameterized value mod to count to that value. To count the time in seconds, we override this value with 10 since the least significant digit of the seven-segment display should only display values 0-9. The enable signal to this module comes from our parameterized delay module period_enb. After counting to 10, a carryout is produced. This carry out becomes the enable signal of the next counter that counts the second digit of the time in seconds. Since we only have up to 60 seconds before we advance to a minute, we instantiate counter_rc_mod and override mod with the value 6. This way, a carry output is generated each time we reach the value six. The carry out from that second instance of counter-rc_mod is used as the enable to the third counter (first counter of minutes). Since we can only count up to 60 minutes the procedure for instantiating and overriding the counter_rc_mod instances are similar to those of seconds. This module produces a carry out (from the fourth counter). This will be the enable signal to the hr counter

Counting time in hrs and generating am/pm

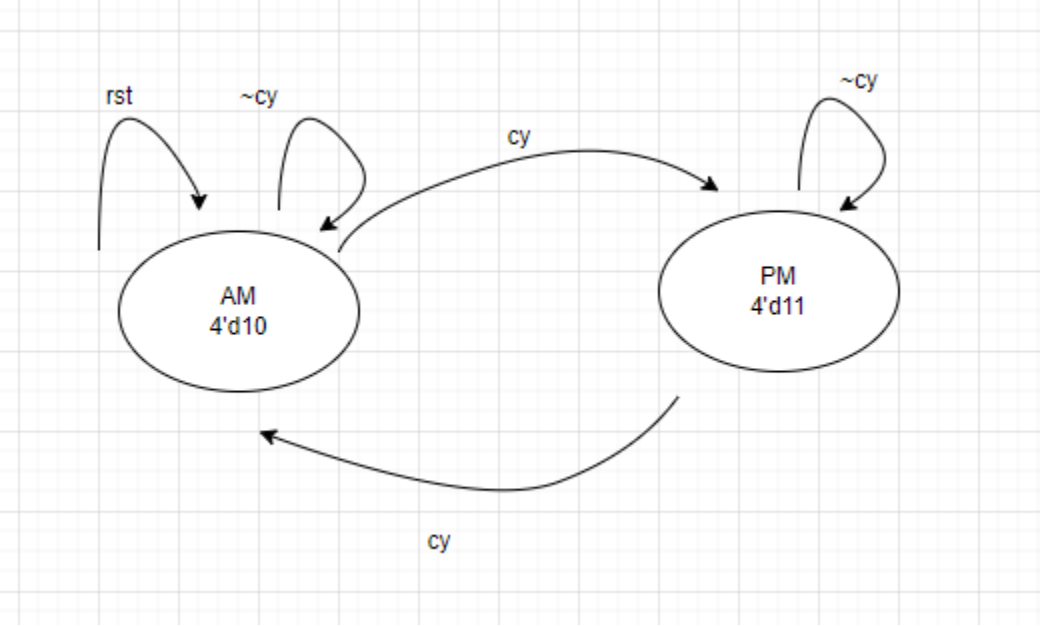
Producing the value for hours requires some special consideration and therefore we created a separate module name hr to do this. The default value of the clock should always be 12:00:00 am. That means that whenever the clock is reset the value of hrs has to be 12. This module like min_sec utilizes an instance of counter_rc_mod. The enable signal for the counter comes from the carryout of min_sec.

However, in this case the parameter mod is overridden with the value 12. This is because we are using the twelve hr system and we can only go through a cycle of 12 hrs. before transitioning from am to pm. When hr counter starts counting, it should always produce a twelve instead of a zero. So, every time the counter restarts high we check for this condition.

To produce an am or pm output we have to be careful. We need some form of storage to remember the last state we were in. This requires the use of a finite state machine with two states AM and PM. I We check for the condition when counter_rc_mod in this module produces a carry out. If carry out goes high, then the state should change from AM to PM if it was in the AM state and vice versa. In each state we specify a 4bit constant that corresponds to the decimal equivalent of the letter A for AM or P for PM

in the seven-segment decoder. The seven-segment display has no way to display the letter M so we just use the letters A and P.

The figure below shows the finite state machine



Manipulation of the time by the user

An important part of the clock design is to allow the user to change the time. When adv_min is pressed, the time in seconds should remain the same while time in seconds should advance by one. When adv_hr is pressed the time in minutes and seconds should remain the same while the time in hrs should advance by one. To achieve this functionality, we take the adv_min and adv_hr signal and invert them such that when they are asserted by the user, they are always active low rather than high. We then and this inverted forms with the period enable signal from pe_enb. The output of the AND gate becomes our enable signal to the first instance of counter_rc_mode. At the other end of the second counter, the adv_min signal is ANDed with the period enable signal to delay the set time by one second and the result is ORed with the carry out of the second counter. The result becomes the enable signal of the third counter (the counter that starts counting in minutes); The same is also done with adv_min at the end of the fourth counter of min_sec

The way this works is that when either adv_hr or adv_min is high, the AND produces an active low signal. This in turn stops the first counter from counting thus retaining its value. If adv_min is high and adv_hr is low the enable signal to the third counter is high so the value of minutes increases by one every millisecond. If adv_hr is high and adv_min is low, there is no enable to minute while hr is enabled. The hr advances by one while minutes and seconds retain their value.

Displaying the time

The outputs of dig_clock are fed into the seven-segment controller that was described in lab1.

Design realization

The design described above was the interfaced with the NEXYSA7 100T PCB by writing the constraints in XDC in Vivado suite. The design was elaborate, synthesized, implemented, routed and bitstream generated. We then programmed our device and observed the behavior of clock on the seven segment display.

3. Results

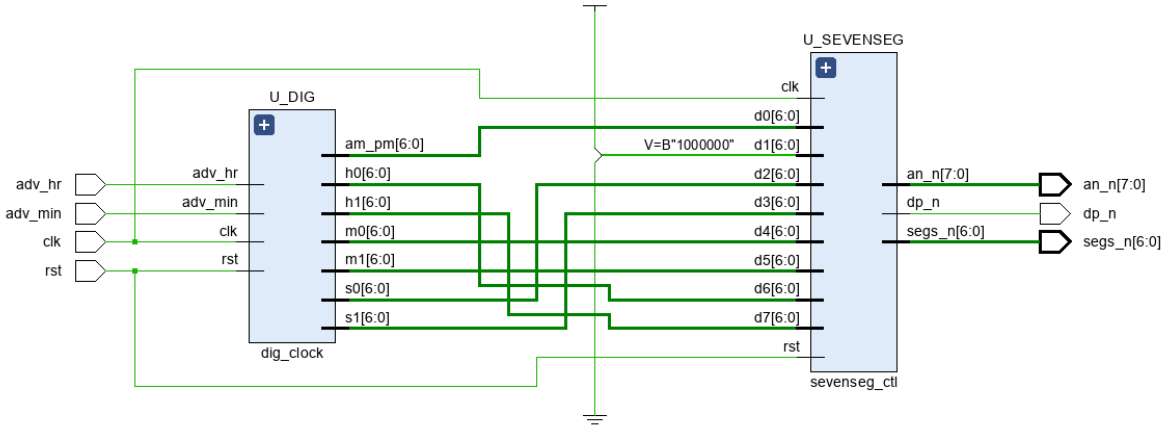


Figure 1 schematic diagram for the dig_clock_top

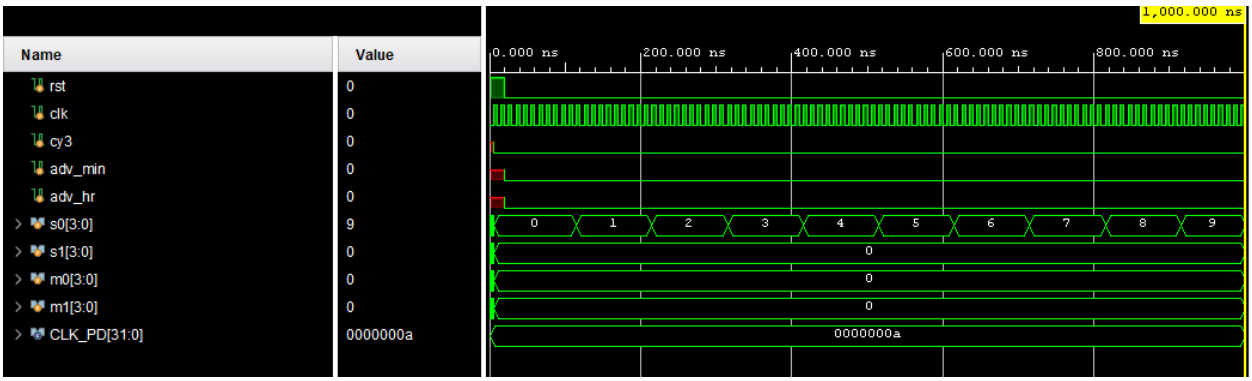


Figure 2 A copy of the simulation scope for min_sec

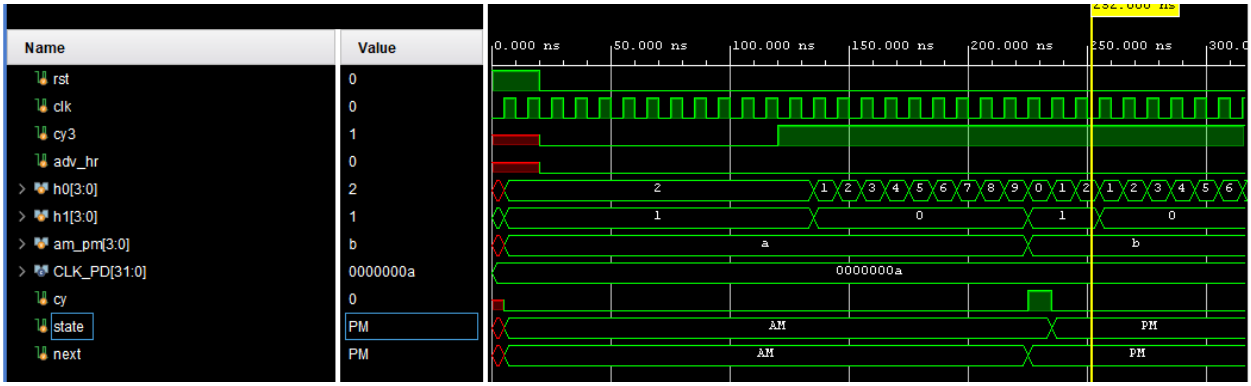


Figure 3 simulation scope for hr

The synthesis report

#---

 # Vivado v2020.2 (64-bit)

 # SW Build 3064766 on Wed Nov 18 09:12:45 MST 2020

 # IP Build 3064653 on Wed Nov 18 14:17:31 MST 2020

 # Start of session at: Mon Oct 2 00:10:47 2023

 # Process ID: 8696

 # Current directory: C:/Users/otienom/Documents/lab_02/lab_02.runs/synth_1

 # Command line: vivado.exe -log dig_clock_top.vds -product Vivado -mode batch -messageDb vivado.pb -notrace -source dig_clock_top.tcl

 # Log file: C:/Users/otienom/Documents/lab_02/lab_02.runs/synth_1/dig_clock_top.vds

 # Journal file: C:/Users/otienom/Documents/lab_02/lab_02.runs/synth_1\vivado.jou

#---

source dig_clock_top.tcl -notrace

Command: synth_design -top dig_clock_top -part xc7a100tcsg324-1

Starting synth_design

Attempting to get a license for feature 'Synthesis' and/or device 'xc7a100t'

INFO: [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a100t'

INFO: [Device 21-403] Loading part xc7a100tcsg324-1

INFO: [Synth 8-7079] Multithreading enabled for synth_design using a maximum of 2 processes.

INFO: [Synth 8-7078] Launching helper process for spawning children vivado processes

INFO: [Synth 8-7075] Helper process launched with PID 5876

Starting RTL Elaboration : Time (s): cpu = 00:00:00 ; elapsed = 00:00:03 . Memory (MB): peak = 1141.848 ; gain = 32.086

INFO: [Synth 8-6157] synthesizing module 'dig_clock_top' [C:/Users/otienom/Lab02/Lab02.srcs/sources_1/new/clock.sv:22]

INFO: [Synth 8-6157] synthesizing module 'dig_clock' [C:/Users/otienom/Lab02/Lab02.srcs/sources_1/new/dig_clock.sv:28]

INFO: [Synth 8-6157] synthesizing module 'time_ctr' [C:/Users/otienom/Lab02/Lab02.srcs/sources_1/new/time_ctr.sv:22]

INFO: [Synth 8-6157] synthesizing module 'hr' [C:/Users/otienom/Lab02/Lab02.srcs/sources_1/new/hr.sv:23]

INFO: [Synth 8-6157] synthesizing module 'period_enb' [C:/Users/otienom/Lab02/Lab02.srcs/sources_1/new/period_enb.sv:1]

Parameter PERIOD_MS bound to: 1000 - type: integer

Parameter PERIOD_US bound to: 1000000 - type: integer

Parameter PERIOD_NS bound to: 1000000000 - type: integer

Parameter CLKFREQ_MHZ bound to: 100 - type: integer

Parameter CLKPD_NS bound to: 10 - type: integer

Parameter PERIOD_COUNT_LIMIT bound to: 100000000 - type: integer

Parameter PERIOD_COUNT_BITS bound to: 27 - type: integer

INFO: [Synth 8-6155] done synthesizing module 'period_enb' (1#1) [C:/Users/otienom/Lab02/Lab02.srcs/sources_1/new/period_enb.sv:1]

INFO: [Synth 8-6157] synthesizing module 'counter_rc_mod' [C:/Users/otienom/Lab02/Lab02.srcs/sources_1/new/counter_rc_mod.sv:11]

Parameter MOD bound to: 12 - type: integer

INFO: [Synth 8-6155] done synthesizing module 'counter_rc_mod' (2#1) [C:/Users/otienom/Lab02/Lab02.srcs/sources_1/new/counter_rc_mod.sv:11]

INFO: [Synth 8-6157] synthesizing module 'dbl_dabble'
[C:/Users/otienom/Lab02/Lab02.srcs/sources_1/new/dbl_dabble.sv:15]

INFO: [Synth 8-251] dbl_dabble input: x
[C:/Users/otienom/Lab02/Lab02.srcs/sources_1/new/dbl_dabble.sv:24]

INFO: [Synth 8-251] shift 1 4'bxxxx 4'bxxxx 4'bxxxx 8'bxxxxxxxx
[C:/Users/otienom/Lab02/Lab02.srcs/sources_1/new/dbl_dabble.sv:39]

INFO: [Synth 8-251] shift 2 4'bxxxx 4'bxxxx 4'bxxxx 8'bxxxxxxxx
[C:/Users/otienom/Lab02/Lab02.srcs/sources_1/new/dbl_dabble.sv:39]

INFO: [Synth 8-251] shift 3 4'bxxxx 4'bxxxx 4'bxxxx 8'bxxxxxxxx
[C:/Users/otienom/Lab02/Lab02.srcs/sources_1/new/dbl_dabble.sv:39]

INFO: [Synth 8-251] add3o 4 4'bxxxx 4'bxxxx 4'bxxxx 8'bxxxxxxxx
[C:/Users/otienom/Lab02/Lab02.srcs/sources_1/new/dbl_dabble.sv:31]

INFO: [Synth 8-251] shift 4 4'bxxxx 4'bxxxx 4'bxxxx 8'bxxxxxxxx
[C:/Users/otienom/Lab02/Lab02.srcs/sources_1/new/dbl_dabble.sv:39]

INFO: [Synth 8-251] add3o 5 4'bxxxx 4'bxxxx 4'bxxxx 8'bxxxxxxxx
[C:/Users/otienom/Lab02/Lab02.srcs/sources_1/new/dbl_dabble.sv:31]

INFO: [Synth 8-251] shift 5 4'bxxxx 4'bxxxx 4'bxxxx 8'bxxxxxxxx
[C:/Users/otienom/Lab02/Lab02.srcs/sources_1/new/dbl_dabble.sv:39]

INFO: [Synth 8-251] add3o 6 4'bxxxx 4'bxxxx 4'bxxxx 8'bxxxxxxxx
[C:/Users/otienom/Lab02/Lab02.srcs/sources_1/new/dbl_dabble.sv:31]

INFO: [Synth 8-251] shift 6 4'bxxxx 4'bxxxx 4'bxxxx 8'bxxxxxxxx
[C:/Users/otienom/Lab02/Lab02.srcs/sources_1/new/dbl_dabble.sv:39]

INFO: [Synth 8-251] add3o 7 4'bxxxx 4'bxxxx 4'bxxxx 8'bxxxxxxxx
[C:/Users/otienom/Lab02/Lab02.srcs/sources_1/new/dbl_dabble.sv:31]

INFO: [Synth 8-251] add3t 7 4'bxxxx 4'bxxxx 4'bxxxx 8'bxxxxxxxx
[C:/Users/otienom/Lab02/Lab02.srcs/sources_1/new/dbl_dabble.sv:35]

INFO: [Synth 8-251] shift 7 4'bxxxx 4'bxxxx 4'bxxxx 8'bxxxxxxxx
[C:/Users/otienom/Lab02/Lab02.srcs/sources_1/new/dbl_dabble.sv:39]

INFO: [Synth 8-251] add3o 8 4'bxxxx 4'bxxxx 4'bxxxx 8'bxxxxxxxx
[C:/Users/otienom/Lab02/Lab02.srcs/sources_1/new/dbl_dabble.sv:31]

INFO: [Synth 8-251] add3t 8 4'bxxxx 4'bxxxx 4'bxxxx 8'bxxxxxxxx
[C:/Users/otienom/Lab02/Lab02.srcs/sources_1/new/dbl_dabble.sv:35]

INFO: [Synth 8-251] shift 8 4'bxxxx 4'bxxxx 4'bxxxx 8'bxxxxxxxx
[C:/Users/otienom/Lab02/Lab02.srcs/sources_1/new/dbl_dabble.sv:39]

INFO: [Synth 8-251] result x x x
[C:/Users/otienom/Lab02/Lab02.srcs/sources_1/new/dbl_dabble.sv:41]

INFO: [Synth 8-6155] done synthesizing module 'dbl_dabble' (3#1)
[C:/Users/otienom/Lab02/Lab02.srcs/sources_1/new/dbl_dabble.sv:15]

INFO: [Synth 8-6155] done synthesizing module 'hr' (4#1)
[C:/Users/otienom/Lab02/Lab02.srcs/sources_1/new/hr.sv:23]

INFO: [Synth 8-6157] synthesizing module 'min_sec'
[C:/Users/otienom/Lab02/Lab02.srcs/sources_1/new/min_sec.sv:37]

INFO: [Synth 8-6157] synthesizing module 'counter_rc_mod__parameterized0'
[C:/Users/otienom/Lab02/Lab02.srcs/sources_1/new/counter_rc_mod.sv:11]

Parameter MOD bound to: 10 - type: integer

INFO: [Synth 8-6155] done synthesizing module 'counter_rc_mod__parameterized0' (4#1)
[C:/Users/otienom/Lab02/Lab02.srcs/sources_1/new/counter_rc_mod.sv:11]

INFO: [Synth 8-6157] synthesizing module 'counter_rc_mod__parameterized1'
[C:/Users/otienom/Lab02/Lab02.srcs/sources_1/new/counter_rc_mod.sv:11]

Parameter MOD bound to: 6 - type: integer

INFO: [Synth 8-6155] done synthesizing module 'counter_rc_mod__parameterized1' (4#1)
[C:/Users/otienom/Lab02/Lab02.srcs/sources_1/new/counter_rc_mod.sv:11]

INFO: [Synth 8-6155] done synthesizing module 'min_sec' (5#1)
[C:/Users/otienom/Lab02/Lab02.srcs/sources_1/new/min_sec.sv:37]

INFO: [Synth 8-6155] done synthesizing module 'time_ctr' (6#1)
[C:/Users/otienom/Lab02/Lab02.srcs/sources_1/new/time_ctr.sv:22]

INFO: [Synth 8-6155] done synthesizing module 'dig_clock' (7#1)
[C:/Users/otienom/Lab02/Lab02.srcs/sources_1/new/dig_clock.sv:28]

INFO: [Synth 8-6157] synthesizing module 'sevenseg_ctl'
[C:/Users/otienom/Lab02/Lab02.srcs/sources_1/new/sevenseg_ctl.sv:18]

INFO: [Synth 8-6157] synthesizing module 'period_enb__parameterized0'
[C:/Users/otienom/Lab02/Lab02.srcs/sources_1/new/period_enb.sv:1]

Parameter PERIOD_MS bound to: 1 - type: integer

Parameter PERIOD_US bound to: 1000 - type: integer

Parameter PERIOD_NS bound to: 1000000 - type: integer

Parameter CLKFREQ_MHZ bound to: 100 - type: integer

Parameter CLKPD_NS bound to: 10 - type: integer

Parameter PERIOD_COUNT_LIMIT bound to: 100000 - type: integer

Parameter PERIOD_COUNT_BITS bound to: 17 - type: integer

INFO: [Synth 8-6155] done synthesizing module 'period_enb__parameterized0' (7#1)
[C:/Users/otienom/Lab02/Lab02.srcs/sources_1/new/period_enb.sv:1]

INFO: [Synth 8-6157] synthesizing module 'counter'
[C:/Users/otienom/Lab02/Lab02.srcs/sources_1/new/counter.sv:23]

Parameter W bound to: 3 - type: integer

INFO: [Synth 8-6155] done synthesizing module 'counter' (8#1)
[C:/Users/otienom/Lab02/Lab02.srcs/sources_1/new/counter.sv:23]

INFO: [Synth 8-6157] synthesizing module 'dec_3_8_n'
[C:/Users/otienom/Lab02/Lab02.srcs/sources_1/new/dec_3_8.sv:11]

INFO: [Synth 8-226] default block is never used
[C:/Users/otienom/Lab02/Lab02.srcs/sources_1/new/dec_3_8.sv:19]

INFO: [Synth 8-6155] done synthesizing module 'dec_3_8_n' (9#1)
[C:/Users/otienom/Lab02/Lab02.srcs/sources_1/new/dec_3_8.sv:11]

INFO: [Synth 8-6157] synthesizing module 'mux8'
[C:/Users/otienom/Lab02/Lab02.srcs/sources_1/new/mux8.sv:11]

Parameter W bound to: 7 - type: integer

INFO: [Synth 8-226] default block is never used
[C:/Users/otienom/Lab02/Lab02.srcs/sources_1/new/mux8.sv:18]

INFO: [Synth 8-6155] done synthesizing module 'mux8' (10#1)
[C:/Users/otienom/Lab02/Lab02.srcs/sources_1/new/mux8.sv:11]

INFO: [Synth 8-6157] synthesizing module 'sevenseg_ext'
[C:/Users/otienom/Lab02/Lab02.srcs/sources_1/new/sevenseg_ext.sv:23]

INFO: [Synth 8-6155] done synthesizing module 'sevenseg_ext' (11#1)
[C:/Users/otienom/Lab02/Lab02.srcs/sources_1/new/sevenseg_ext.sv:23]

INFO: [Synth 8-6155] done synthesizing module 'sevenseg_ctl' (12#1)
[C:/Users/otienom/Lab02/Lab02.srcs/sources_1/new/sevenseg_ctl.sv:18]

INFO: [Synth 8-6155] done synthesizing module 'dig_clock_top' (13#1)
[C:/Users/otienom/Lab02/Lab02.srcs/sources_1/new/clock.sv:22]

Finished RTL Elaboration : Time (s): cpu = 00:00:01 ; elapsed = 00:00:04 . Memory (MB): peak = 1194.891 ; gain = 85.129

Start Handling Custom Attributes

Finished Handling Custom Attributes : Time (s): cpu = 00:00:01 ; elapsed = 00:00:04 . Memory (MB): peak = 1194.891 ; gain = 85.129

Finished RTL Optimization Phase 1 : Time (s): cpu = 00:00:01 ; elapsed = 00:00:04 . Memory (MB): peak = 1194.891 ; gain = 85.129

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.002 . Memory (MB): peak = 1194.891 ; gain = 0.000

INFO: [Project 1-570] Preparing netlist for logic optimization

Processing XDC Constraints

Initializing timing engine

Parsing XDC File [C:/Users/otienom/Lab02/Lab02.srcs/constrs_1/new/sevenseg_ctl_const.xdc]

Finished Parsing XDC File [C:/Users/otienom/Lab02/Lab02.srcs/constrs_1/new/sevenseg_ctl_const.xdc]

INFO: [Project 1-236] Implementation specific constraints were found while reading constraint file [C:/Users/otienom/Lab02/Lab02.srcs/constrs_1/new/sevenseg_ctl_const.xdc]. These constraints will be ignored for synthesis but will be used in implementation. Impacted constraints are listed in the file [.Xil/dig_clock_top_propImpl.xdc].

Resolution: To avoid this warning, move constraints listed in [.Xil/dig_clock_top_propImpl.xdc] to another XDC file and exclude this new file from synthesis with the used_in_synthesis property (File Properties dialog in GUI) and re-run elaboration/synthesis.

Completed Processing XDC Constraints

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1311.352 ; gain = 0.000

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

Constraint Validation Runtime : Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.003 . Memory (MB): peak = 1311.352 ; gain = 0.000

Finished Constraint Validation : Time (s): cpu = 00:00:02 ; elapsed = 00:00:08 . Memory (MB): peak = 1311.352 ; gain = 201.590

Start Loading Part and Timing Information

Loading part: xc7a100tcsg324-1

Finished Loading Part and Timing Information : Time (s): cpu = 00:00:02 ; elapsed = 00:00:08 . Memory (MB): peak = 1311.352 ; gain = 201.590

Start Applying 'set_property' XDC Constraints

Finished applying 'set_property' XDC Constraints : Time (s): cpu = 00:00:02 ; elapsed = 00:00:08 . Memory (MB): peak = 1311.352 ; gain = 201.590

Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:02 ; elapsed = 00:00:08 . Memory (MB): peak = 1311.352 ; gain = 201.590

Start RTL Component Statistics

Detailed RTL Component Info :

+---Adders :

2 Input 4 Bit Adders := 12

2 Input 3 Bit Adders := 1

+---Registers :

4 Bit Registers := 6

3 Bit Registers := 1

1 Bit Registers := 1

+---Muxes :

8 Input 8 Bit Muxes := 1

2 Input 7 Bit Muxes := 1

17 Input 7 Bit Muxes := 1

2 Input 4 Bit Muxes := 7

4 Input 4 Bit Muxes := 1

2 Input 1 Bit Muxes := 2

3 Input 1 Bit Muxes := 1

Finished RTL Component Statistics

Start Part Resource Summary

Part Resources:

DSPs: 240 (col length:80)

BRAMs: 270 (col length: RAMB18 80 RAMB36 40)

Finished Part Resource Summary

Start Cross Boundary and Area Optimization

Finished Cross Boundary and Area Optimization : Time (s): cpu = 00:00:04 ; elapsed = 00:00:13 . Memory (MB): peak = 1412.316 ; gain = 302.555

Start Applying XDC Timing Constraints

Finished Applying XDC Timing Constraints : Time (s): cpu = 00:00:05 ; elapsed = 00:00:17 . Memory (MB): peak = 1412.316 ; gain = 302.555

Start Timing Optimization

Finished Timing Optimization : Time (s): cpu = 00:00:06 ; elapsed = 00:00:21 . Memory (MB): peak = 1596.992 ; gain = 487.230

Start Technology Mapping

Finished Technology Mapping : Time (s): cpu = 00:00:06 ; elapsed = 00:00:21 . Memory (MB): peak = 1596.992 ; gain = 487.230

Start IO Insertion

Start Flattening Before IO Insertion

Finished Flattening Before IO Insertion

Start Final Netlist Cleanup

Finished Final Netlist Cleanup

Finished IO Insertion : Time (s): cpu = 00:00:06 ; elapsed = 00:00:23 . Memory (MB): peak = 1596.992 ; gain = 487.230

Start Renaming Generated Instances

Finished Renaming Generated Instances : Time (s): cpu = 00:00:06 ; elapsed = 00:00:23 . Memory (MB): peak = 1596.992 ; gain = 487.230

Start Rebuilding User Hierarchy

Finished Rebuilding User Hierarchy : Time (s): cpu = 00:00:06 ; elapsed = 00:00:23 . Memory (MB): peak = 1596.992 ; gain = 487.230

Start Renaming Generated Ports

Finished Renaming Generated Ports : Time (s): cpu = 00:00:06 ; elapsed = 00:00:23 . Memory (MB): peak = 1596.992 ; gain = 487.230

Start Handling Custom Attributes

Finished Handling Custom Attributes : Time (s): cpu = 00:00:06 ; elapsed = 00:00:23 . Memory (MB): peak = 1596.992 ; gain = 487.230

Start Renaming Generated Nets

Finished Renaming Generated Nets : Time (s): cpu = 00:00:06 ; elapsed = 00:00:23 . Memory (MB): peak = 1596.992 ; gain = 487.230

Start Writing Synthesis Report

Report BlackBoxes:

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| |BlackBox name |Instances |

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Report Cell Usage:

	Cell	Count
1	BUFG	1
2	CARRY4	19
3	LUT1	8
4	LUT2	13
5	LUT3	21
6	LUT4	21
7	LUT5	5
8	LUT6	35
9	FDRE	97
10	FDSE	2
11	IBUF	4
12	OBUF	16

Finished Writing Synthesis Report : Time (s): cpu = 00:00:06 ; elapsed = 00:00:23 . Memory (MB): peak = 1596.992 ; gain = 487.230

Synthesis finished with 0 errors, 0 critical warnings and 0 warnings.

Synthesis Optimization Runtime : Time (s): cpu = 00:00:05 ; elapsed = 00:00:22 . Memory (MB): peak = 1596.992 ; gain = 370.770

Synthesis Optimization Complete : Time (s): cpu = 00:00:06 ; elapsed = 00:00:23 . Memory (MB): peak = 1596.992 ; gain = 487.230

INFO: [Project 1-571] Translating synthesized netlist

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.001 . Memory (MB): peak = 1596.992 ; gain = 0.000

INFO: [Netlist 29-17] Analyzing 19 Unisim elements for replacement

INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

INFO: [Project 1-570] Preparing netlist for logic optimization

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 1596.992 ; gain = 0.000

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

INFO: [Common 17-83] Releasing license: Synthesis

66 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.

synth_design completed successfully

synth_design: Time (s): cpu = 00:00:07 ; elapsed = 00:00:28 . Memory (MB): peak = 1596.992 ; gain = 487.230

INFO: [Common 17-1381] The checkpoint 'C:/Users/otienom/Documents/lab_02/lab_02.runs/synth_1/dig_clock_top.dcp' has been generated.

INFO: [runtcl-4] Executing : report_utilization -file dig_clock_top_utilization_synth.rpt -pb dig_clock_top_utilization_synth.pb

INFO: [Common 17-206] Exiting Vivado at Mon Oct 2 00:11:20 2023...

Conclusion

It was easier to implement the min and seconds counting than the hr counting because of the nature of how the 12 hr system works. It took quite some thinking to achieve the overall design but no significant challenges were met

Time spent on lab

7 hrs