數位系統導論 2021/4/14 作業

(不用繳交，4/21 隨堂抽考)

For each of the following digital designs, please

(a) Construct its truth table;

(b) Show the minterm & maxterm expansions respectively;

(c) Show the equations of the simplified SoP & PoS respectively;

(d) Draw the simplified 2-level full-NAND and full-NOR implementations respectively.

(e) Describe the full-NAND implementation in (d) with **Verilog structural modeling**, using `nand2(dout,d0,d1)`, `nand3(dout,d0,d1,d2)`, `nand4(dout,d0,d1,d2,d3)`, `nand5` … ,

1. A design that outputs logic "1" iff the corresponding decimal of its 4-bit **BCD** input $\{x_3\, x_2\, x_1\, x_0\}$ is prime

2. A design that outputs logic "1" iff the corresponding decimal of its 4-bit **BCD** input $\{x_3\, x_2\, x_1\, x_0\}$ is a Fibonacci number

3. A design that converts a 4-bit signed number $X = \{x_3\, x_2\, x_1\, x_0\}$ (2's complement) to its negated value (i.e. $Y = -X$; also in 2's complement)

4.