數位系統導論實驗 LAB 2

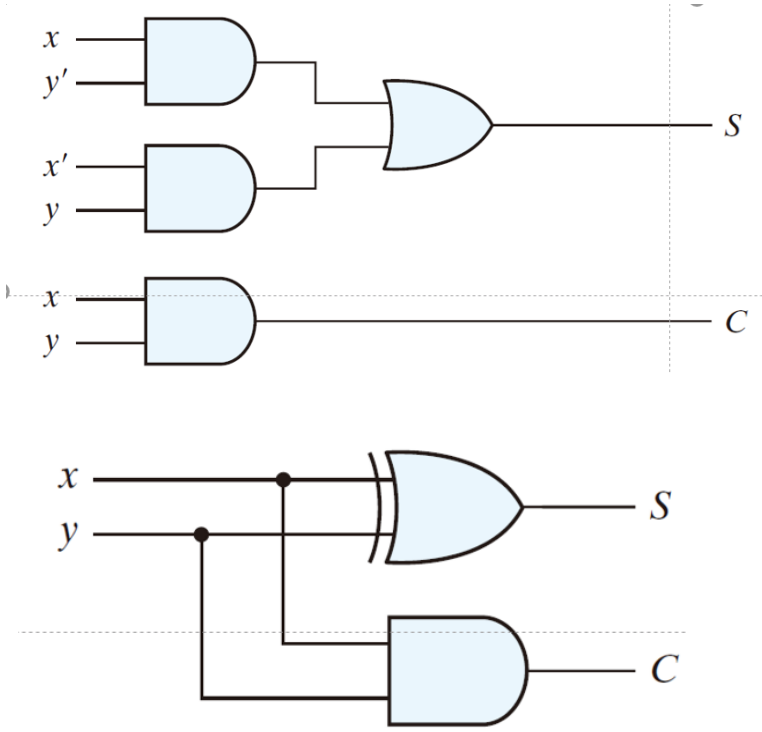
梁郁珮

1-BIT HALF ADDER (HA)

- Only can do **one-bit** addition

- Addition (1-bit)
  - 0 + 0 = 00
  - 0 + 1 = 01
  - 1 + 0 = 01
  - 1 + 1 = 10

x	Y	Carry	Sum
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0



$C = XY$

$S = X'Y + XY' = X \oplus Y$

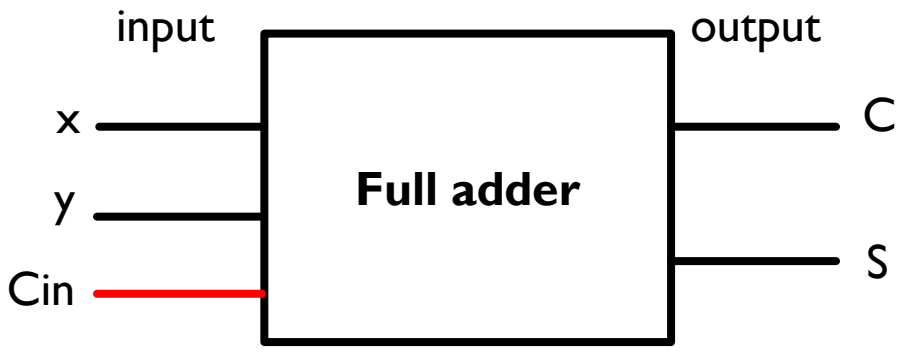
How to add more bit?

- A = (A3A2A1A0), B = (B3B2B1B0)
- A + B

```
          A3 A2 A1 A0
+)        B3 B2 B1 B0
-------------------------
     C  S3 S2 S1 S0
```

Example:

```
          1  1  1
          1  1  0  1
       +) 1  0  1  1
-------------------------
     1    1  0  0  0
```



Full adder

- three input bits
  - x, y: two significant bits
  - Z (Cin): the carry bit from the previous lower significant bit
- Two output bits: C(Cout), S

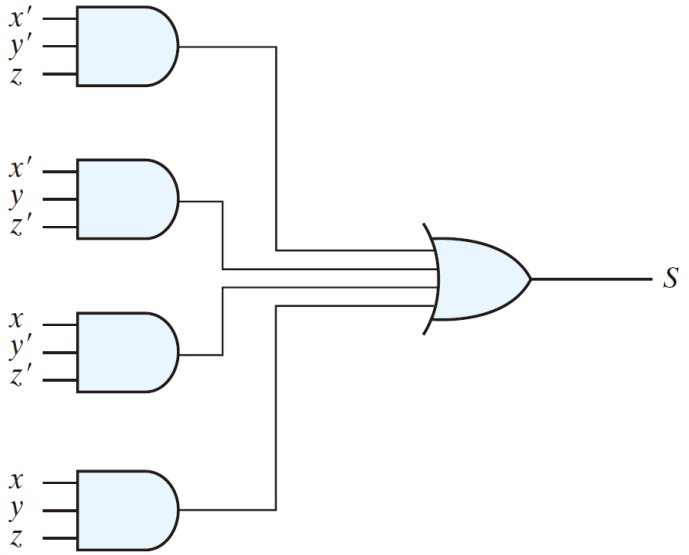
x	y	Cin	Cout	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

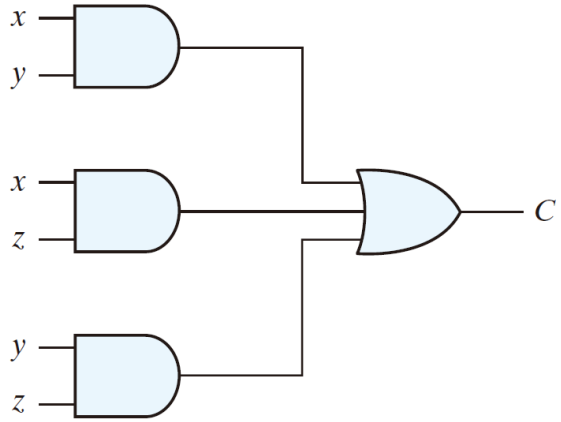
x	y	z	C	S
0	0	0	0	0
0	0	I	0	I
0	I	0	0	I
0	I	I	I	0
I	0	0	0	I
I	0	I	I	0
I	I	0	I	0
I	I	I	I	I

S = x‘y’z+x‘yz’+ xy‘z’+xyz = x⊕y⊕ z

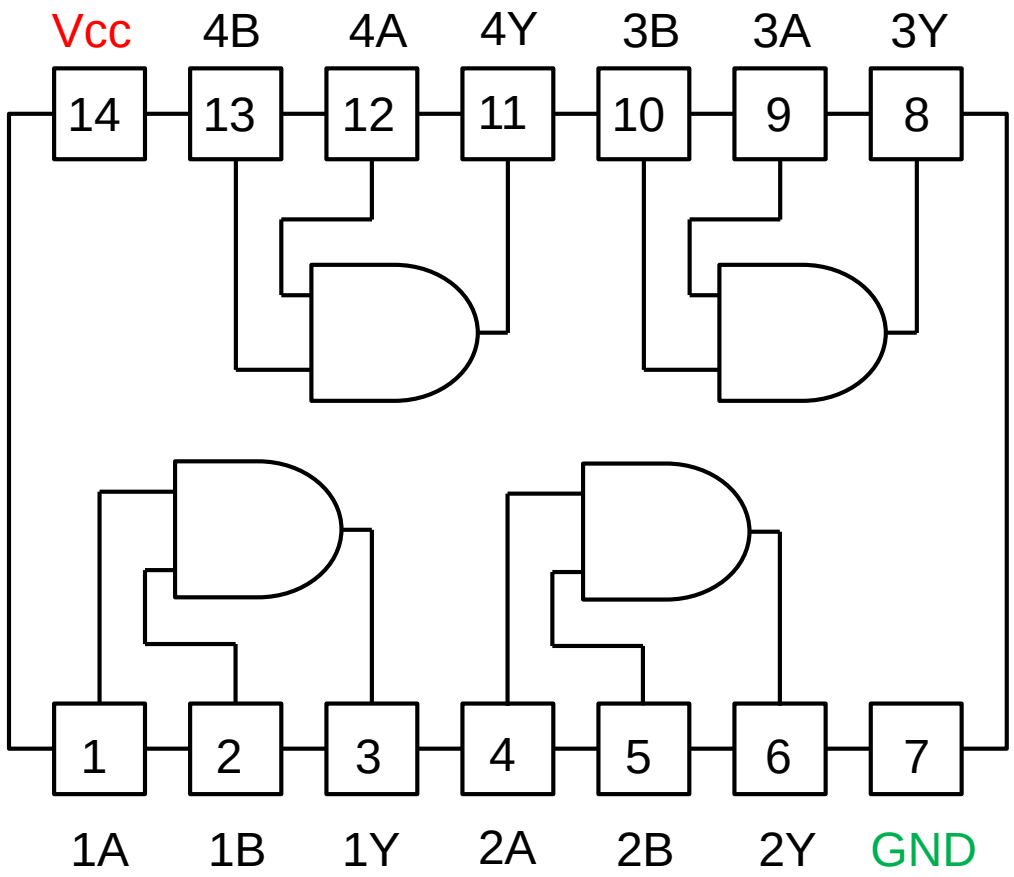
C = x’yz + xy’z + xyz’ + xyz

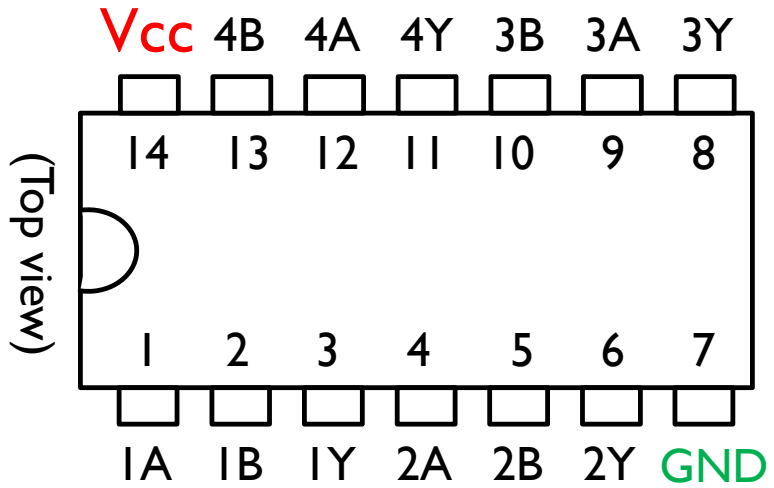
= xy + xz + yz





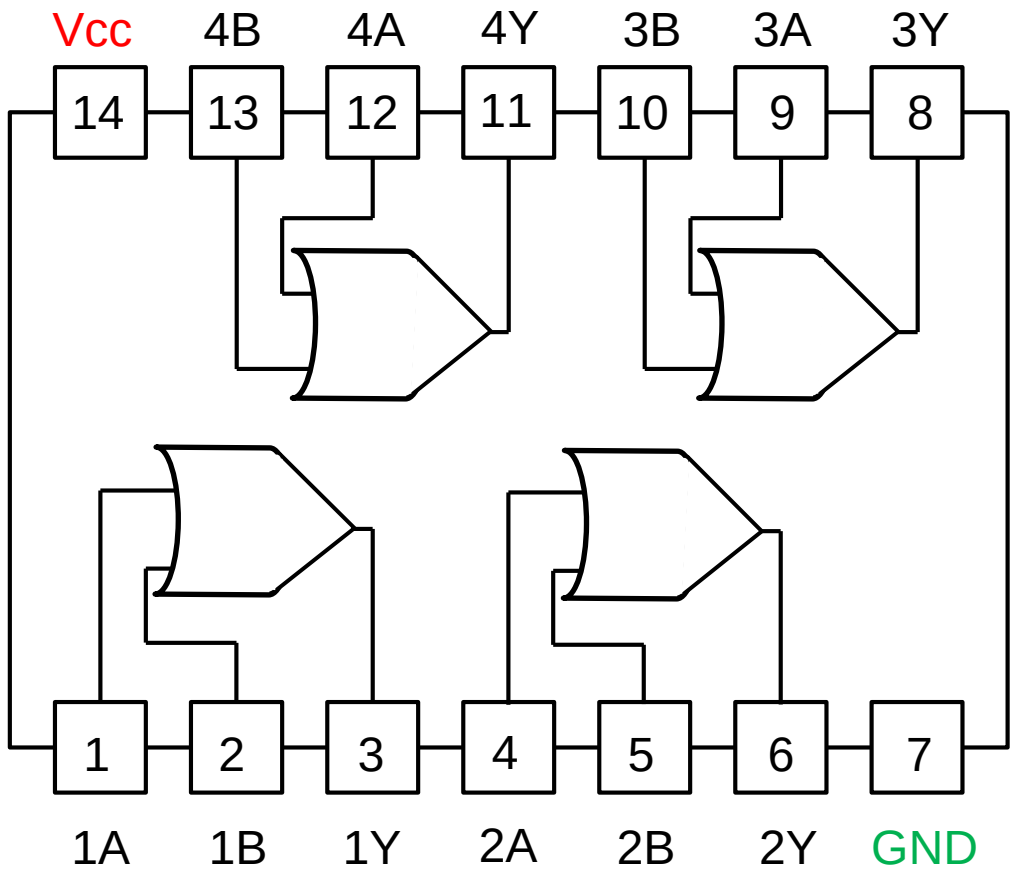
IC介紹(74LS08) 4＊TWO-INPUT AND GATE

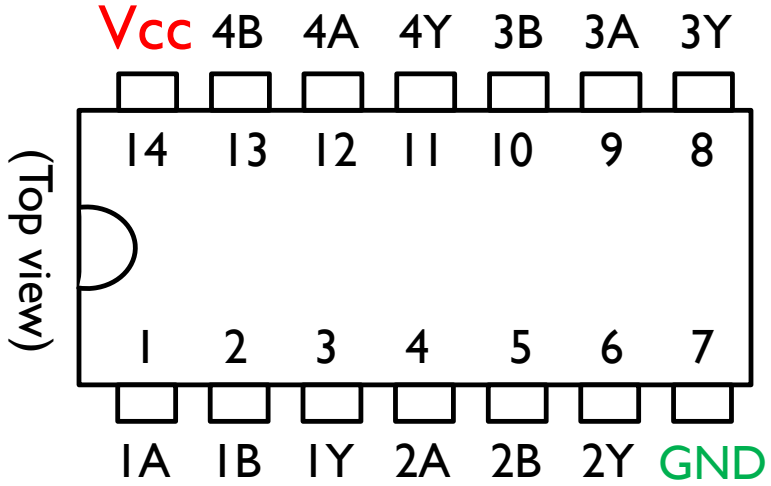




- 7及14接腳：接地及電源
- 1與2；4與5；9與10；12與13接腳：輸入腳位
- 3；6；8；11接腳：輸出腳位

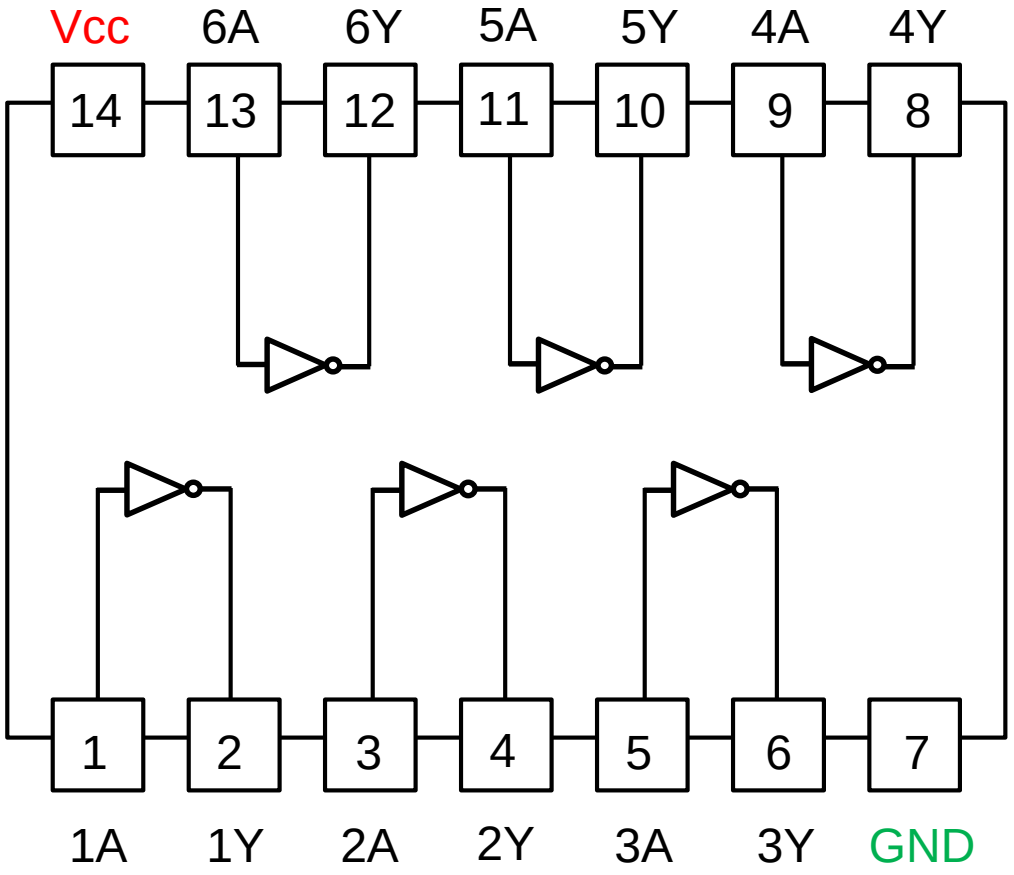
IC介紹(74LS32) 4＊TWO-INPUT OR GATE

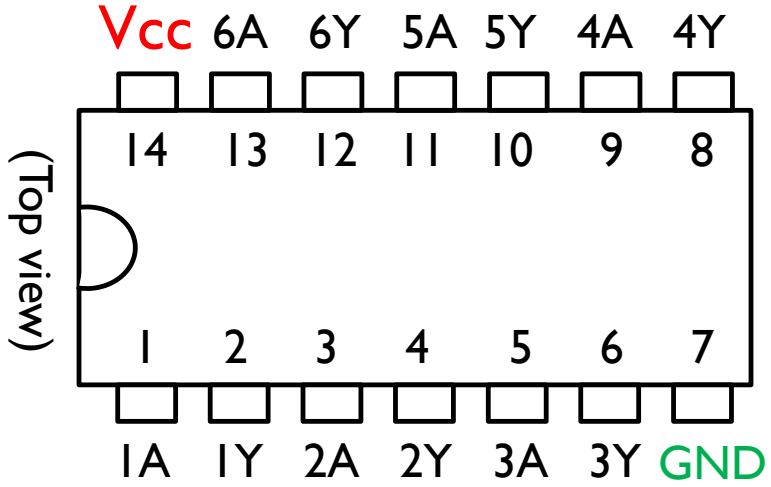




- 7及14接腳：接地及電源
- 1與2；4與5；9與10；12與13接腳：輸入腳位
- 3；6；8；11接腳：輸出腳位

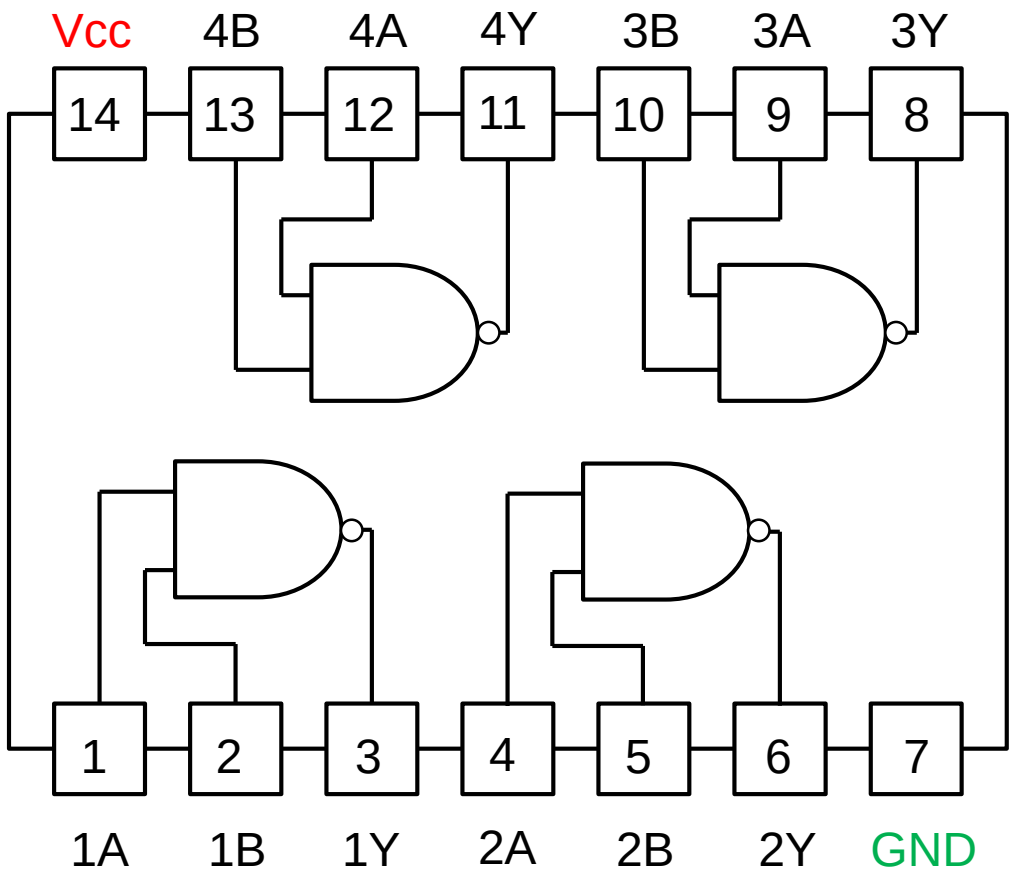
IC介紹(74LS04) 6 * NOT GATE

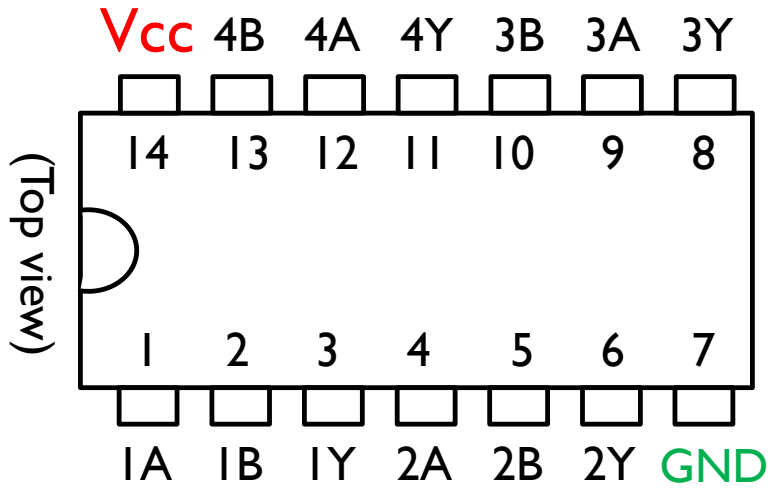




- 7及14接腳：接地及電源
- 1；3；5；9；11；13 接腳：輸入腳位
- 2；4；6；8；10；12 接腳：輸出腳位

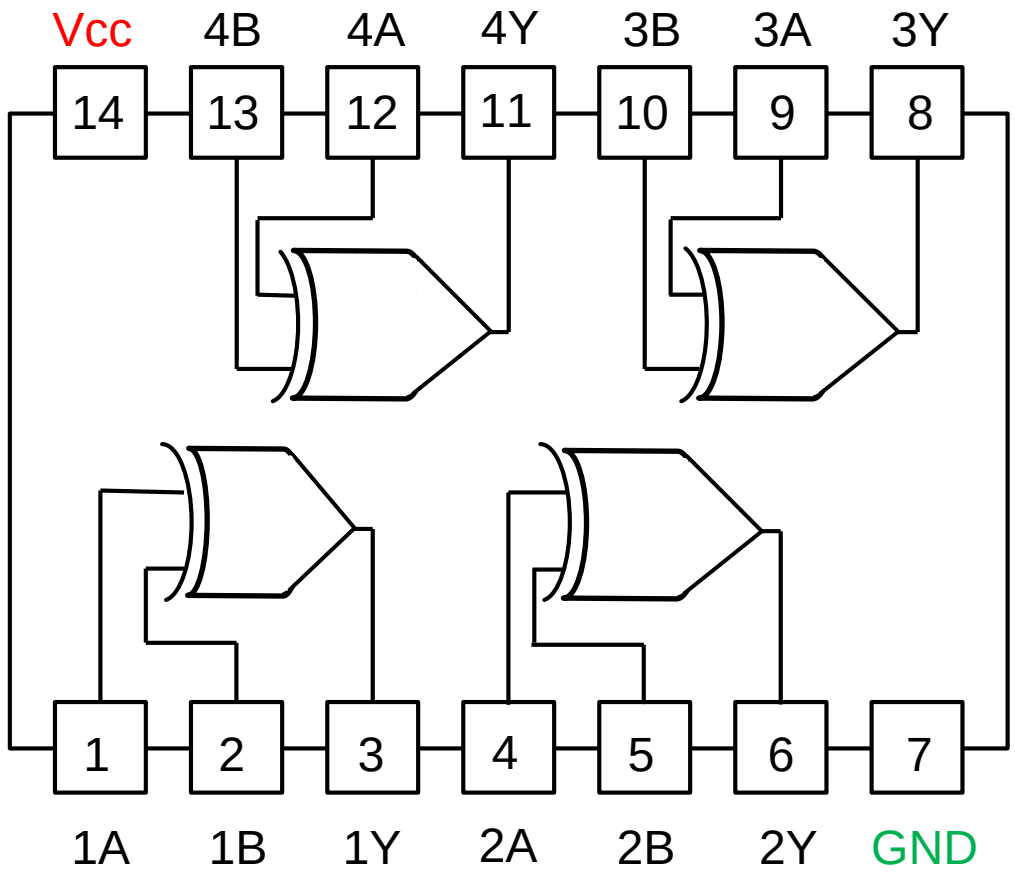
IC介紹(74LS00) 4＊TWO-INPUT NAND GATE

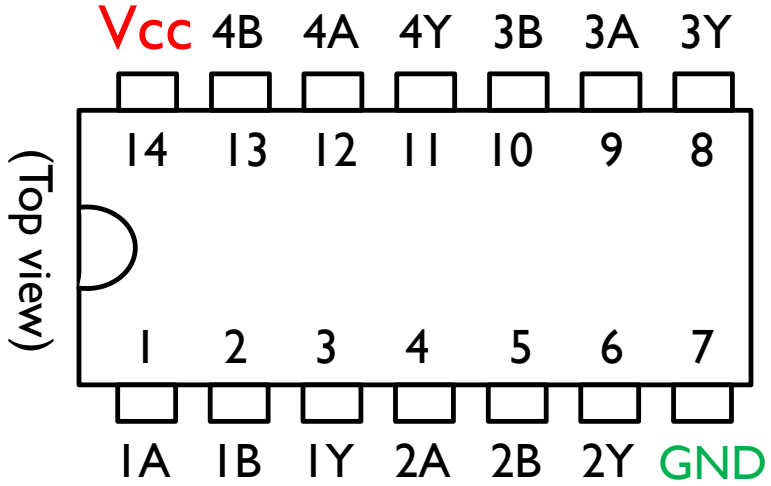




- 7及14接腳：接地及電源
- 1與2；4與5；9與10；12與13接腳：輸入腳位
- 3；6；8；11接腳：輸出腳位

IC介紹(74LS86) 4＊TWO-INPUT XOR GATE



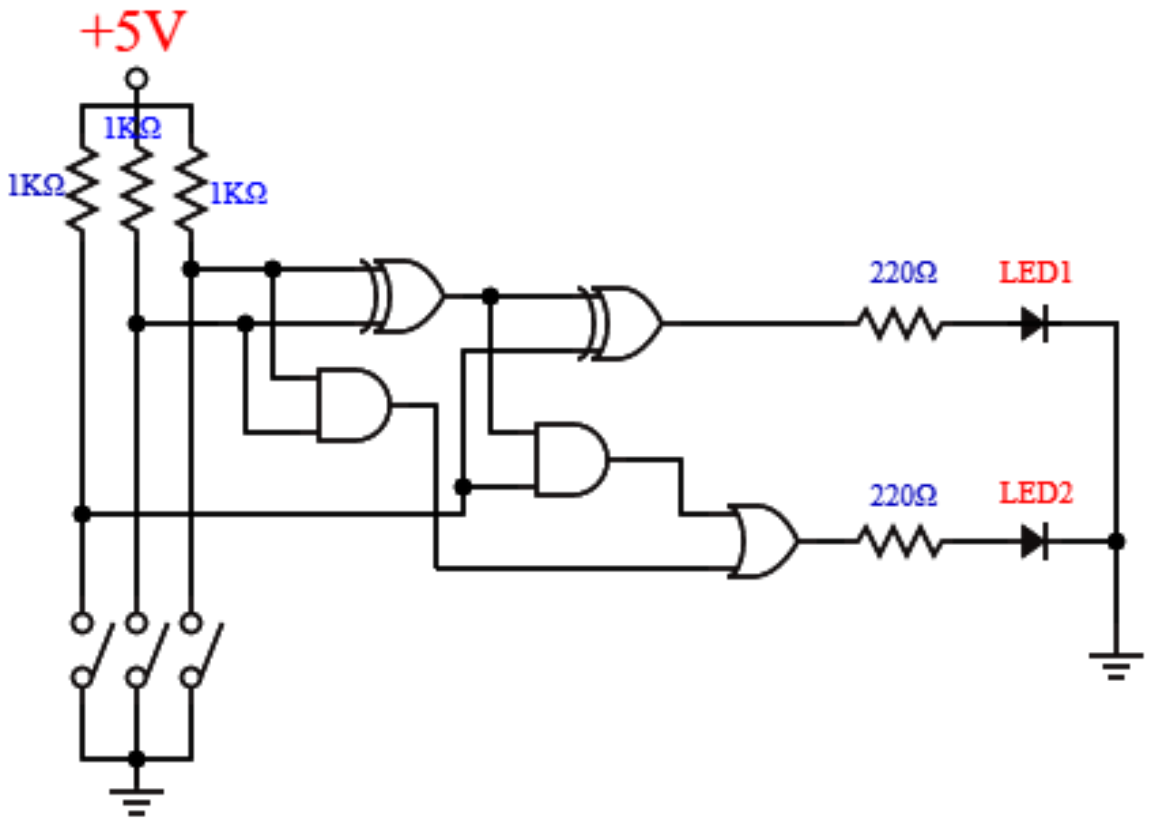


- 7及14接腳：接地及電源
- 1與2；4與5；9與10；12與13接腳：輸入腳位
- 3；6；8；11接腳：輸出腳位

- # Lab 2-1 Implementing a full adder

1. Please implement a full adder with the following circuit

74LS08 (AND), 74LS32(OR), 74LS86(XOR)



實驗注意事項

1. 調整任何電路前請先將電源輸出關閉(output關掉, 輸入端線路移除, DC電源供應器power關掉 …)，待電路調整完再開啟
2. 電源供應器需調整成 c.v. 模式，請注意c.v.燈號是否亮著
3. 輸入電壓固定為5V (請勿使用其他電壓)
4. 記得給IC正確的工作電壓 (腳位7, 14記得接地跟5V)

REPORT OF LAB 2 (4%)

The report should include …

1. Discuss why the circuit on P.11 equals to the results on P. 5

   (討論P. 11 與 P.5的電路為什麼相等)

2. Draw logic diagrams to implement a full subtractor, and write the design procedures and Boolean equations for the implementations

   (畫出以AND, OR, NOT, XOR實作全減器之接線圖，以及寫出設計過程及其布林函數)

3. Discussion and experience (everyone)

   (所有人的心得與討論)

- File type: pdf
- File name: Lab2_(Number of team)_report
- Deadline: 2022/3/28 24:00