

數位系統導論實驗

Quartus軟體操作

梁郁珮

軟體安裝

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Intel® Quartus® Prime Pro Edition Design Software Version 20.1 for Linux	660923	06/14/20	20.1	🔖 ▾

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軟體安裝

解壓縮並下載主程式

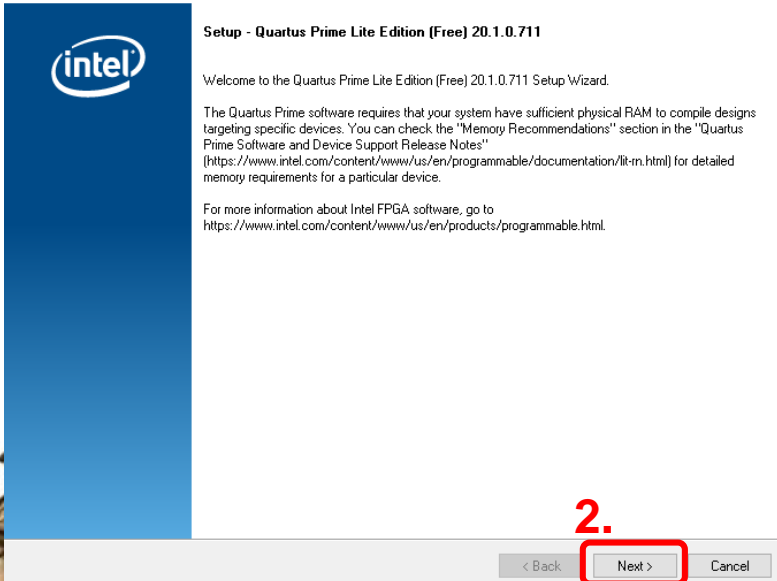
名稱

components

1. readme.txt

setup.bat

Installing Quartus Prime Lite Edition (Free) 20.1.0.711



Installing Quartus Prime Lite Edition (Free) 20.1.0.711

License Agreement



You can view the full license agreement at the link below or use -install_lic option from command-line to get the license agreement files before the installation. You must accept the terms of the agreement before continuing with the installation.

<http://ipgasoftware.intel.com/eula/>

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InstallBuilder

Installing Quartus Prime Lite Edition (Free) 20.1.0.711

Installation directory



5. Specify the directory where Quartus Prime Lite Edition (Free) 20.1.0.711 will be installed.

Installation directory: D:\quartus

InstallBuilder

6. < Back Next > Cancel

軟體安裝

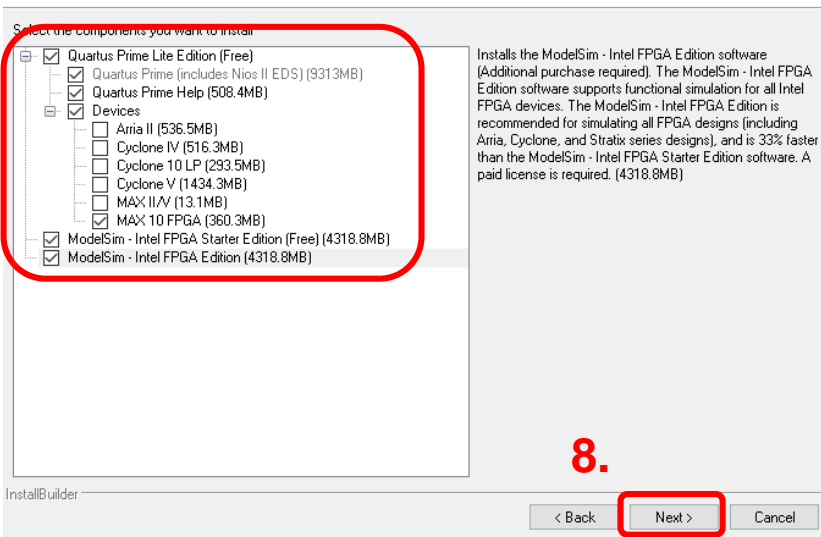
請注意選取的安裝內容

Installing Quartus Prime Lite Edition (Free) 20.1.0.711

Select Components



7.



8.

Installing Quartus Prime Lite Edition (Free) 20.1.0.711

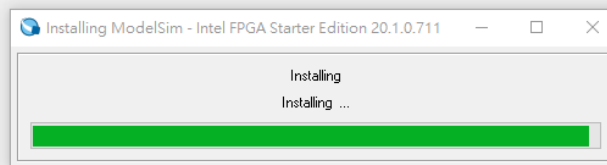
Installing



Wait while Setup installs Quartus Prime Lite Edition (Free) 20.1.0.711

Installing

Installing ModelSim - Intel FPGA Starter Edition (Free)...



InstallBuilder

< Back

Next >

Cancel



國立中正大學

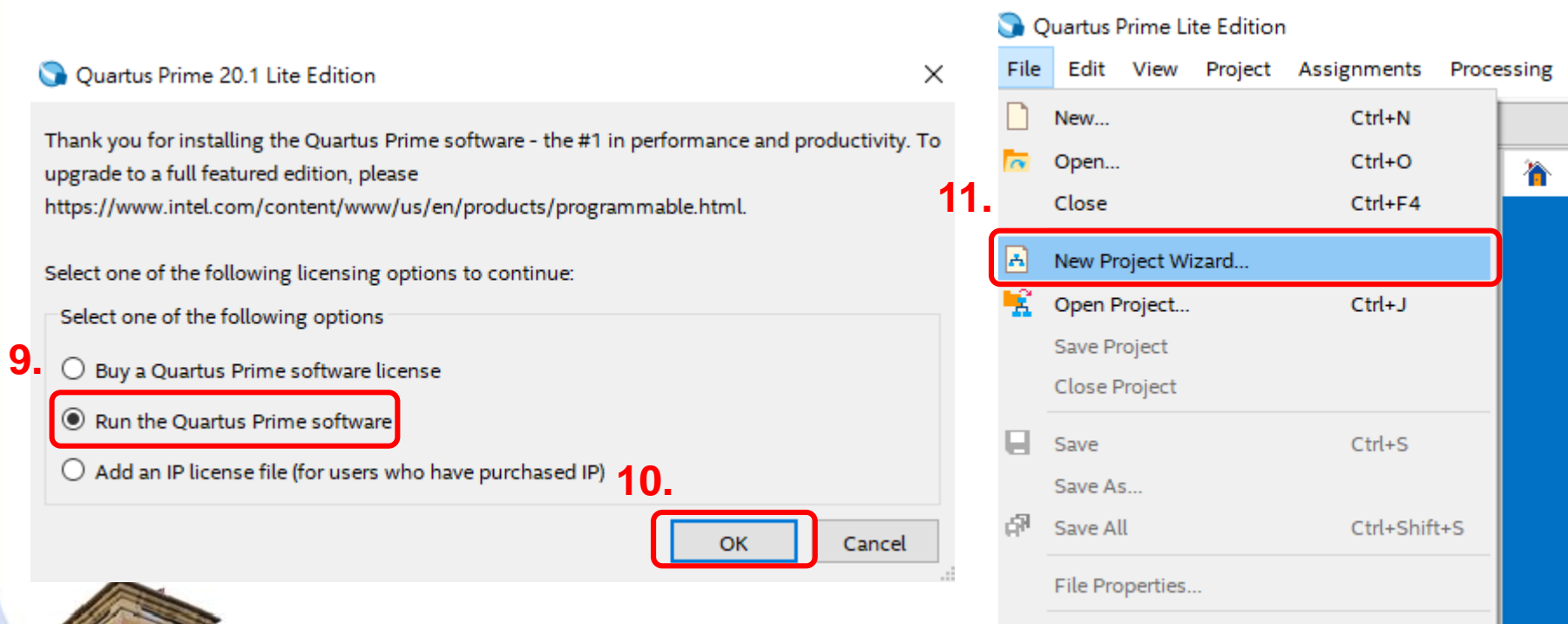
National Chung Cheng University



建立新專案

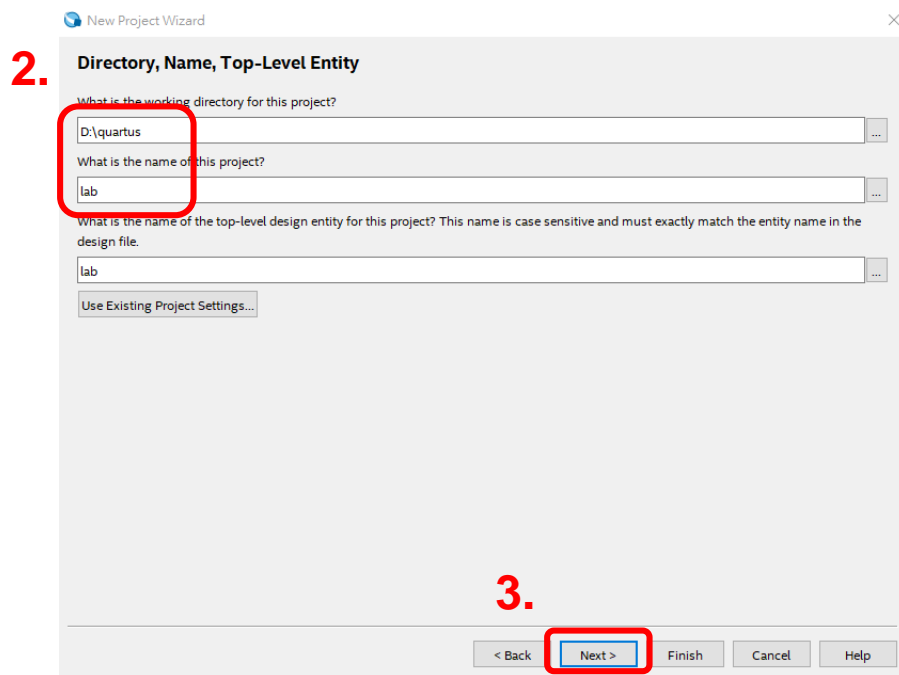
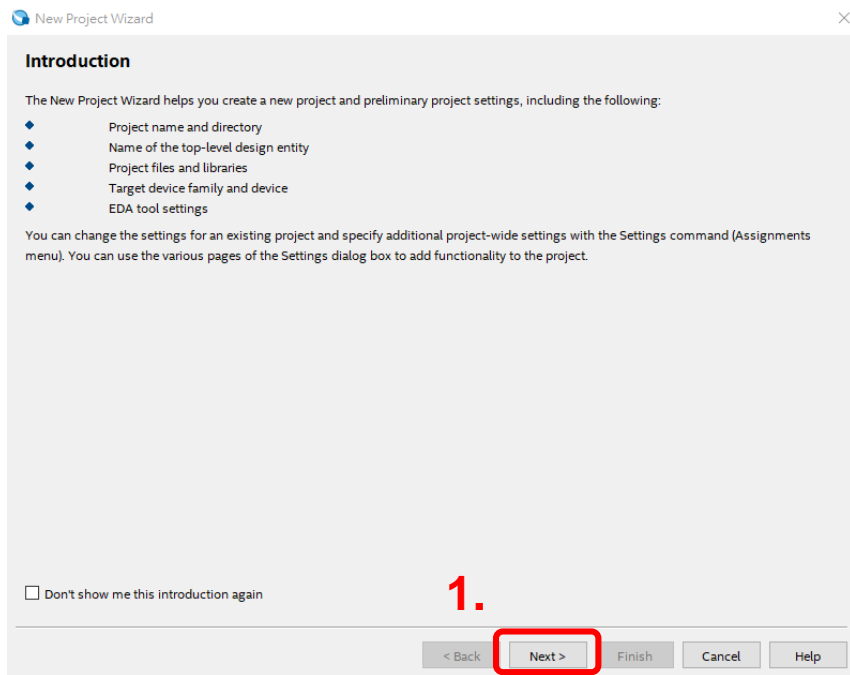
因Lite版本軟體為免費版，所以選擇第二個選項

選擇【File】/【New Project Wizard】開啟一個新的專案



建立新專案

命名專案名稱，檔案儲存路徑（自行決定）

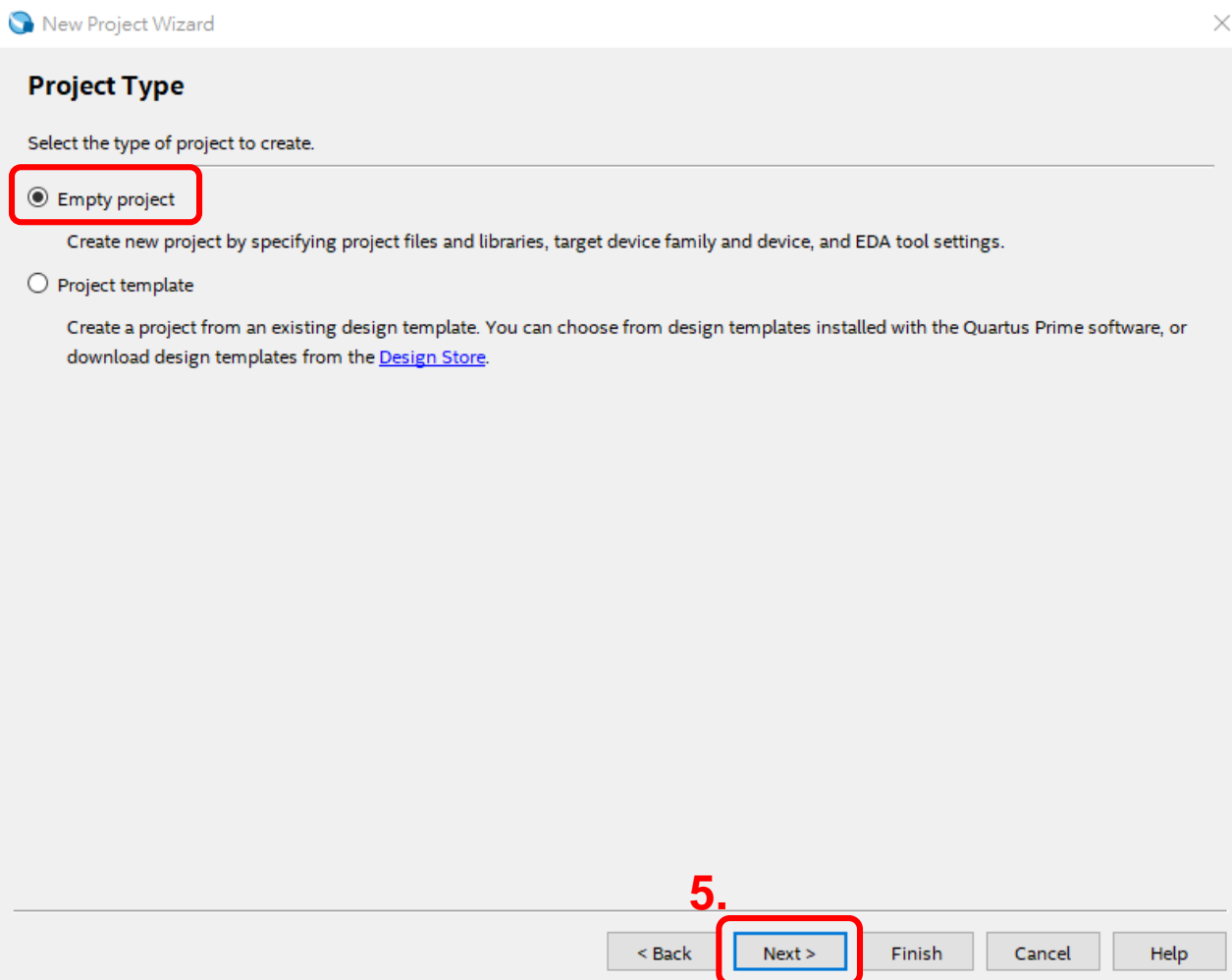


備註：也能直接點選Finish



建立新專案

選擇空白專案

4. The image shows a 'New Project Wizard' dialog box. It has a title bar with a blue icon and the text 'New Project Wizard' and a close button. The main area is titled 'Project Type' and contains the instruction 'Select the type of project to create.' There are two radio button options: 'Empty project' and 'Project template'. The 'Empty project' option is selected and highlighted with a red rectangle. Below it, there is a description: 'Create new project by specifying project files and libraries, target device family and device, and EDA tool settings.' The 'Project template' option is unselected. Below it, there is a description: 'Create a project from an existing design template. You can choose from design templates installed with the Quartus Prime software, or download design templates from the [Design Store](#).' At the bottom of the dialog, there are five buttons: '< Back', 'Next >', 'Finish', 'Cancel', and 'Help'. The 'Next >' button is highlighted with a red rectangle.

New Project Wizard

Project Type

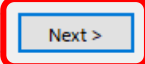
Select the type of project to create.

☒ Empty project

Create new project by specifying project files and libraries, target device family and device, and EDA tool settings.

☐ Project template

Create a project from an existing design template. You can choose from design templates installed with the Quartus Prime software, or download design templates from the [Design Store](#).

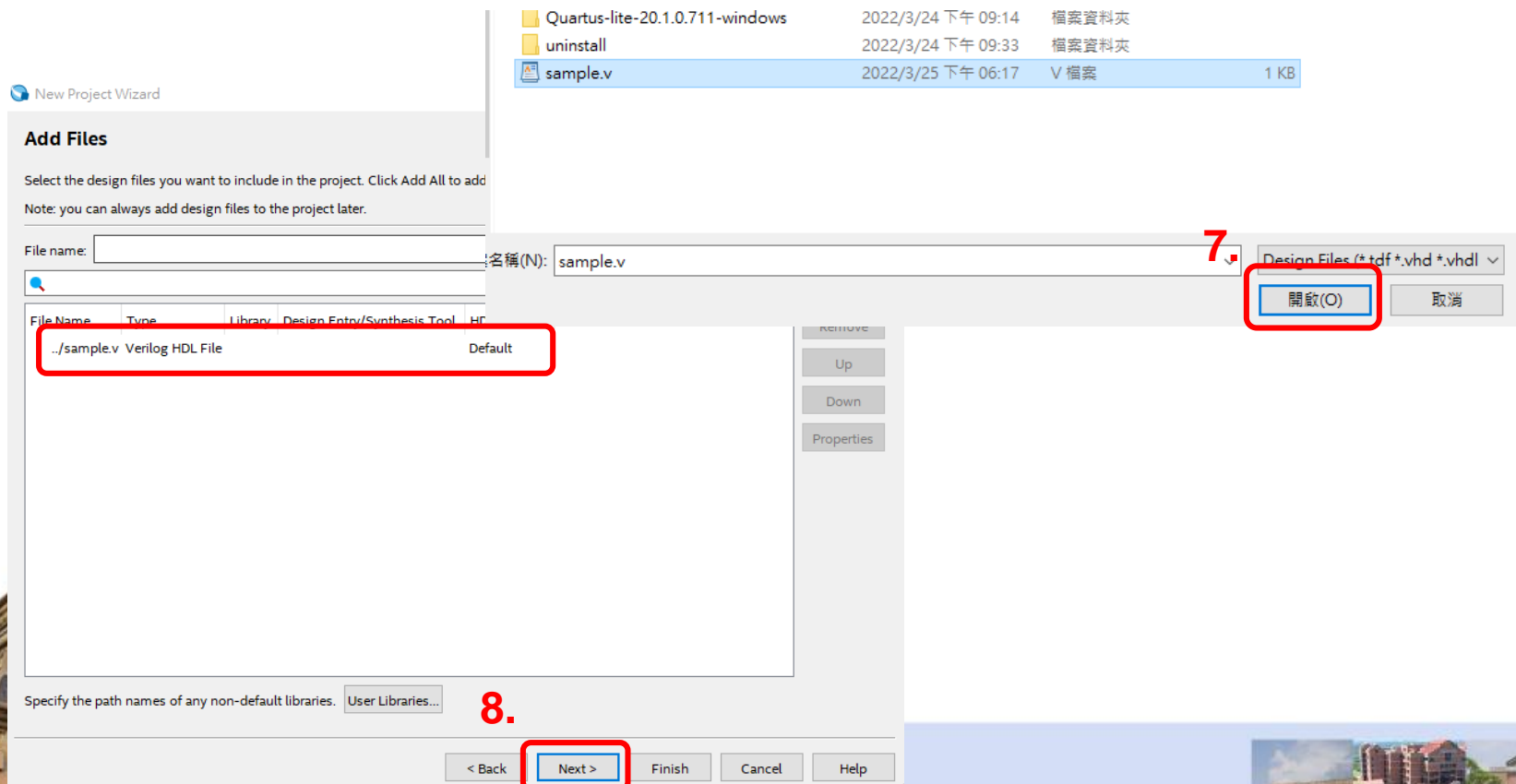
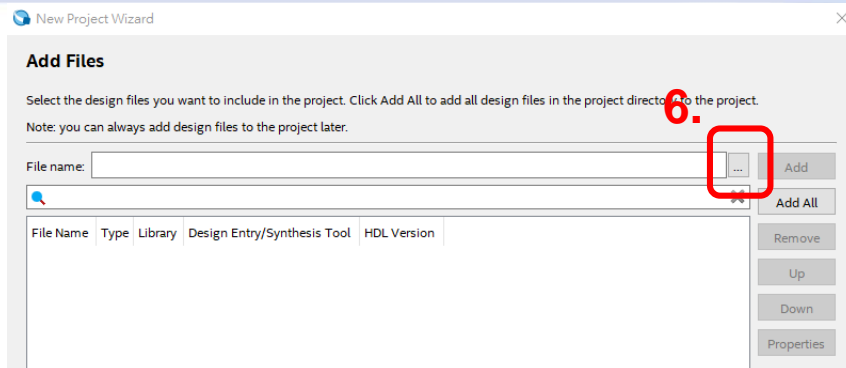
5. The image shows the 'Next >' button in the 'New Project Wizard' dialog box. The button is highlighted with a red rectangle.

< Back Next > Finish Cancel Help



建立新專案

載入sample VHDL



建立新專案

New Project Wizard

EDA Tool Settings

Specify the other EDA tools used with the Quartus Prime software to develop your project.

EDA tools:

Tool Type	Tool Name	Format(s)	Run Tool Automatically
Design Entry/Synth...	<None>	<None>	<input type="checkbox"/> Run this tool automatically to synthesize the current design
Simulation	<None>	<None>	<input type="checkbox"/> Run gate-level simulation automatically after compilation
Board-Level	Timing	<None>	
	Symbol	<None>	
	Signal Integrity	<None>	
	Boundary Scan	<None>	

7.

Help < Back **Next >** Finish Cancel

Family: MAX 10

Package: FBGA

Pin count : 484

Core Speed grade: 7

選擇 10M50DAF484C7G

Device

Device Board

Select the family and device you want to target for compilation.
You can install additional device support with the Install Devices command on the Tools menu.

To determine the version of the Quartus Prime software in which your target device is supported, refer to the [Device Support List](#) webpage.

Device family

Family: MAX 10 (DA/DF/DC/SA/SC)

Device: All

Target device

☐ Auto device selected by the Fitter

☒ Specific device selected in 'Available devices' list

☐ Other: n/a

Show in 'Available devices' list

Package: FBGA

Pin count: 484

Core speed grade: 7

Name filter:

☒ Show advanced devices

Device and Pin Options...

Available devices:

Name	Core Voltage	LEs	Total I/Os	GPIOs	Memory Bits	Embedded multiplier 9-t
10M40DCF484C7G	1.2V	40368	360	360	1290240	250
10M40DGF484I7G	1.2V	40368	360	360	1290240	250
10M50DAF484C7G	1.2V	49760	360	360	1677312	288
10M50DAF484I7G	1.2V	49760	360	360	1677312	288

8.

Migration Devices... 0 migration devices selected

9.

Buy Software OK Cancel Help



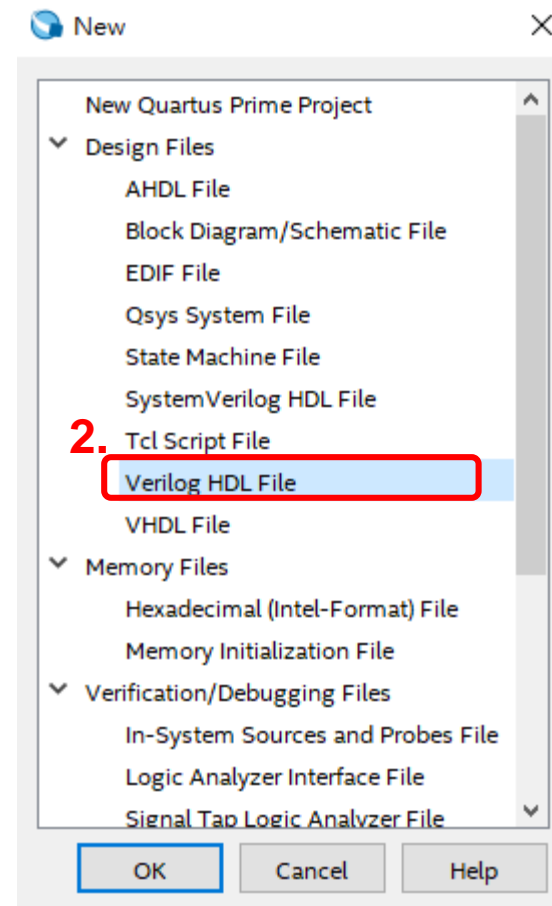
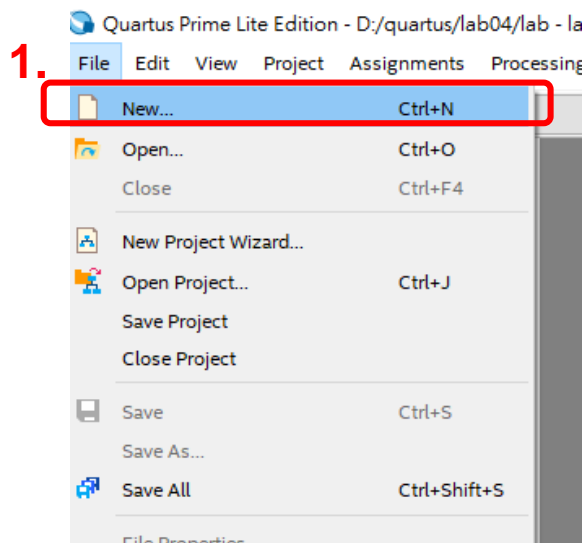
建立新設計

建立一個新設計(New Entity)

Entity有很多設計類型

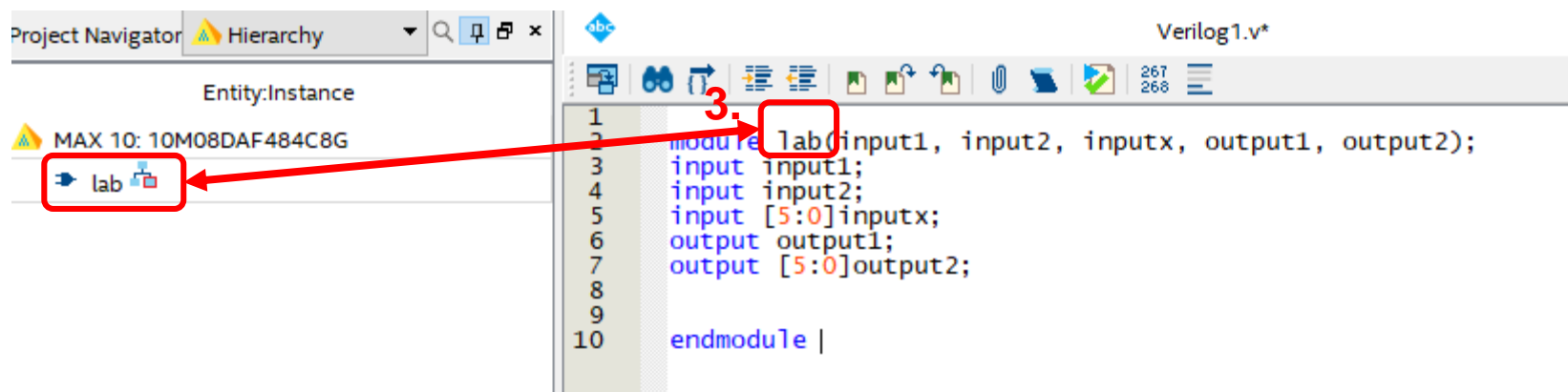
1. Verilog
2. VHDL
3. AHDL
4. Block Diagram/Schematic File
5. Etc...

這裡先以 Verilog 作為熟悉Quartus的範例。



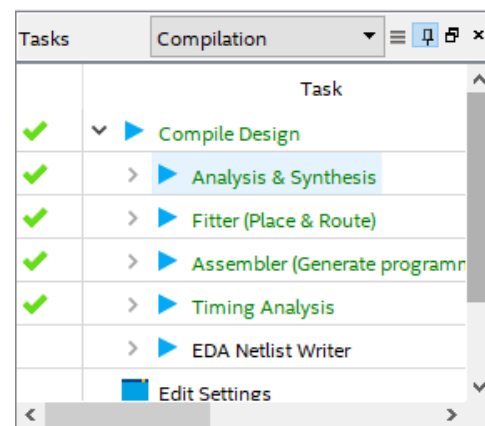
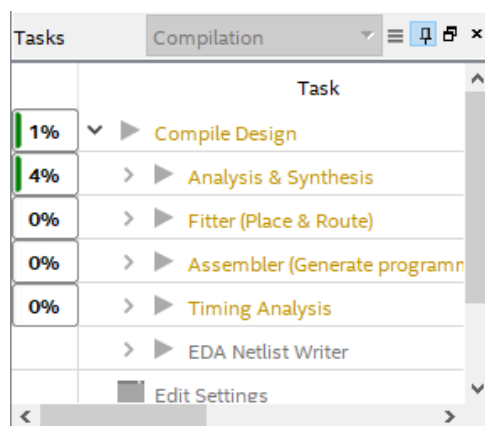
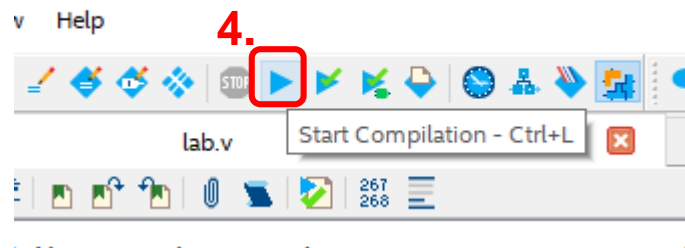
建立新設計

新設計的名稱需與top module名稱一致



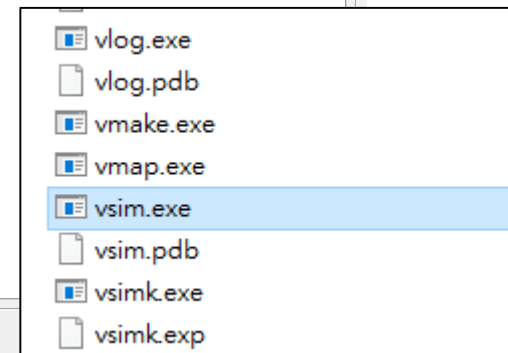
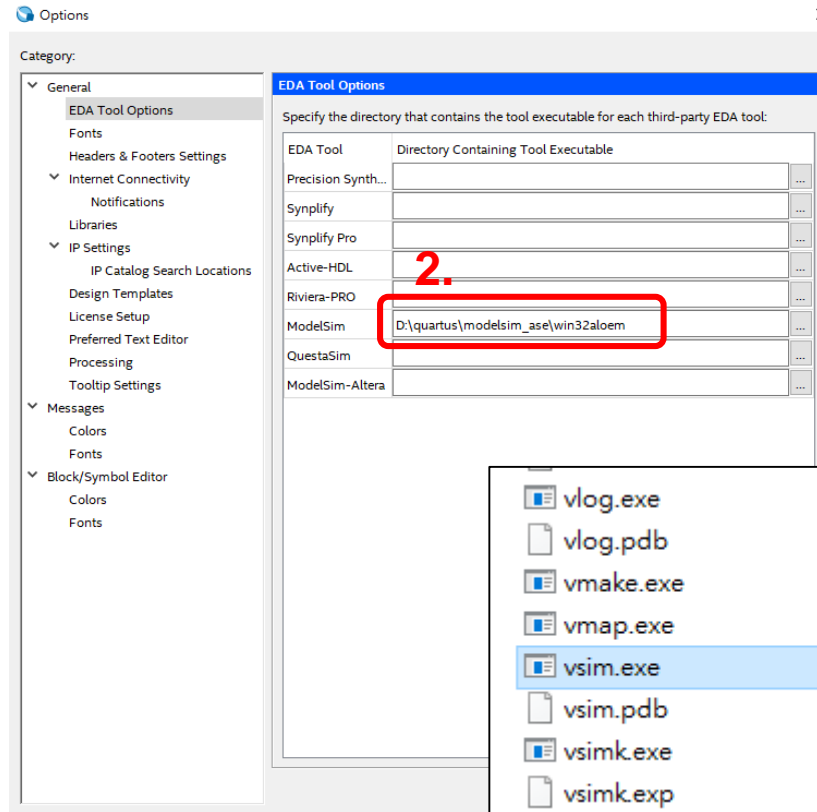
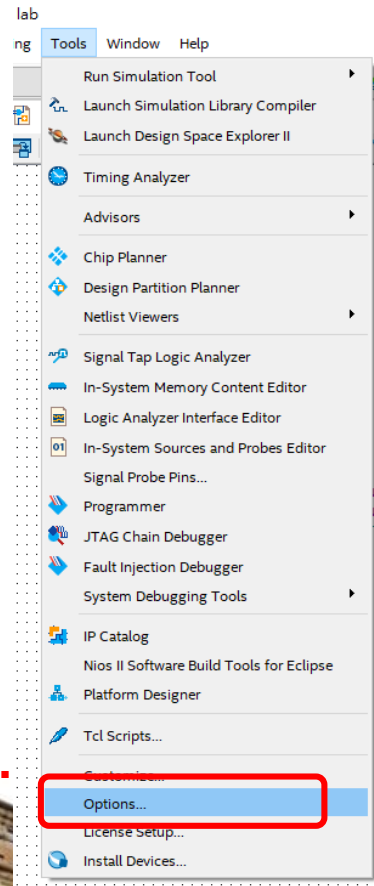
建立新設計

合成編譯電路



電路模擬設定

在Tools內選擇Options，並在EDA Tool Options設定ModelSim路徑

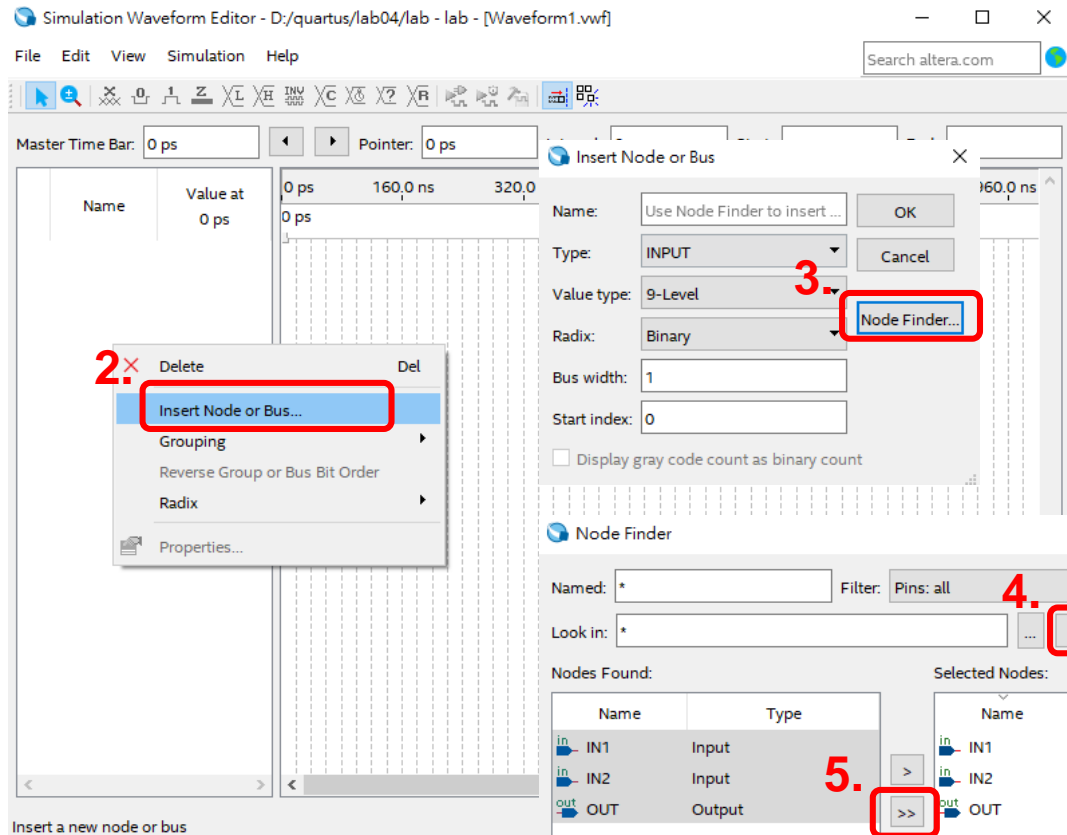
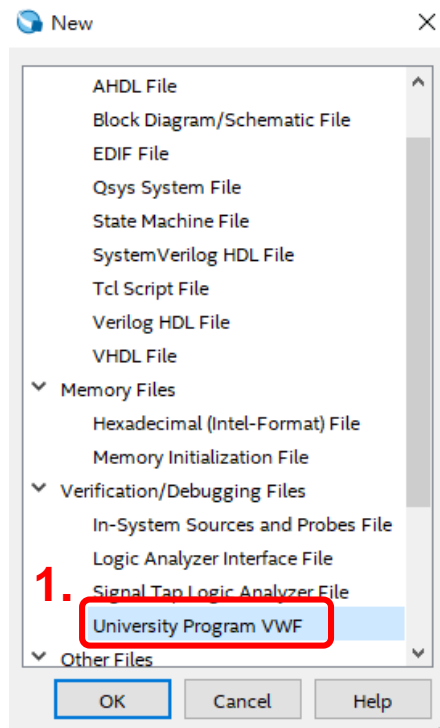


備註：選擇含有vsim.exe的資料夾，通常是aloem結尾



電路模擬

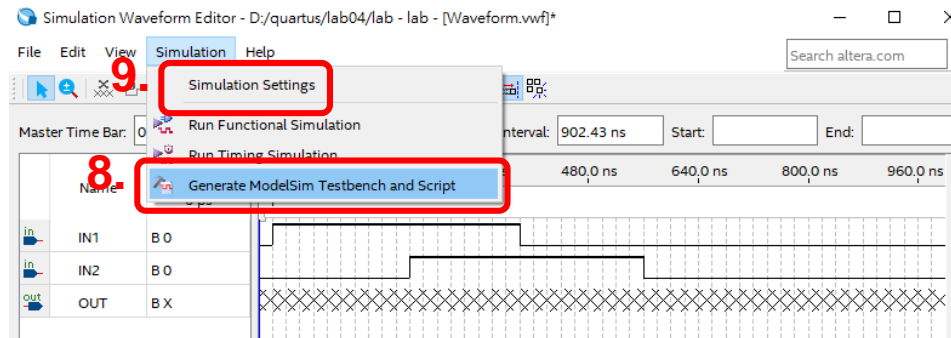
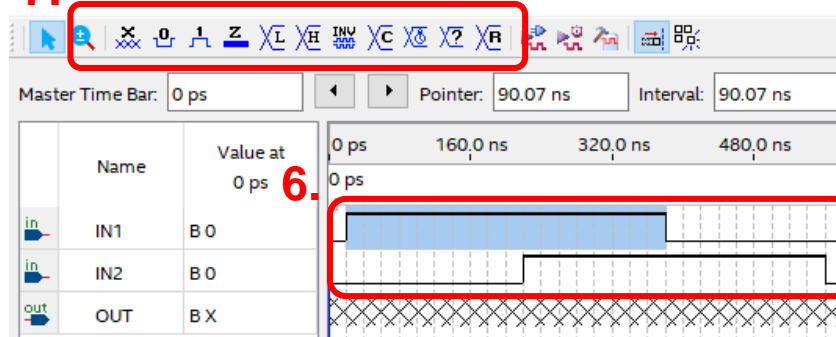
新增波形檔案，並指定顯示的輸入輸出



電路模擬

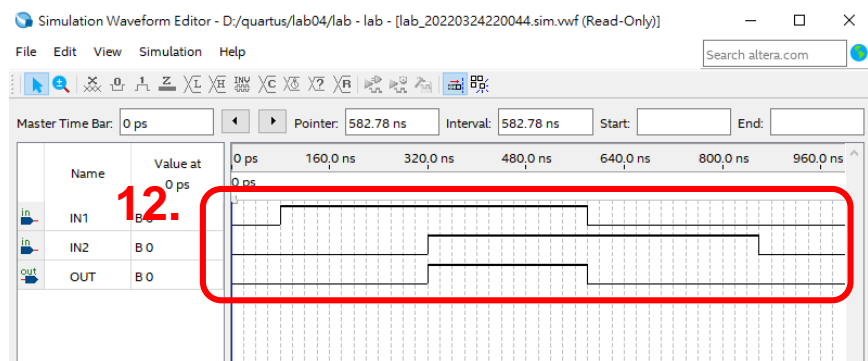
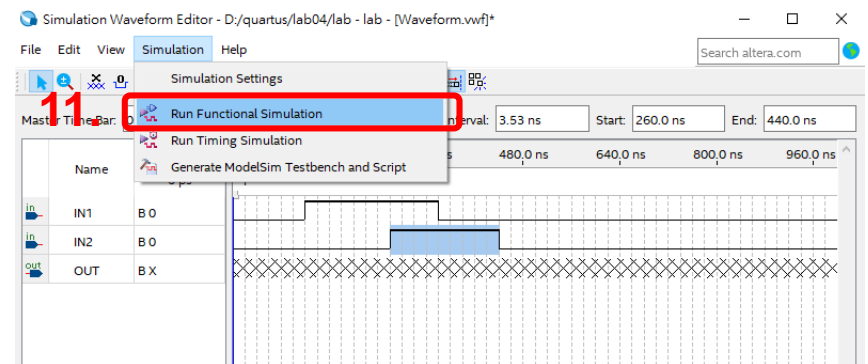
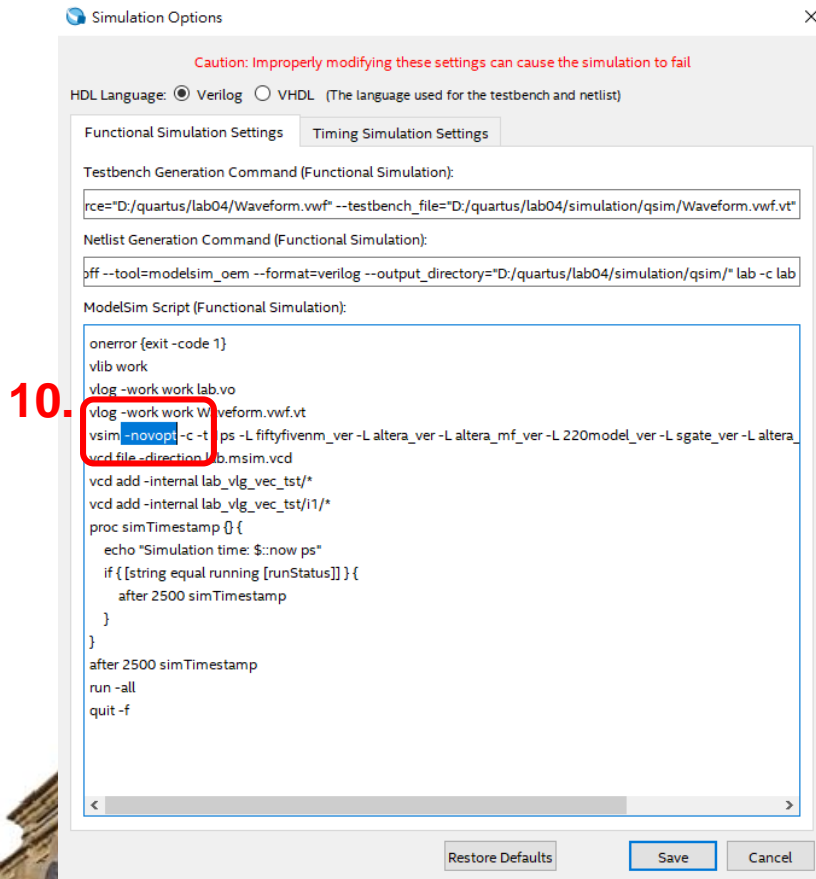
反白選取線段，並設定輸入值再產生測試檔

7.



電路模擬

因版本問題，需將Setting中的-novopt刪除，即可開始模擬

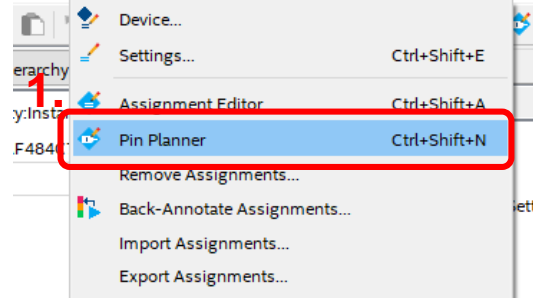


FPGA燒錄

對輸入/輸出指定腳位

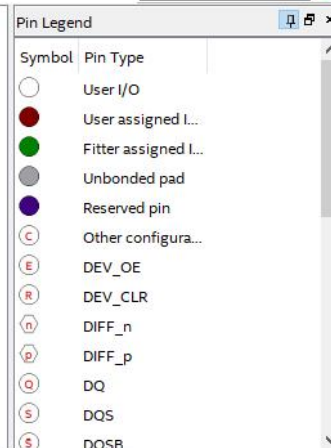
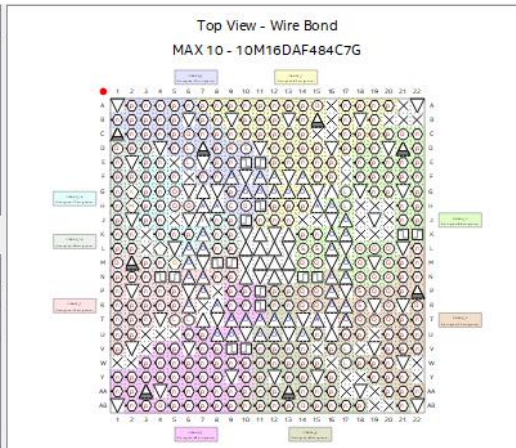
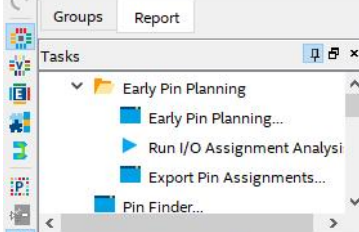
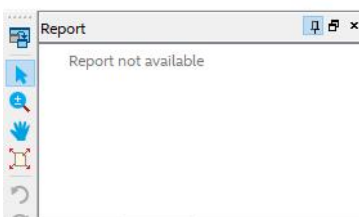
Edition - D:/quartus/lab04/lab - lab

project Assignments Processing Tools Window Help



Pin Planner - D:/quartus/lab04/lab - lab

File Edit View Processing Tools Window Help



Named:	*	Edit:						Filter: Pins: all
Node Name	Direction	Location	I/O Bank	VREF Group	I/O Standard	Reserved	Current Strength	Slew
IN1	Input				2.5 V (default)		12mA (default)	
IN2	Input				2.5 V (default)		12mA (default)	
OUT	Output				2.5 V (default)		12mA (default)	2 (default)
<<new node>>								

FPGA燒錄

參考A1與A2的User Manual文件，選擇Switch為輸入與LED作為輸出，將對應的FPGA IO編號輸入，並重新編譯。

Pin Planner - D:/quartus/lab4 - lab4

File Edit View Processing Tools Window Help

Search Intel FPGA

Report

Report not available

Groups Report

Tasks

Early Pin Planning

Early Pin Planning...

Named: * Edit: X 2. <<new node>>

Filter: Pins: all

Node Name	Direction	Location	I/O Bank	VREF Group	Fitter Location	I/O Standard	Reserved	Curr
IN1	Input	PIN_C10	7	B7_N0	PIN_AB4	2.5 V (default)		
IN2	Input	PIN_C11	7	B7_N0	PIN_AA3	2.5 V (default)		
OUT	Output	PIN_A8	7	B7_N0	PIN_W8	2.5 V (default)		
<<new node>>								

Table 3-4 Pin Assignment of

Signal Name	FPGA Pin No
SW0	PIN_C10
SW1	PIN_C11
SW2	PIN_D12
SW3	PIN_C12
SW4	PIN_A12
SW5	PIN_B12
SW6	PIN_A13
SW7	PIN_A14
SW8	PIN_B14
SW9	PIN_F15

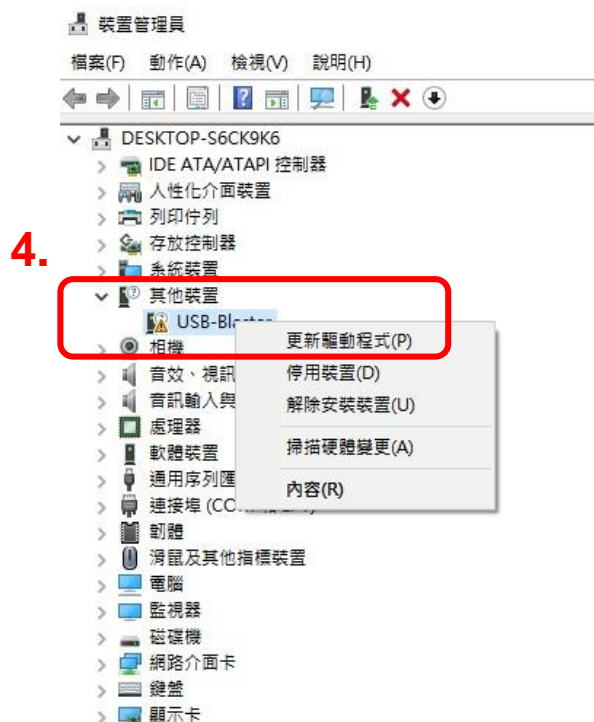
Help

3.

lab.v Start Compilation - Ctrl+L

FPGA燒錄

呼叫裝置管理員後，在未辨識的USB-Blaster右鍵，選取更新驅動程式



← 更新驅動程式 - USB-Blaster

您要如何搜尋驅動程式？

→ 自動搜尋驅動程式

Windows 會在您的電腦中搜尋最佳可用的驅動程式，並安裝到您的裝置上。(&S)

5.

→ 瀏覽電腦上的驅動程式

手動尋找並安裝驅動程式 (&R)。



FPGA燒錄

選擇從Ecourse2下載的USB-Blaster驅動程式解壓縮後的路徑，並完成安裝

6.

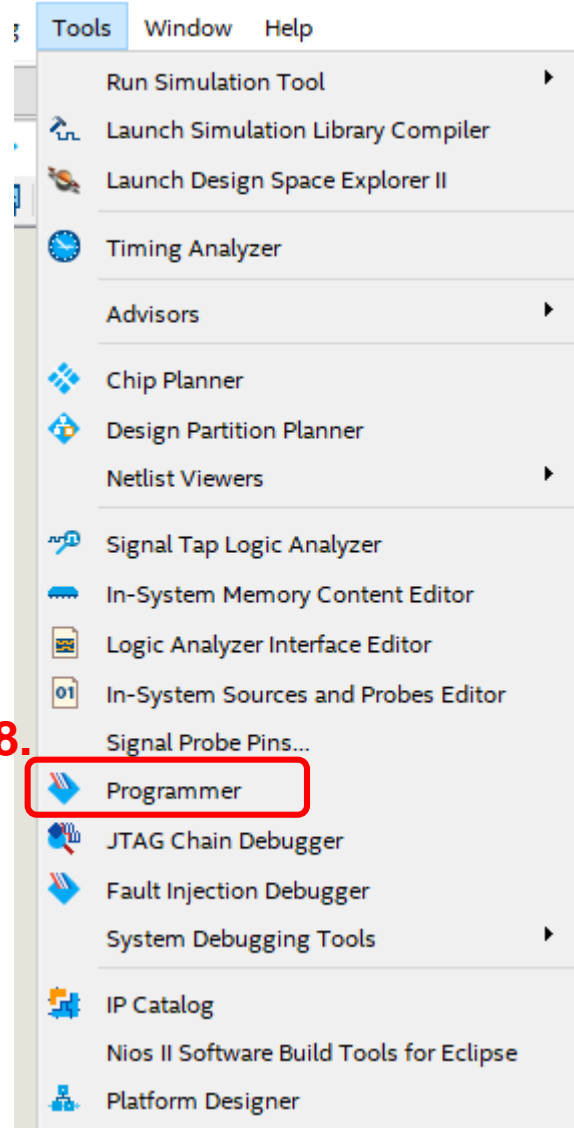


7.



FPGA燒錄

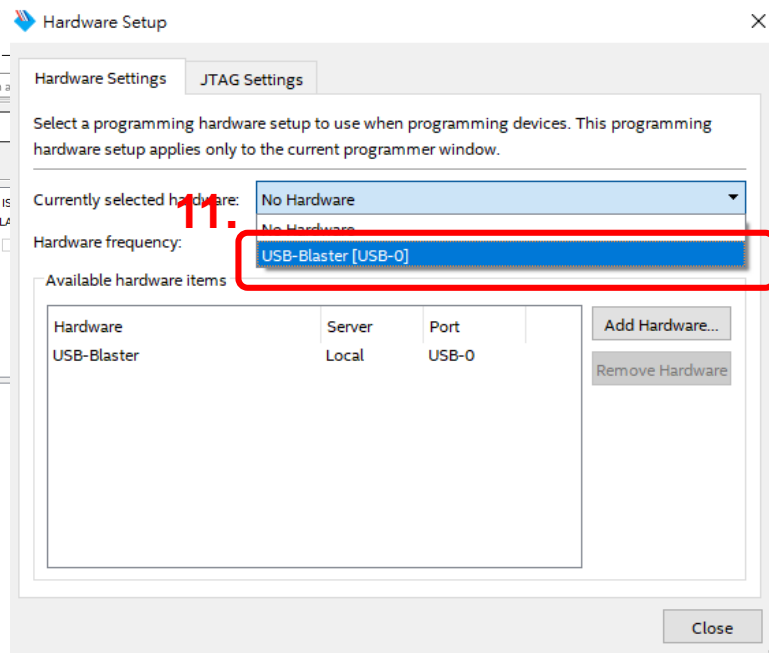
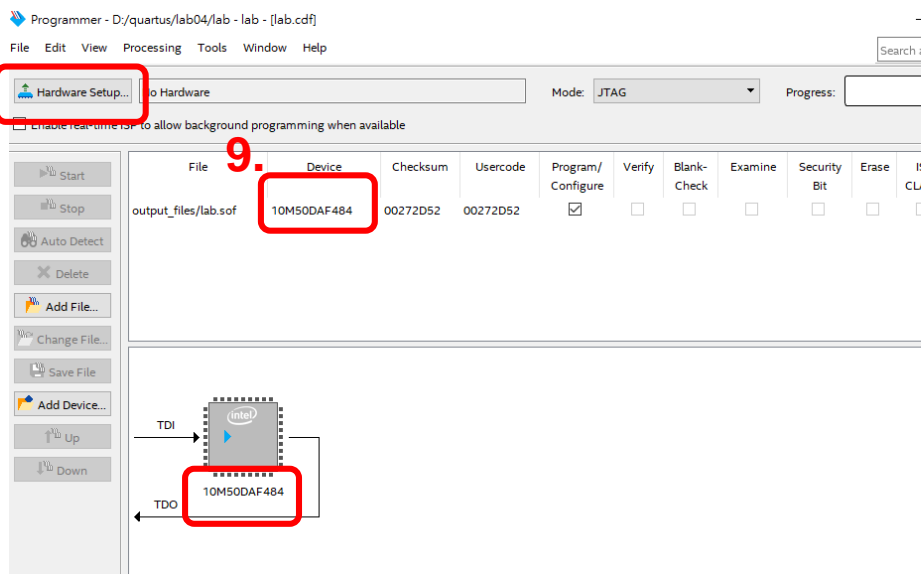
完成安裝後，開啟燒錄頁面



FPGA燒錄

先確認選到正確的板子後，選取USB驅動程式

10.



FPGA燒錄

選取完後即可直接燒錄

12.

