


數位系統導論實驗 LAB 4

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Verilog HDL 介紹

- Verilog 是一種 HDL 硬體描述語言 (Hardware Description Language)。
  HDL 在數位系統設計中已經成為設計方法的主流，基於 HDL 數位系統設計的最大優勢在於 designer 可以將精力放在電路功能的實現上，而不需處理電路構造，因此可以提高設計效率

- Verilog 可縮短數位系統開發時間，模擬電路時序圖並逐步修正電路功能

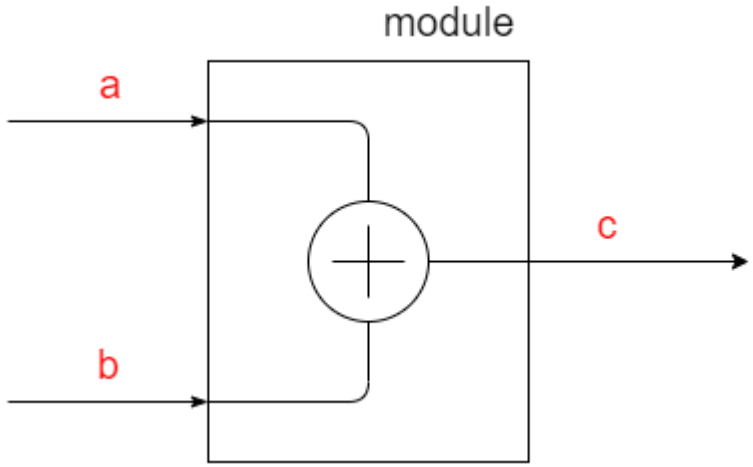
目的

- 瞭解 Verilog 的應用
- Verilog 描述電路的方法
- 如何用 Verilog 設計硬體

Basic unit - module

- module 是實現某個特定功能的 verilog code block
- A module should be enclosed within module and endmodule keywords.
  module name 寫在 module keyword 的右方，並在 ( ) 內宣告 I/O ports
  下圖是一個實現加法器 module 的例子：

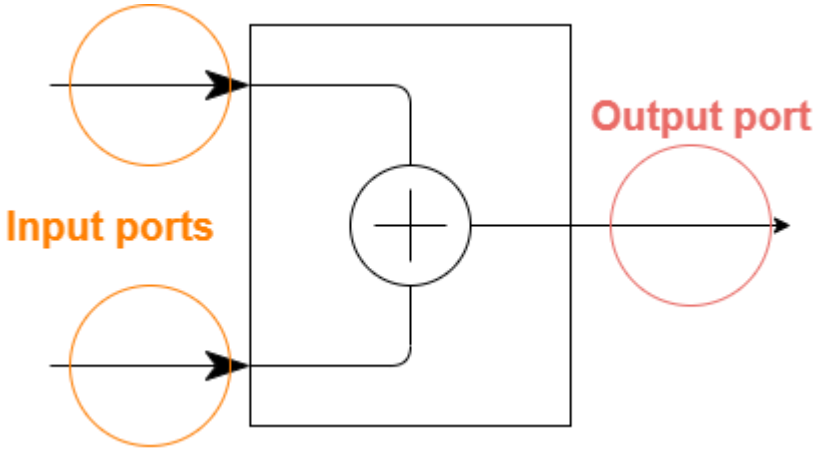
```
1
2   module add (                                          module
3
4   // Ports_list                                         ports
5       a,
6       b,
7       c
8   );
9   //-------Input ports-------
10  input    [3:0]   a          ;
11  input    [3:0]   b          ;
12  //-------Output ports-------
13  output   [4:0]   c          ;
14  //-----declare net types-----
15  wire             a          ;
16  wire             b          ;
17  wire             c          ;
18
19  //----statements----(with Continuous assignment)
20  assign c = a + b ;                                    statements
21
22  endmodule
23
```



I/O Ports

```
input  [<MSB> : <LSB>]  a  ;
input  [<MSB> : <LSB>]  b  ;
output [<MSB> : <LSB>]  c  ;
```

```
9   //-------Input ports-------
10  input    [3:0]   a          ;
11  input    [3:0]   b          ;
12  //-------Output ports-------
13  output   [4:0]   c          ;
```



MSB: most significant bit LSB: least significant bit

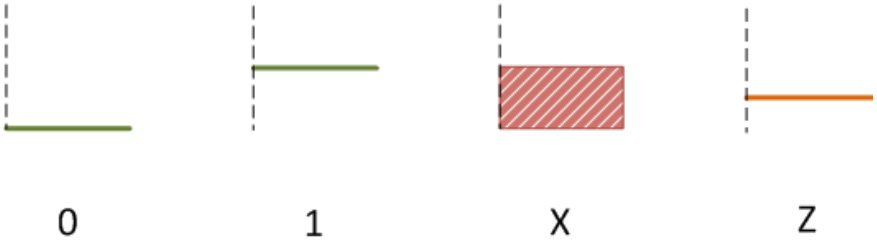
Port	Description
Input	The design module can only receive values from outside using its input ports
Output	The design module can only send values to the outside using its output ports
Inout	The design module can either send or receive values using its inout ports

Data types (1/2)

- **variables 只具有以下四種狀態**

0	represents a logic zero, or a false condition
1	represents a logic one, or a true condition
x	represents an unknown logic value // can be 1 or 0, where it means " don't care "
z	represents a high-impedance state

下圖是如何在時序圖和 simulation 的波形中表示這些值
大部分 simulation tool 皆是如此，其中紅色代表任意值，橙色代表高阻抗



Data types (2/2)

- **Declaration syntax:**

  <data_type> <port name> ;

- **data_type:**
  - wire: represent physical connections between devices. **(If it is not drived, default value = z)**
  - reg: represent abstract data storage element. **(default value = x)**

```
 9  //-------Input ports-------
10  input    [3:0]   a          ;
11  input    [3:0]   b          ;
12  //-------Output ports-------
13  output   [4:0]   c          ;
14  //-----declare net types-----
15  wire             a          ;
16  wire             b          ;
17  wire             c          ;
18
```

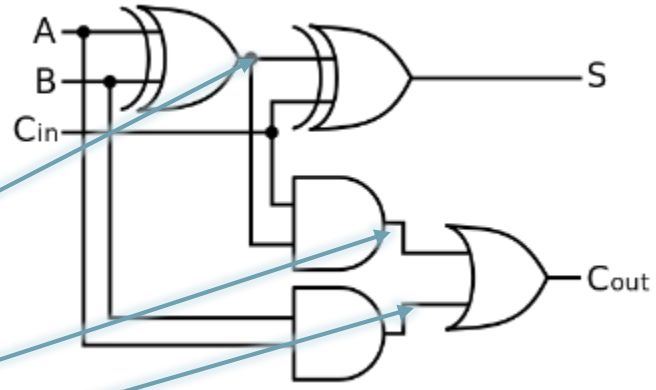
Gate level assign

```
module LAB(inputA, inputB, outputY);
//-------Input ports-------
input  A;
input  B;
//-------Output ports-------
output outputY;
//-----component assignment-----
AND2X1   x0(.A(inputA), .B(inputB), .Y(outputY));
endmodule


AND2X1   x0(inputA, inputB, outputY);
```

```
module AND2X1(A, B, Y);
input A, B;
output Y;
assign Y= A & B;
endmodule
```

Verilog example

```
module FA(A, B, Cin, S, Cout);
//-------Input ports-------
input  A;
input  B;
input  Cin;
//-------Output ports------
output S;
output Cout;
//-----declare net types-----
wire    AxorB, AxorBandCin, AandB;
//-----component assignment-----
XOR2X1  x0(.A(A), .B(B), .Y(AxorB));
XOR2X1  x1(.A(AxorB), .B(Cin), .Y(S));
AND2X1  x2(.A(AxorB), .B(Cin), .Y(AxorBandCin));
AND2X1  x3(.A(A), .B(B), .Y(AandB));
OR2X1   x4(.A(AandB), .B(AxorBandCin), .Y(Cout));

endmodule
```



Sample.v

NAND2X1

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

AND2X1

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

OR2X1

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

NOR2X1

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

XOR2X1

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

INVX1

A	Y
0	1
1	0
0	1
1	0

LAB

- 實驗一：A[3:0] - B[3:0] 的 4 bit 減法器運算

  A、B為unsigned，輸出為signed Y[4:0]

  並於波型檔完整顯示

A = 3

[3]	[2]	[1]	[0]
0	0	1	1

−

B = 5

[3]	[2]	[1]	[0]
0	1	0	1

=

Y = - 2

[4]	[3]	[2]	[1]	[0]
1	1	1	1	0

A = 3

[3]	[2]	[1]	[0]
0	0	1	1

−

B = 1

[3]	[2]	[1]	[0]
0	0	0	1

=

Y = 2

[4]	[3]	[2]	[1]	[0]
0	0	0	1	0

A = 3

[3]	[2]	[1]	[0]
0	0	1	1

−

B = 15

[3]	[2]	[1]	[0]
1	1	1	1

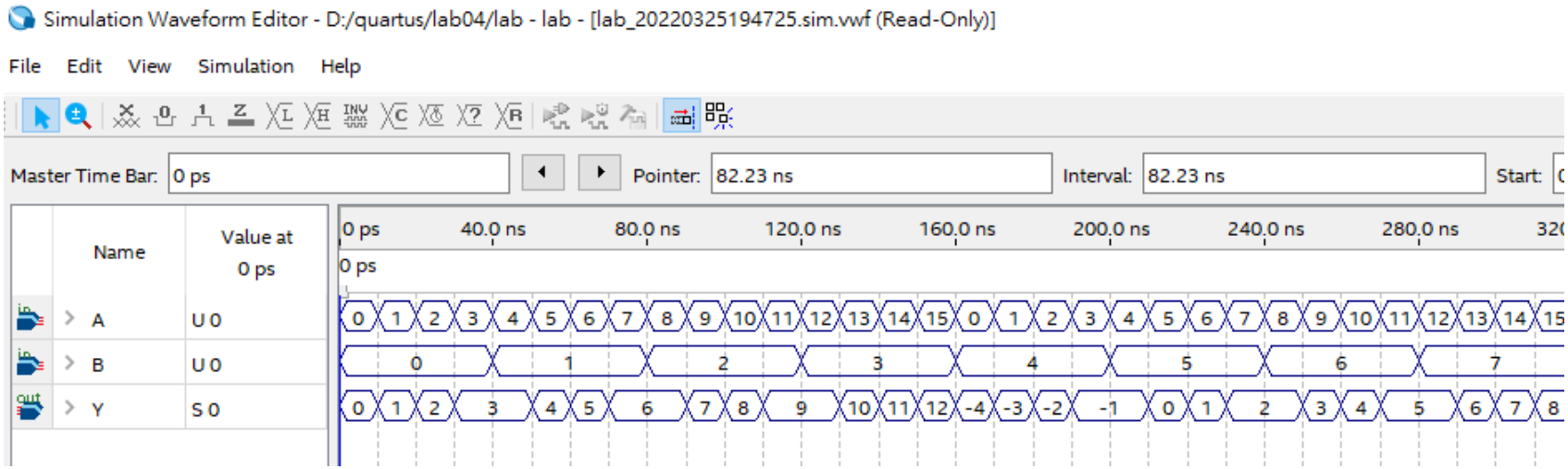
=

Y = - 12

[4]	[3]	[2]	[1]	[0]
1	0	1	0	0

LAB

範例波形檔


Simulation Waveform Editor - D:/quartus/lab04/lab - lab - [lab_20220325194725.sim.vwf (Read-Only)]
File Edit View Simulation Help
Master Time Bar: 0 ps
Pointer: 82.23 ns
Interval: 82.23 ns
Start:
Name
Value at 0 ps
A U 0
B U 0
Y S 0
0 ps 40.0 ns 80.0 ns 120.0 ns 160.0 ns 200.0 ns 240.0 ns 280.0 ns

REPORT OF LAB 4 (4%)

The report should include …

1. 請截圖輸出波形，波形和真值表是否一致？
2. 請簡述程式實作過程、遇到的困難及解決方法。
3. Discussion and experience (Everyone)
   (所有人的心得與討論)

- File type: pdf
- File name: Lab4_(Number of team)_report
- Deadline: 2022/04/13 24:00