數位系統導論 2021/4/7 作業

(不用繳交，4/14 隨堂抽考)

For each of the following digital designs, please

(a) Construct its truth table;

(b) Show the minterm & maxterm expansions respectively;

(c) Show the equations of the simplified SoP & PoS respectively;

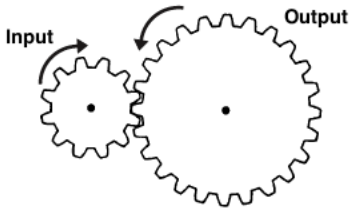
(d) Draw the simplified 2-level full-NAND and full NOR implementations respectively.

1. A design that outputs logic "1" iff the corresponding decimal of its 4-bit binary input $\{x_3\, x_2\, x_1\, x_0\}$ is prime

2. A design that outputs logic "1" iff the corresponding decimal of its 4-bit binary input $\{x_3\, x_2\, x_1\, x_0\}$ is a Fibonacci number

3. A design that converts a 4-bit binary number to its Gray code

4. A design that derives the output gear count from a 4-bit counter for the input gear (the ratio of two gears is 5:1)



5. A design that sums up its 4 binary inputs *a*, *b*, *c*, and *d* (i.e., $\{y_2\, y_1\, y_0\} = a+b+c+d$)

6. A design that multiplies its two 2-bit inputs (both the inputs and output are signed numbers with the 2's complement representation)