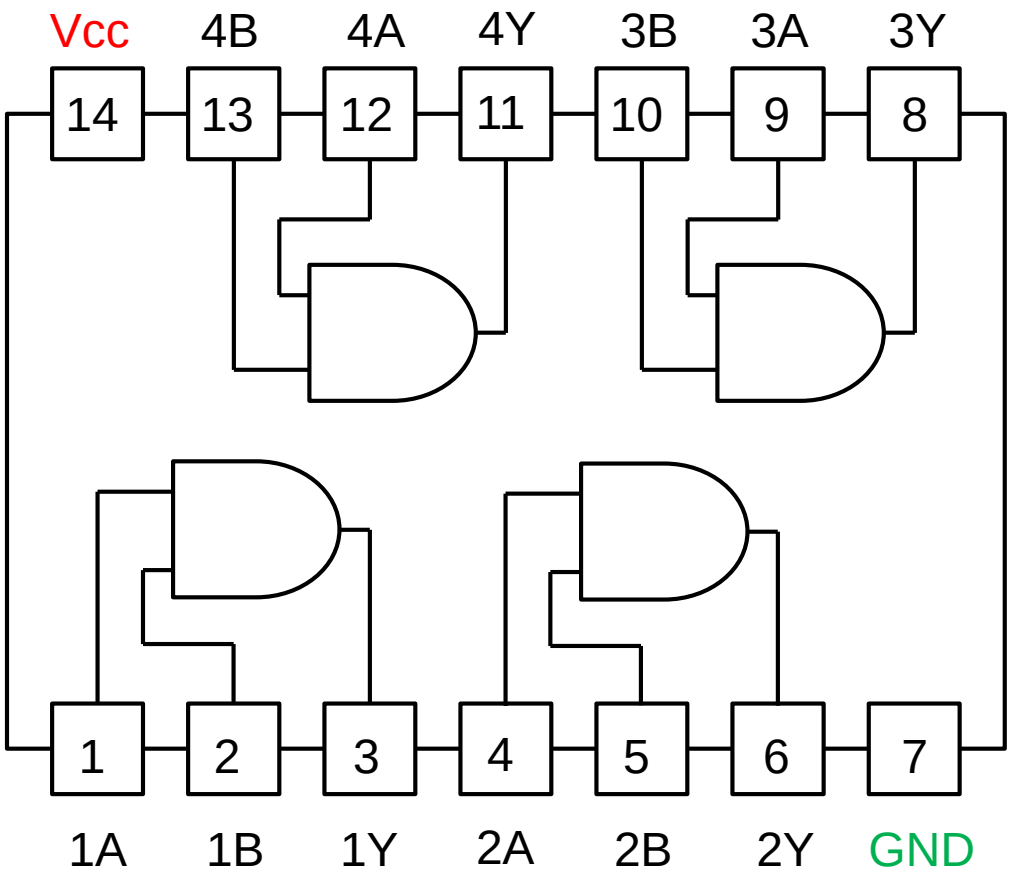
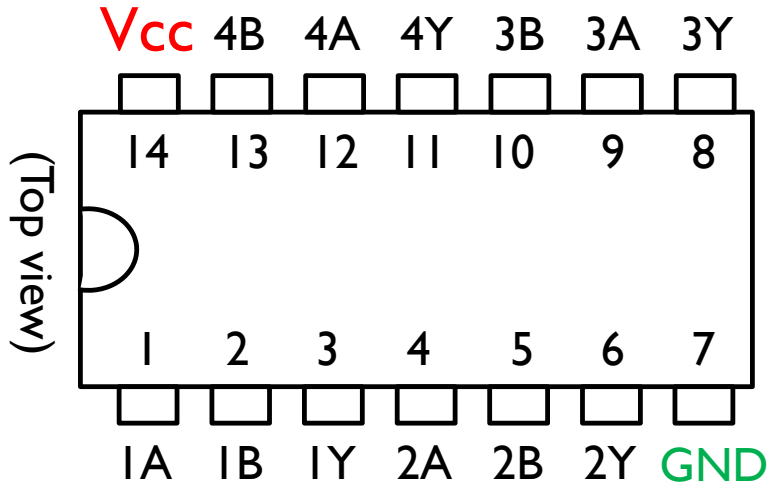
數位系統導論實驗 LAB 1

梁郁珮

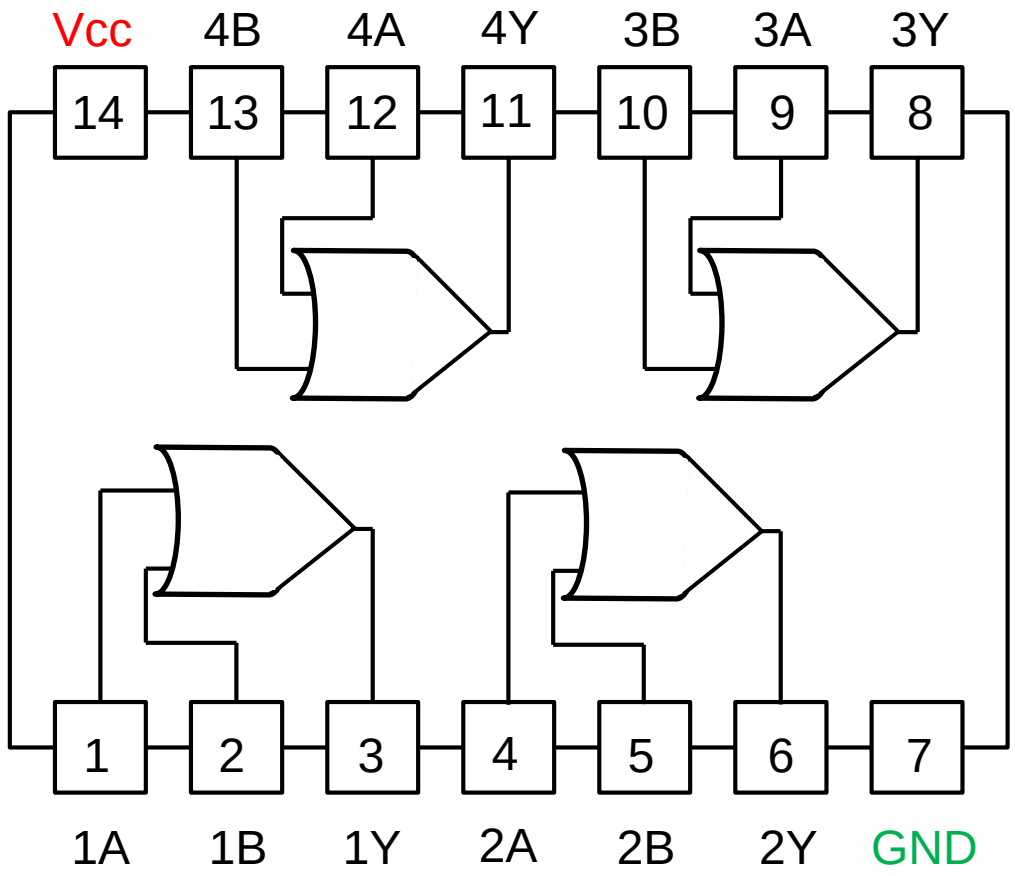
IC介紹(74LS08) 4＊TWO-INPUT AND GATE

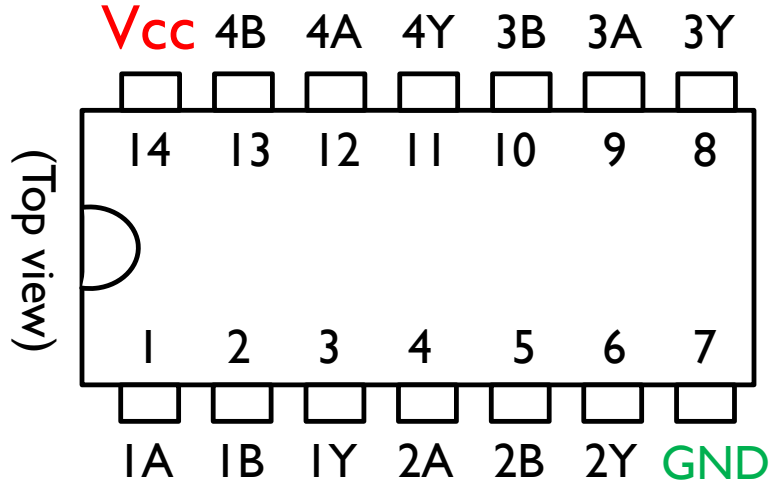




- 7及14接腳：接地及電源
- 1與2；4與5；9與10；12與13接腳：輸入腳位
- 3；6；8；11接腳：輸出腳位

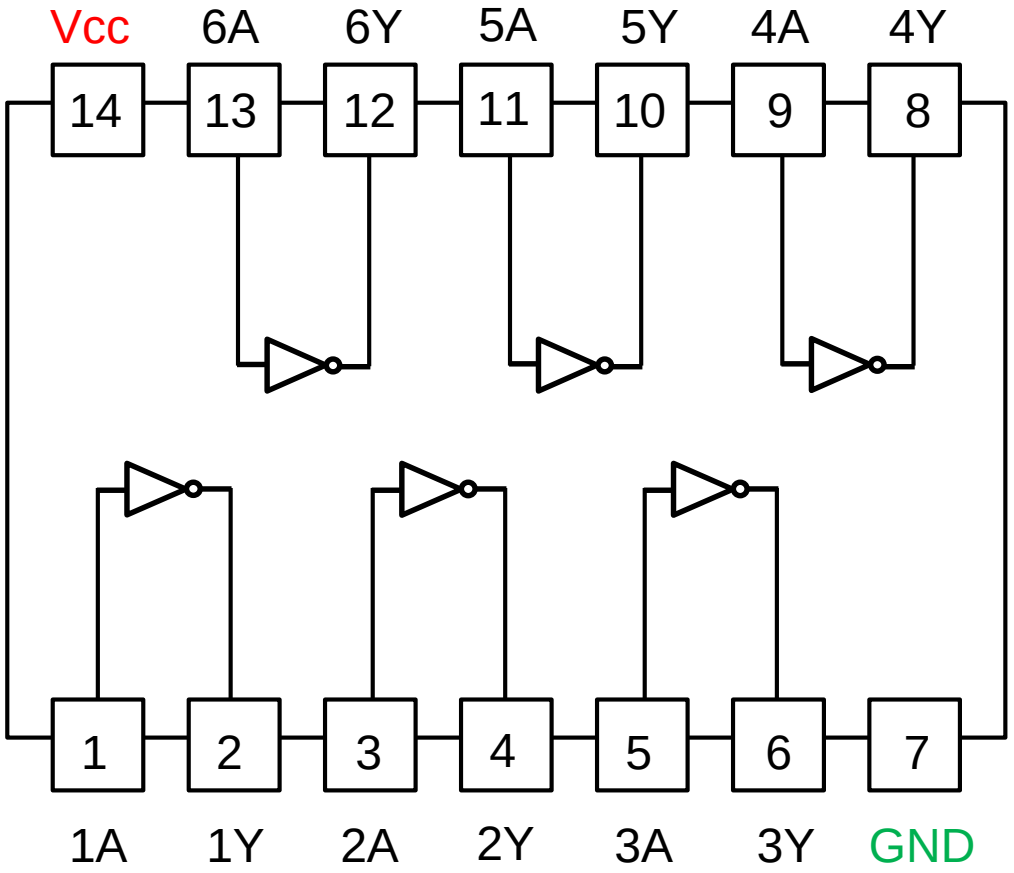
IC介紹(74LS32) 4＊TWO-INPUT OR GATE

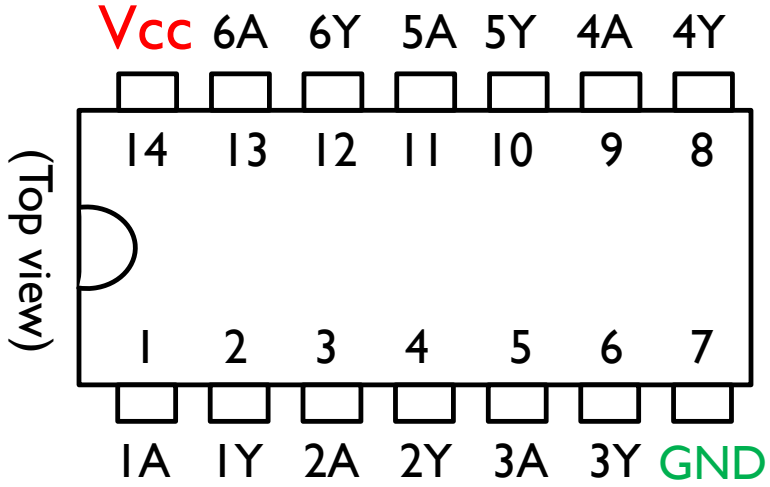




- 7及14接腳：接地及電源
- 1與2；4與5；9與10；12與13接腳：輸入腳位
- 3；6；8；11接腳：輸出腳位

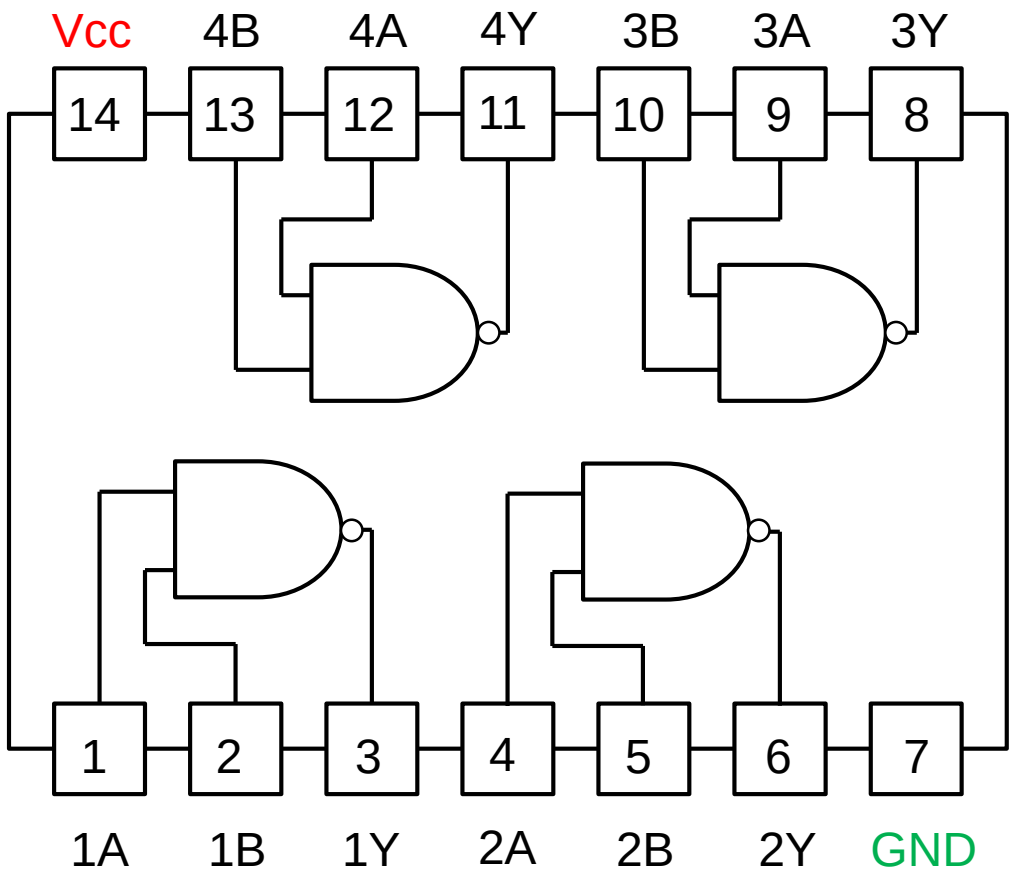
IC介紹(74LS04) 6 * NOT GATE

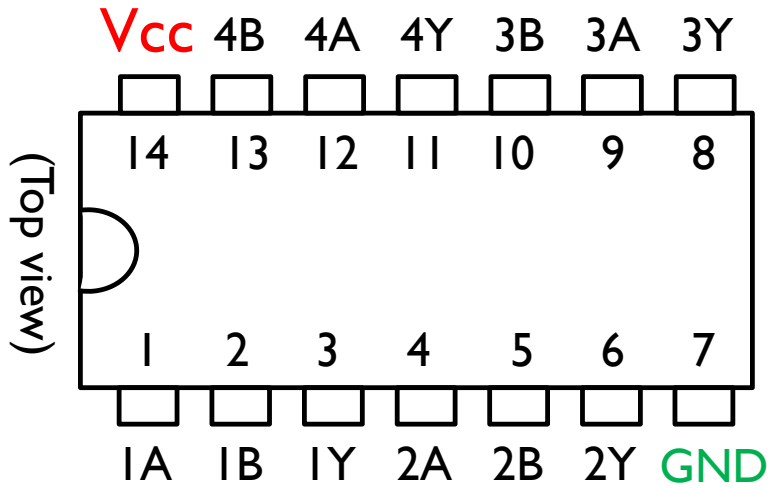




- 7及14接腳：接地及電源
- 1；3；5；9；11；13 接腳：輸入腳位
- 2；4；6；8；10；12 接腳：輸出腳位

IC介紹(74LS00) 4＊TWO-INPUT NAND GATE

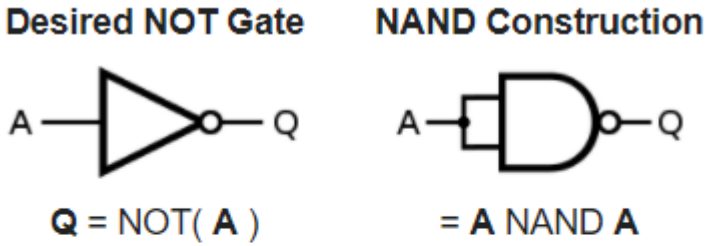




- 7及14接腳：接地及電源
- 1與2；4與5；9與10；12與13接腳：輸入腳位
- 3；6；8；11接腳：輸出腳位

通用閘 NAND/NOR

- NAND to NOT
  - A NOT gate is made by joining the inputs of a NAND gate together. Since a NAND gate is equivalent to an AND gate followed by a NOT gate, joining the inputs of a NAND gate leaves only the NOT gate.
  - (A · A) ' = A'



Truth Table

Input A	Output Q
0	1
1	0

https://en.wikipedia.org/wiki/NAND_logic

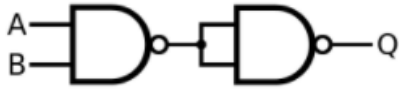
通用閘 NAND/NOR

- NAND to AND
  - An AND gate is made by inverting the output of a NAND gate as shown below.
  - A and B = not (A nand B)

Desired AND Gate

Q = A AND B

NAND Construction



= (**A** NAND **B**) NAND (**A** NAND **B**)

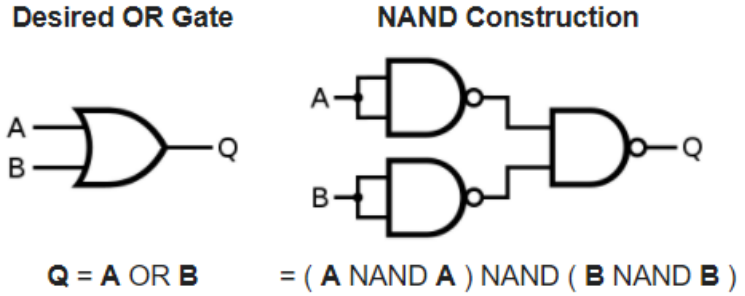
Truth Table

Input A	Input B	Output Q
0	0	0
0	1	0
1	0	0
1	1	1

https://en.wikipedia.org/wiki/NAND_logic

通用閘 NAND/NOR

- NAND to OR
- If the truth table for a NAND gate is examined or by applying De Morgan's Laws, it can be seen that if any of the inputs are 0, then the output will be 1. To be an OR gate, however, the output must be 1 if any input is 1. Therefore, if the inputs are inverted, any high input will trigger a high output.
- (A + B) = (A'B')' (DeMorgan's Law)



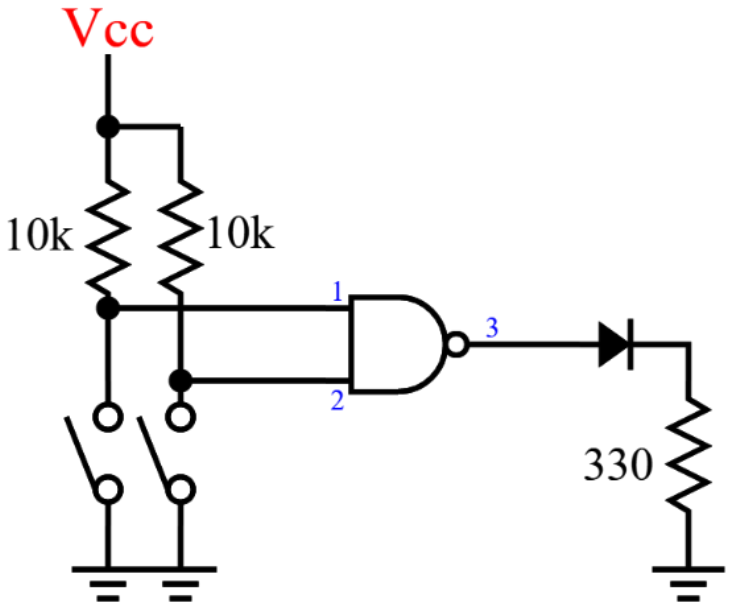
Truth Table

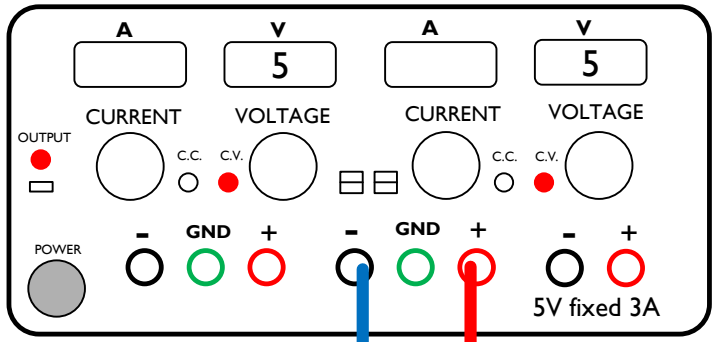
Input A	Input B	Output Q
0	0	0
0	1	1
1	0	1
1	1	1

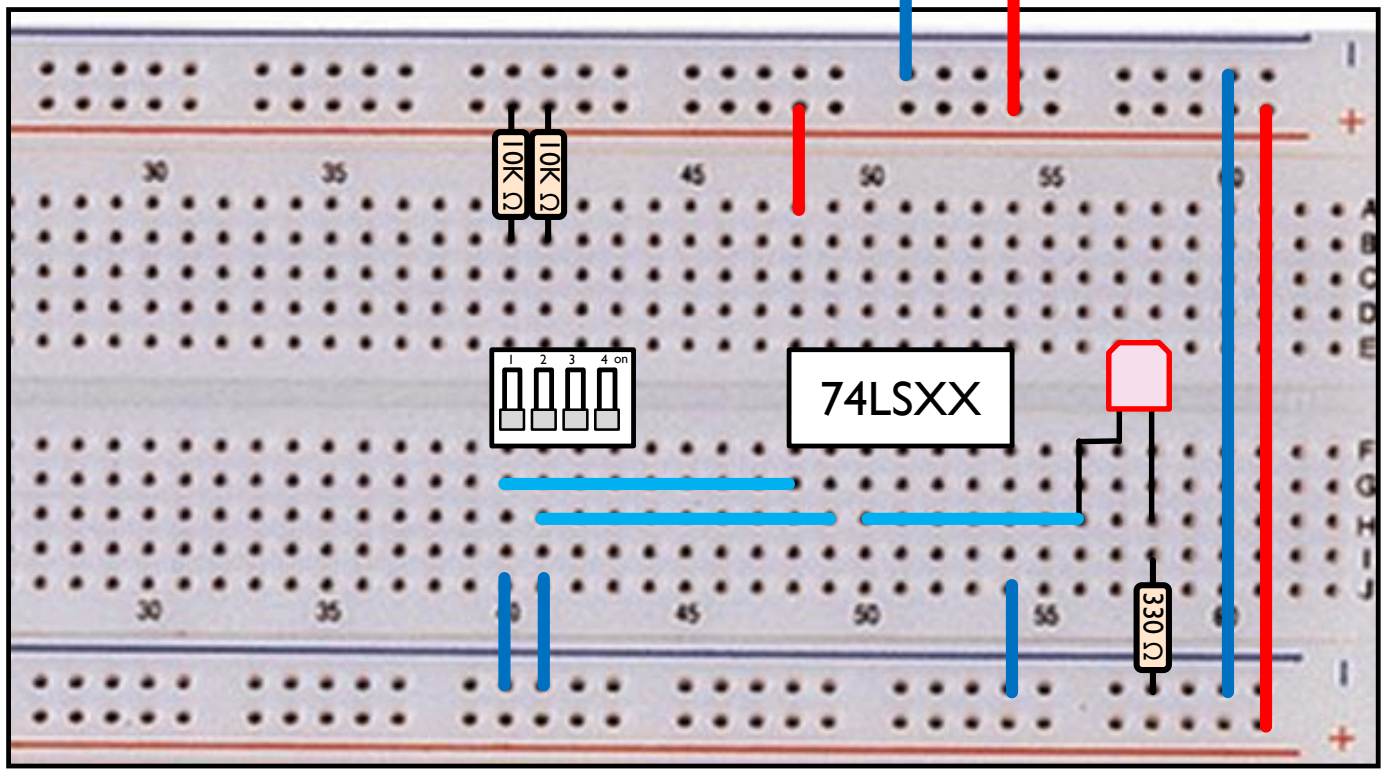
https://en.wikipedia.org/wiki/NAND_logic

- # Lab 1-1 Verify the basic logic ic

1. Please verify the basic logic ic 74LS08 (AND), 74LS32(OR), 74LS00(NAND) with the following circuit
2. Please change the circuit to verify the NOT gate (74LS04)

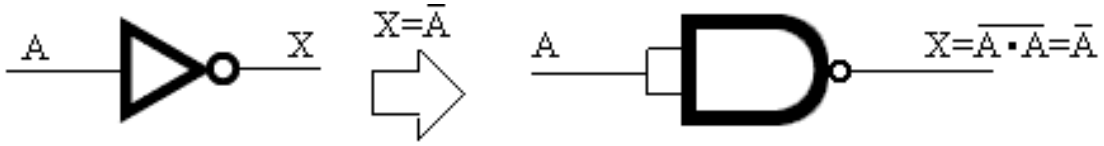


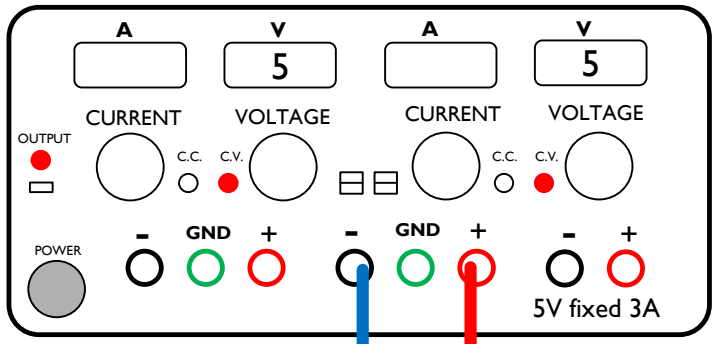




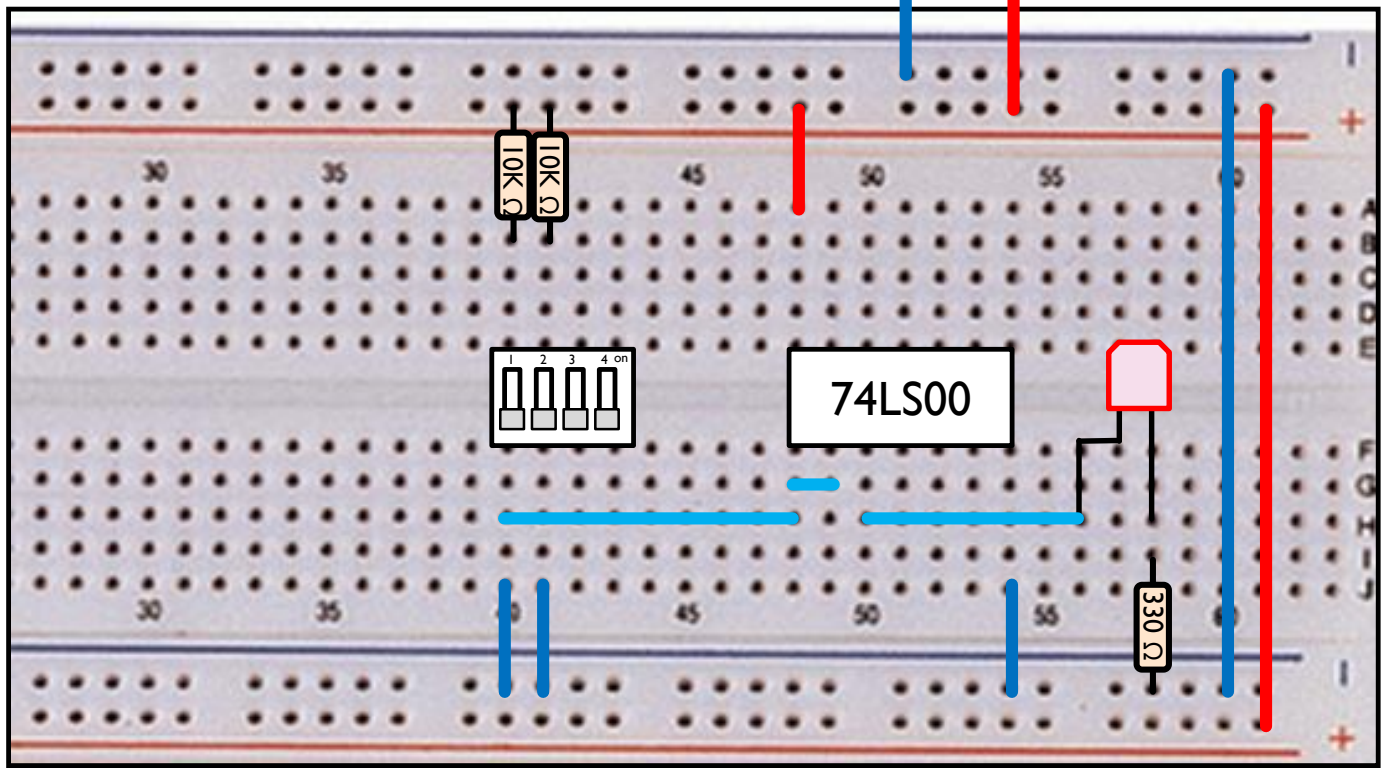
• Lab 1-2 implement AND, OR, NOT with NAND gate

1. Please design the circuits to implement AND, OR, NOT with 74LS00 (NAND)





Example of implementing NOT gate with NAND



實驗注意事項

1. 調整任何電路前請先將電源輸出關閉(output關掉, 輸入端線路移除, DC電源供應器power關掉 …)，待電路調整完再開啟
2. 電源供應器需調整成 c.v. 模式，請注意c.v.燈號是否亮著
3. 輸入電壓固定為5V (請勿使用其他電壓)

REPORT OF LAB 1 (4%) WITH DEMO SCORE (2%)

The report should include …

1. Pictures of your circuit with each state of the switch and LED (照片) (DEMO SCORE 2%)
2. Truth table and the state of the LED (真值表以及開關/LED 狀態紀錄)
3. Draw logic diagrams to implement basic gates with "NOR" gate, also write the Boolean equations for the implementations

   (畫出以NOR實作AND, OR, NOT之接線圖，以及寫出其布林函數)
4. Discussion and experience (everyone)

   (所有人的心得與討論)

- File type: pdf
- File name: Lab1_(Number of team)_report
- Deadline: 2022/3/21 24:00