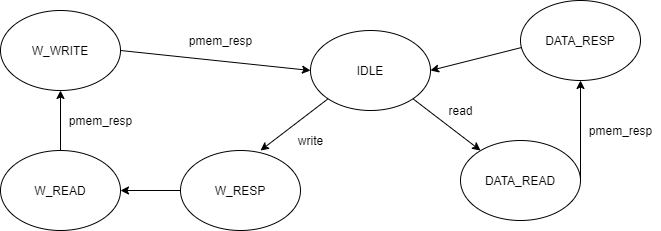
Advanced Feature Proposal for Outel

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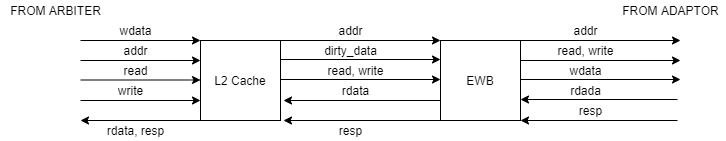
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1. Eviction Write Buffer (EWB)

The eviction write buffer (EWB) enables the cache to process the missed address first and holds the dirty data to be written back. With an EWB, the CPU can receive data faster since it doesn’t need to wait for writing back.

1. L2 Cache

The L1 cache itself is incapable of speeding up the CPU too much, especially when the CPU is handling very complex instructions and programmes. Thus, a L2 cache is essential. Here, we are planning to implement a L2 cache with higher associativity (at least 4-way).

1. RISC-V M Extension

The RISC-V M extension supports integer multiplication and division instructions. We can implement the multiplier using either the add-shift implementation from Lab5, ECE 485, or other fancy hardware algorithms such as Wallace tree or Dadda multiplier.

1. Basic hardware Prefetching

Prefetching is going to improve our CPU’s performance. We will implement prefetching function in to our arbiter unit. There should be one more state being inserted after cache read. We will use a one block lookahead prefetch. It will ask for data line a +1 when a line is accessed and result in a cache miss.

1. Local 2-level Branch History Table

With the local 2-level branch history table, at the fetch stage, we firstly check if the fetched instruction is a branch. If so, if the PC value is in the table, and if the branch is predicted to be taken, then the next instruction will be fetched based on the branch history table. We will also update the branch history table at the MEM stage.

Diagram, schematic

Description automatically generated