Progress Report 1

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We split Checkpoint 1 of our final MP4 into four subtasks: control\_rom, datapath, interconnection, and testing. Specifically, each of us was assigned at least one task: Qingyi was responsible for migrating the control module from the previous MP2 to our final project and making it compatible with our pipeline design; she was also responsible for writing the top-level file of the testbench to monitor the signal translation when running the testing code. Shitao implemented the skeleton of the pipelined datapath and other necessary modules. Finally, Mingyuan finished the interconnection between modules on the CPU level and solved signal errors.

The delivery of our CP1 is a basic pipelined CPU connecting to the provided “magic memory” and it can execute most of the RV32I instructions specified in the documentation without considering the data hazards and control hazards. The internal latches in our datapath pass the control words, calculation results, and memory data between stages to make the pipelining feasible.

We tested our implementation with the provided assembly files. We hooked the RVFI monitor on our own to compare the spec data with our results. The RVFI monitor is committed every time we have valid data passed through the MEM\_WB register and we connect the signals at the WB stage with the RVFI monitor to do the comparison. Therefore, all signals necessary for debugging such as instruction, rs1\_addr and rs2\_addr need to be carried by the internal latches to the last stage as well. To make sure that the pipelining design is capable of handling all instructions, we also checked both the data in the register files after execution and the waveform clock-by-clock to verify the working status of each internal signal.

Diagram, schematic

Description automatically generated