# Lab Assignment no.-3

1. To determine the characteristic of an NMOS and PMOS transistors and extract the device parameters such as threshold voltage, transconductance, output resistance, process transconductance parameter and the channel length modulation parameter for L= $L_{min}$, 2 $L_{min}$ and 3 $L_{min}$ keeping W=10 $L_{min}$ same in all three cases.

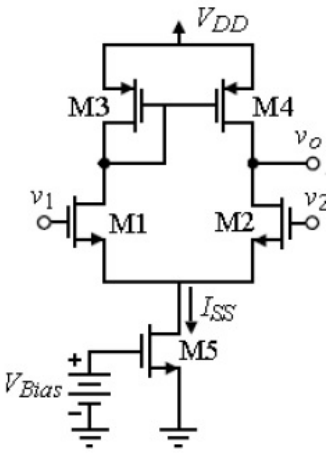
Also explain the proper reasoning for the variation of different parameters with the channel length.

(**Note**:- Where $L_{min}$ is your technology node; say for tsmc180nm, $L_{min}$ =180nm)

2.Design the schematic of a differential amplifier circuit.

(Assume M1 and M2 are NMOS, W=5Lmin, L=L $L_{min}$ and for M3 and M4 PMOS W=10Lmin and L=$L_{min}$ and for M5 NMOS W=7.5 $L_{min}$, L=L $L_{min}$ ).

Determine the gain, CMRR and ICMR of the differential amplifier.




3.Design schematic of CMOS inverter and perform its static and dynamic analysis at 1pf load.

a) Find out (W/L) ratio of PMOS and NMOS for which it is maximum noise immune.
b) Find the switching threshold at different (W/L) ratios.
c) Find rise time, fall time and propagation delay.
d) Find Static, dynamic and direct-path current losses of the circuit.
(**Help**:- Read 1.1.3 from page: 31; 5.5.1 from page: 174, and from page: 179 from eBook of Rabaey)

4. Design schematic for 3 input CMOS NAND and NOR gate.

a) Size the transistors such that its worst case current driving capability is equivalent to that of an inverter.

(For inverter PMOS transistor has L=$L_{min}$, W=5 $L_{min}$ and NMOs transistor has W=2Lmin, L= $L_{min}$. Assume that channel length of all transistors is fixed at L= $L_{min}$)

Calculate the rise time, fall time and propagation delay in this case.

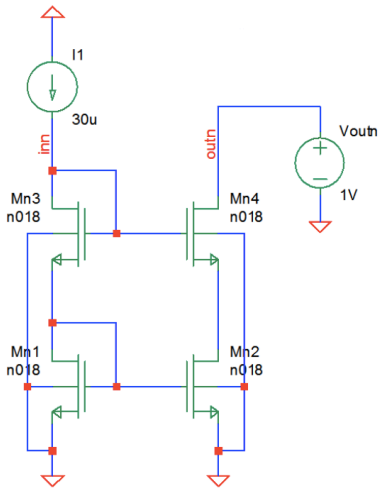
b) Change the W/L ratio of NMOS and PMOS such that they have equal rise time and fall time.

c) Calculate the propagation delay in response to change in W/L ratio. Also calculate the variation of propagation delay in response to different input patterns.

Suggest the possible reasoning for the variation of propagation delay with input patterns and ratio at which rise time and fall time are equal.

(References: -Logical Effort of complex gate at page:245; Static property of complementary CMOS gate at page: 234; Delay Dependence on input patterns at page:243; additional study of section 5.4.3 at page:168)

5. Cascode current Mirror:




(a) Size the transistors in the mirror for a current gain equal to unity, a 30µA input current and $VD_{Sat}$ =200mV for all devices.

(b) Validate the operating points of the components and determine the input and the output resistances. Use the small signal parameters returned by the simulation. Estimate the minimum allowed output voltage and the following parameter for all NMOS transistors: $V_{GS}$, $V_{DS}$, $I_D$, $VD_{Sat}$, $V_{Th}$, gm and $g_{DS}$

(c) Demonstrate through simulation that, if all transistors have same (W/L), the current gain is approximately equal to unity, even when the input-output imbalance is not zero (Vin≠Vout). What is the role of the cascode transistors in determining the current gain error?
(d) Simulate the output characteristic of the mirror, measure the output resistance around the operating point and estimate the $V_{o\text{-}min}$ voltage.
(e) Simulate the input characteristic and measure the input resistance around the bias point.

(Rabaey)

Soft copy of Digital Integrated Circuit by Jan M. Rabaey - https://drive.google.com/open?id=1XGjWSkpIcXY8aNtWXdWwRcd_Rw6xg-bg