Experiment -2

1.1 Aim

Design of Single stage CS amplifier (i) with resistive load (ii) active load

1.2 Circuit Description

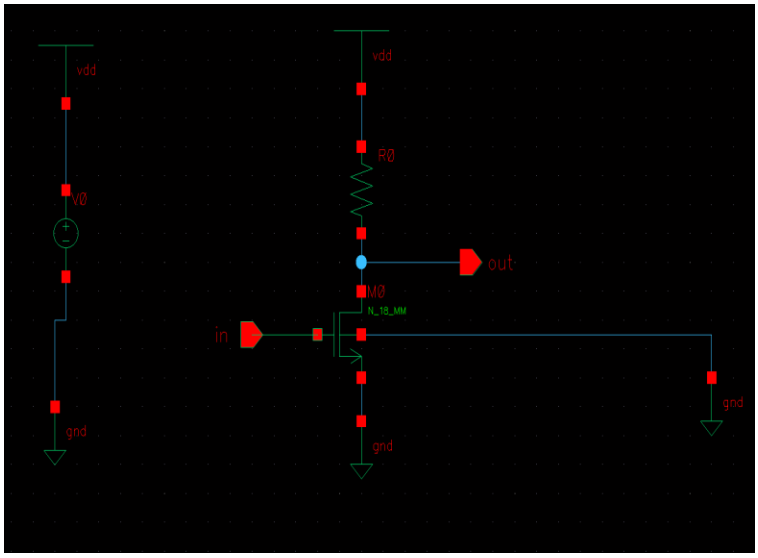

Fig.1.1 CS amplifier with resistive load

In fig.1.1 a simplest form of amplifier is shown. It mainly consists a nMOS, connected in common source configuration. Actually MOS converts gate volte to current i.e. gm Vgs. To get this current in the form of voltage, we attach a resistor and across it we got the corresponding voltage. Here output resistance will be Rd parallel with rds.

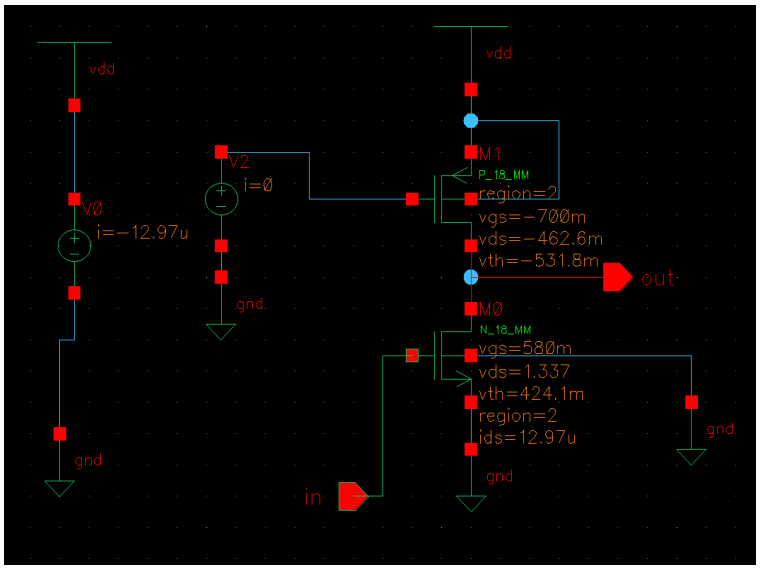

Fig.1.2. CS amplifier with active load

CS source amplifier with active load is shown in figure 1.2, which have output resistance of rds/2 because two rds term will come in parallel. As a load we are using pMOS because it is easier for a PMOS to make current source while connected with VDD.

1.3 Theory

- It has very high input impedance; relatively high gain, low noise, speed, and simplicity, common source amplifiers find different applications from sensor signal amplification to RF low-noise amplification [1].
- It provides 180° phase shift at the output while input is applied to gate and output is taken from the drain terminal [2].
- Being a single stage amplifier it doesn't have much gain but swing is high. These are always stable systems.
- In general its gain is gm*Rout
- It has one dominant pole at the output and one non-dominant pole at the input. With this it also has one right hand side zero [3].

1.4 Design, analysis and calculation

Suppose we want to design it for maximum voltage. Consider over drive voltage – 0.2 V and assume (W/L) is 2.

Now using

$$I_D = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}(V_{GS} - V_T)^2$$

Calculate Id

Id=10.8 uA

Av = gm *(Rd ‖ rds)

If Rd is chosen to be equal to rds, then effective rds will become half

And now, using formula of gain, Av= $\sqrt{2I_{D1}\,\mu_n C_{ox}\frac{W}{L}}$ * (1/λI_{D1})/2 gain can be calculated theoretically Av=10

But as we know rds is very high and if we choose Rd equal to rds then it will take all the voltage at drain and will allow only a very small vds.

To fulfill this condition we can go for active load.

In case of active load Rout = rds ‖ rds and it will increase the gain.

Av= gm (= rds ‖ rds)

1.5 Observation

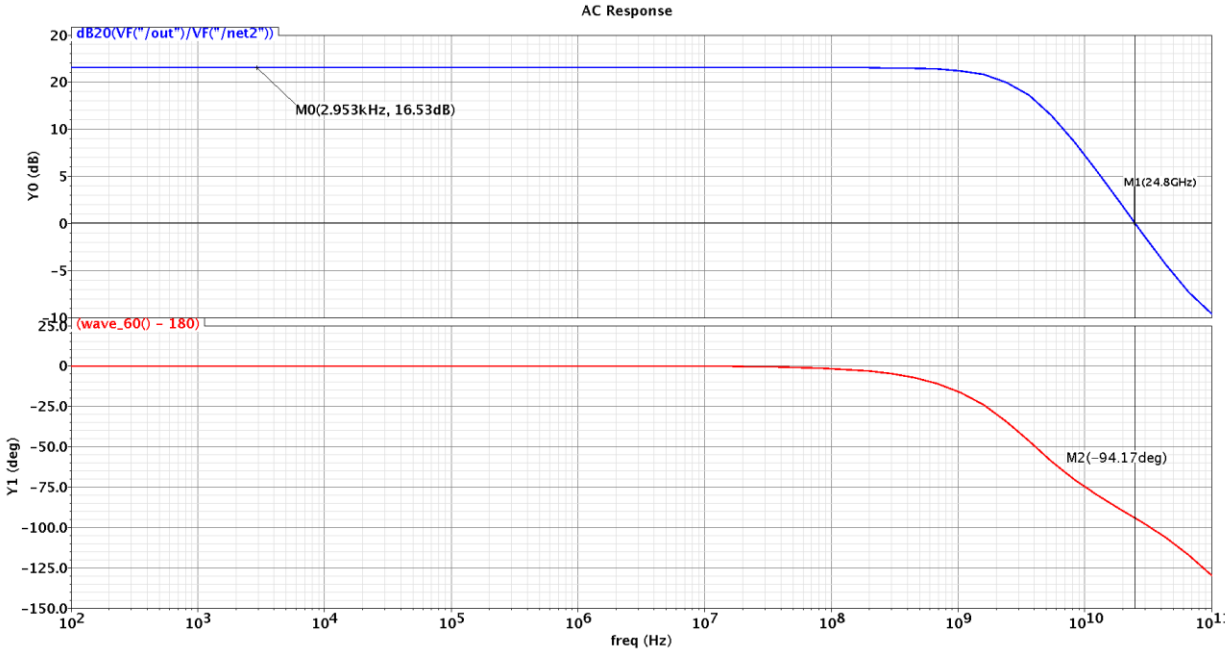

Fig.1.3 Frequency response of CS with resistive load

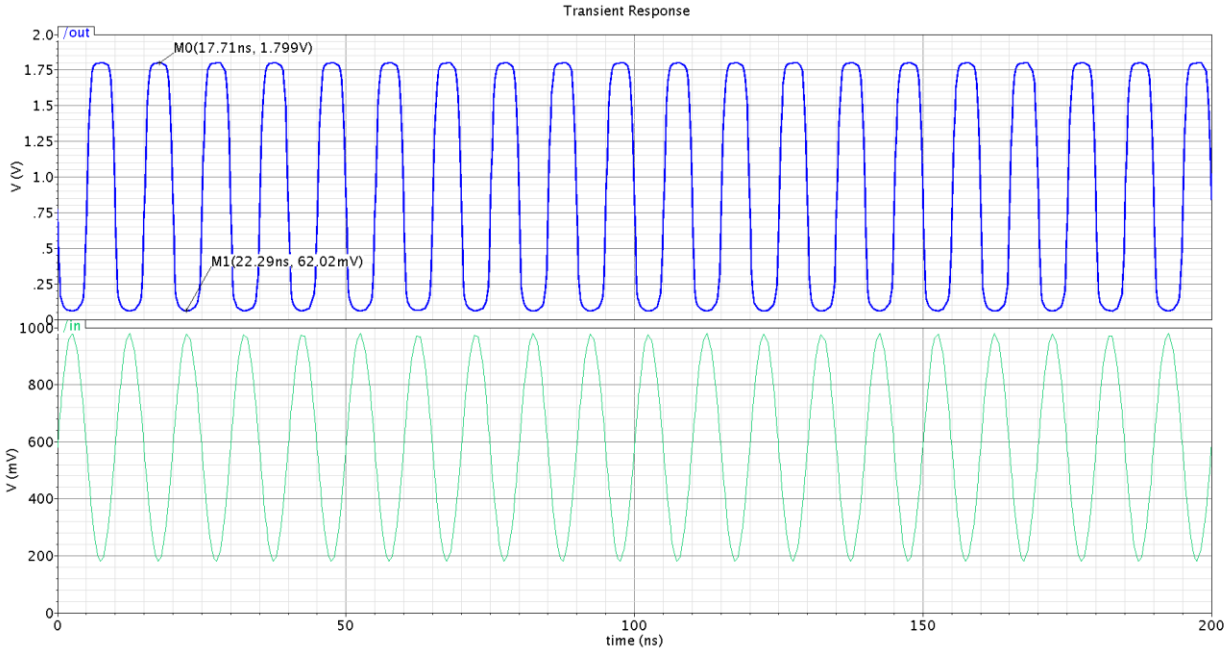

Fig. 1.4. Output voltage swing of CS with resistive load

- Fig.1.3 shows the frequency response of CS amplifier in which it clear from the plot that gain is 16.53dB ≈ 6.7 . We have calculated it as 10 but we could achieve it 6.7.
- It has a phase margin of 86° which means the system is highly stable.
- GBW of the system is 24 GHz and the 3dB frequency is 1 GHz.
- 1 dB compression point it at 11 GHz frequency, see from figure 1.3.
- This system has a great swing. From calculation it is Vdd to Vov i.e. 1.8V to 0.2V but from figure 1.4 it is peak to peak 1.7 V

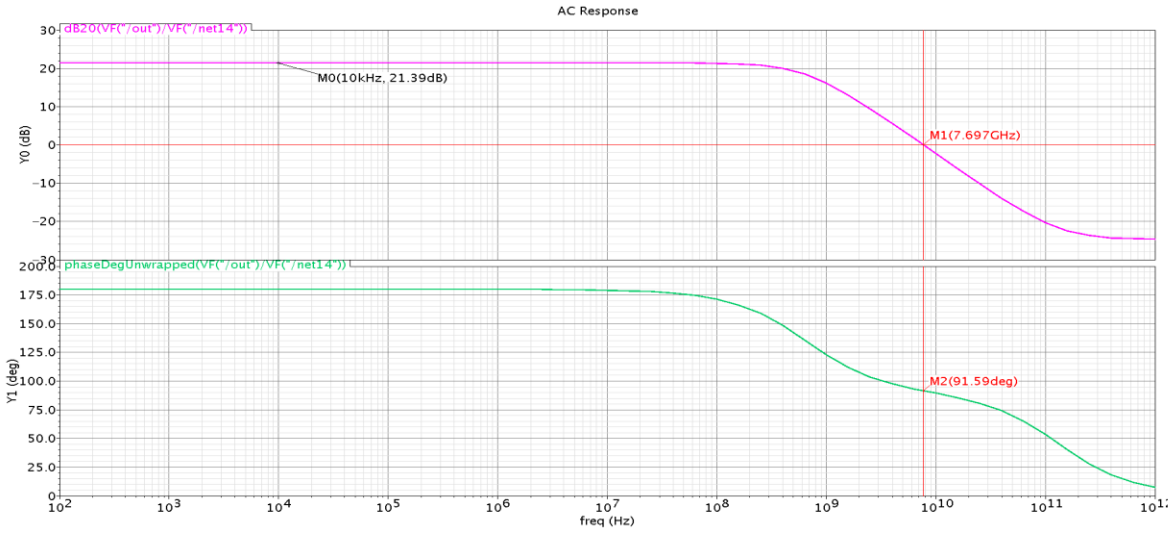

Fig.1.5. Frequency response CS with active load

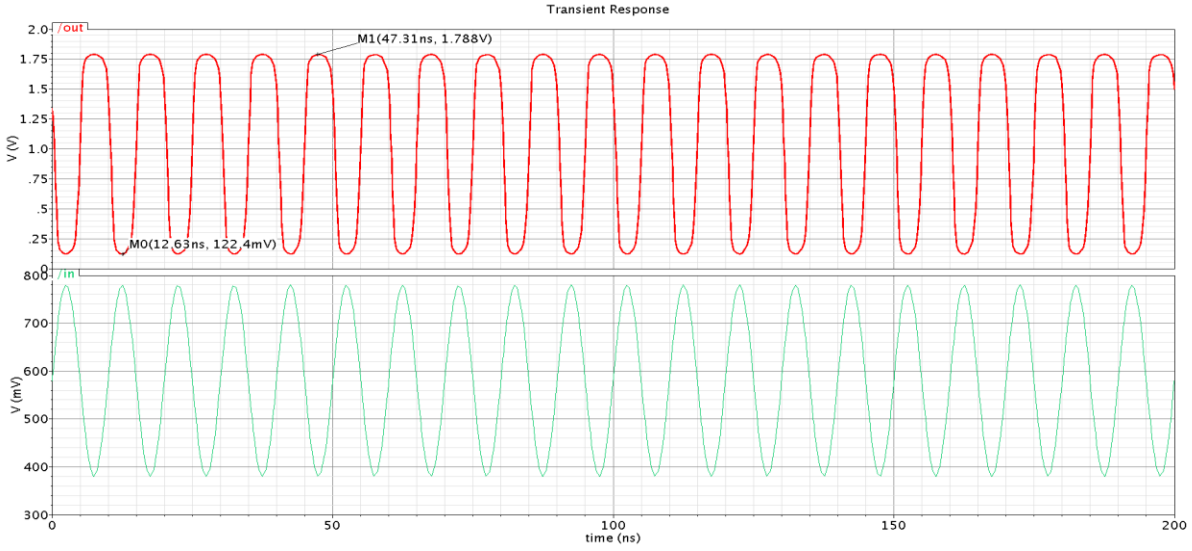

Fig.1.6. Output voltage swing of CS with active load

- It is clear that the gain of using active load with CS increases its gain. Form figure 1.5, gain is 21.39 dB ≈ 11.73.

- Phase margin almost remains same, in this case it is 89°.
- GBW has reduced to 7.6 GHz and so the 3dB bandwidth.
- 1 dB compression point is at 120 MHz.
- In this case swing becomes somewhat poor compare to previous case. It is because theoretically Vmax = VDD-Vov = 1.6 V and Vmin=0.2V. From figure 1.6 peak to peak swing is 1.65 V

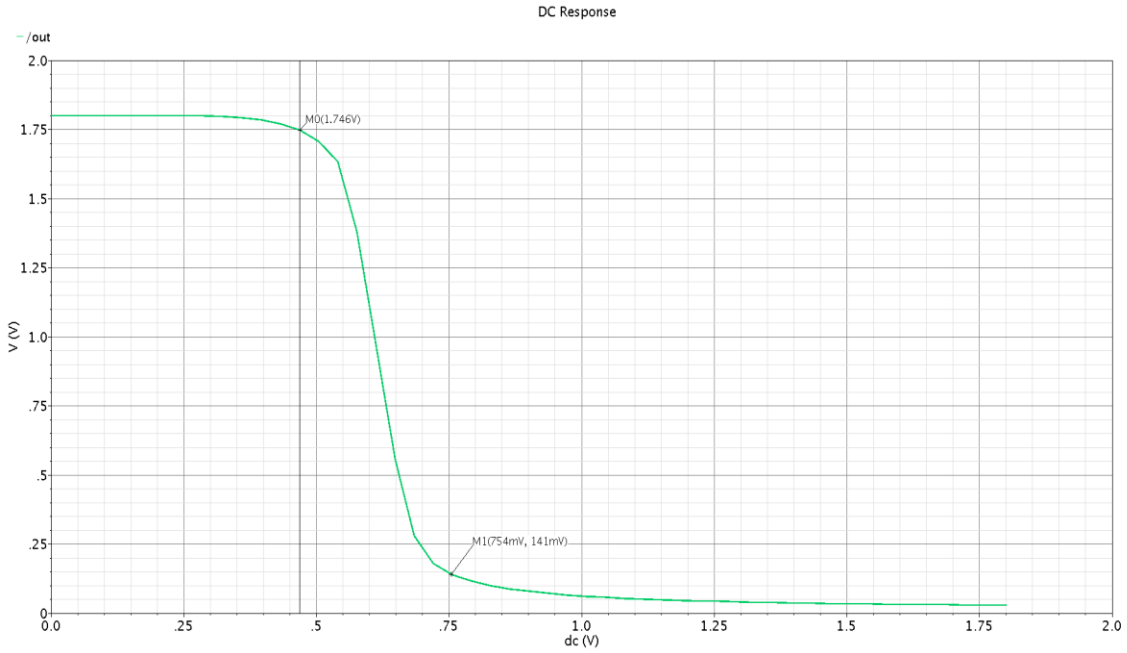

Fig. 1.7. Output voltage to input voltage curve has been drawn

From here also we can estimate the swing of the cs amplifier. We need to look for slop = 1 at this transfer curve. It is drawn here just to verify the swing values.

1.6 Conclusion

- Gain of CS amplifier is very small.
- This kind of system is highly stable as phase margin is close to 90°.
- 1 dB compression point also reduces after using active load with CS.

TABLE I

Parameter	Calculated	Simulated
Av	10	7.6
Id	10.80 uA	11 uA
P-P Swing (resistive load)	1.6 V	1.7V
P-P Swing (active load)	1.4 V	1.65V

- Gain CS with active load is more as compare to CS with resistive load.

- Swing of CS with active load is less compare to CS with resistive load.
- Frequency response of CS amplifier gives one dominant pole at output.
- These kind of amplifiers are not sufficient, therefore we move towards cascode , folded and other structurs.

Reference-

[1]B. Razavi, “Design of Analog CMOS Integrated Circuits”, Tata McGraw Hill edition, 2002.

[2]Willy M. C. Sansen,”Analog Design Essentials” Springer; 1st ed. 2006

[3] Phililip E. Allen and Douglas R. Holberg,”CMOS Analog Circuit Design”, Oxford University Press,2004