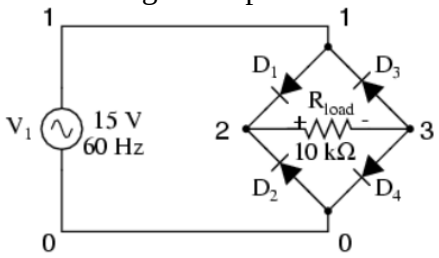
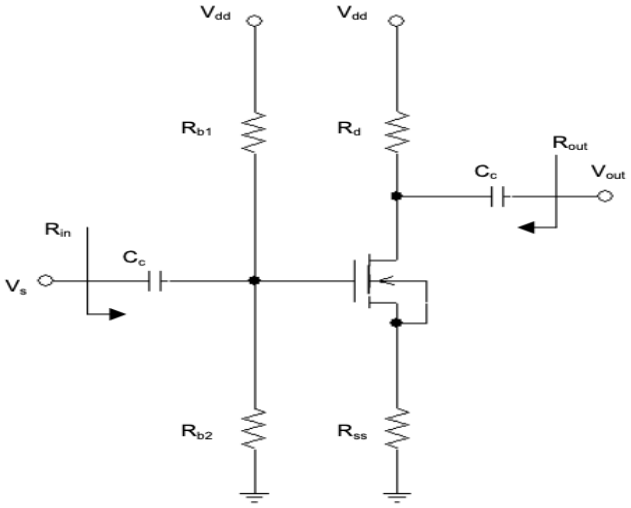
EE311 Laboratory Assignment Problems

Please solve following problems using SPICE.

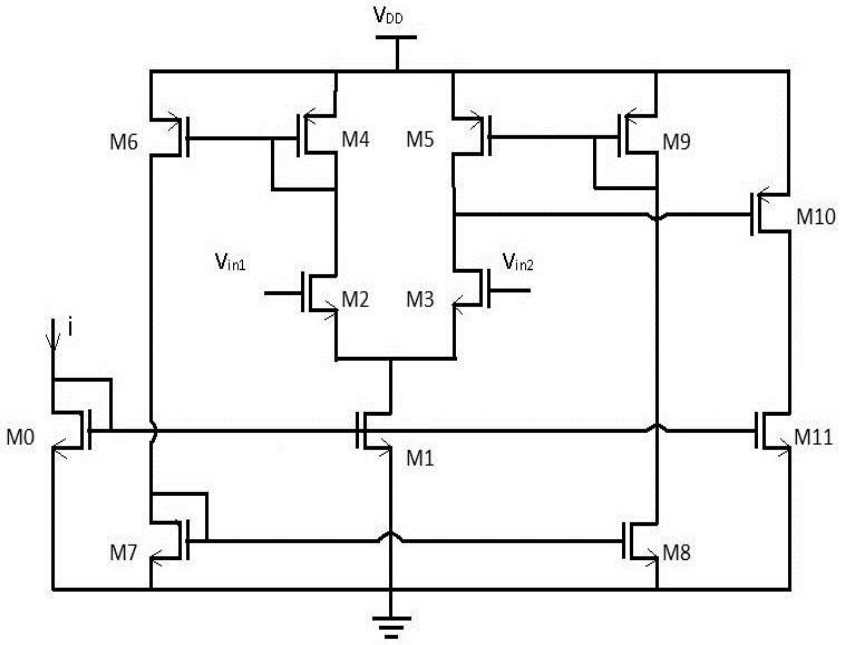
1. A bridge rectifier circuit is given below.
   (a) Find out voltage at each node.
   (b) Plot output waveform for the given input.



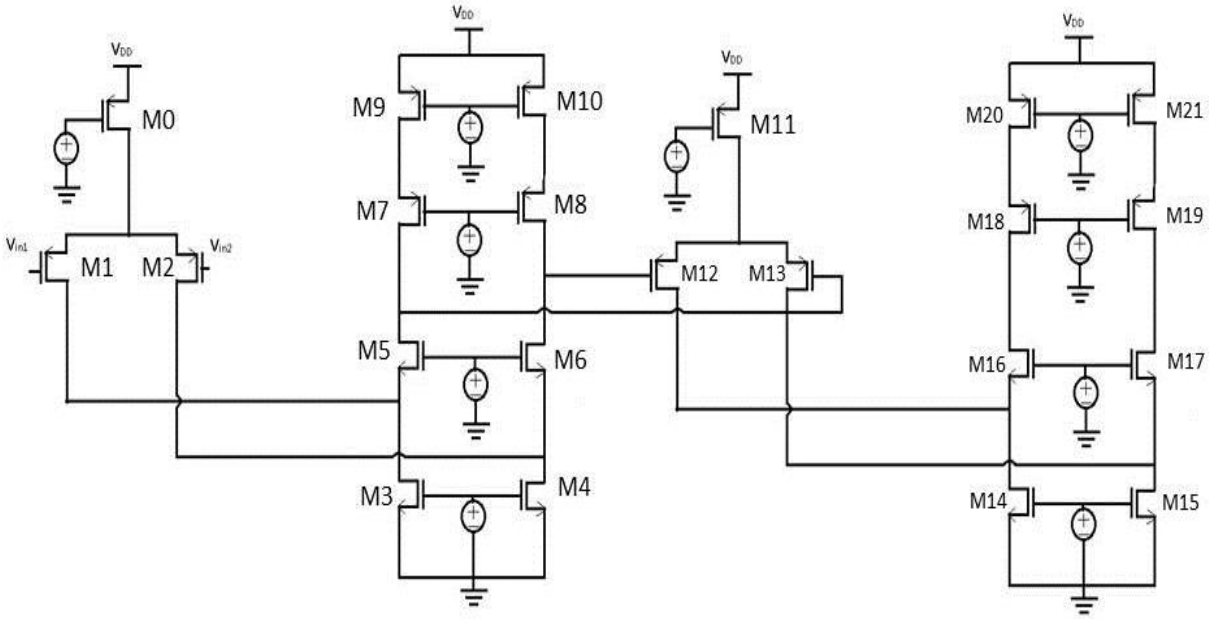
2. Design a Band Pass, Low Pass and High Pass circuit. Design parameters for these circuits maybe chosen on your own.
3. Plot nMOS and pMOS transfer characteristics for different V_{ds} and V_{gs}.
4. Design of CMOS inverter using SPICE.
   (a) Calculate Rise Time and Fall Time using transient analysis, propagation delay with and without load capacitor, C_L.
   (b) Plot VTC of CMOS Inverter for DC input and calculate noise margin (NM).
5. Design of 3 input CMOS NAND, 3 input CMOS NOR and CMOS EX-OR gates using SPICE. Study the effect of change of MOSFET sizes on the gate delays and appropriate comments on it.
6. Design 8 bit adder, 8 bit register, 16 bit counter (of your choice) using SPICE.
7. Design 16 bit fixed point multiplier using SPICE. **(Refer CMOS VLSI Design: A Circuits and Systems Perspective by Neil Weste and David Harris)**
8. Design nMOS amplifier using voltage divider biasing.
   (a) Apply a 50mV peak-to-peak 4kHz sinusoidal signal at the input. Measure the output signal at the drain of the MOSFET
   (b) Using the same circuit, connect a load of 1Meg Ohm at Vout. Measure the output signal at the drain of the MOSFET, and calculate the gain. Repeat this procedure for load values of 50k, 5k, 1k, 500, and 50 ohms. Comment on these variation of characteristics of circuit for each load



9. Design a differential cascade amplifier with bias given below using SPICE.



10. Design a two stage amplifier given below using SPICE.



NOTE:

1. The problems should be completed by **18 August 2019, 23:59Hrs** and submitted to **gtiitgcourses@gmail.com**.No submission will be entertained by us after the above mentioned date.
2. The email must have subject line as per the format given, **"NAME_ROLLNO_SPICE_ASSIGNMENT SUBMISSION"**
3. It is strong advised not to copy assignments other at the end of the semester during evaluation, otherwise severe penalty will be imposed.

4. The viva based on the assignments will be conducted by EE311 Laboratory TAs. The final decision will be of TAs only while assignment evaluation and only in the exceptional cases, course instructors will intervene.
5. For any query, you can approach TAs after taking an appointment with them.
6. For any dispute or issue to be resolved, you can always approach course instructors, Prof. Harshal B. Nemade and Dr. Gaurav Trivedi.

All the best!