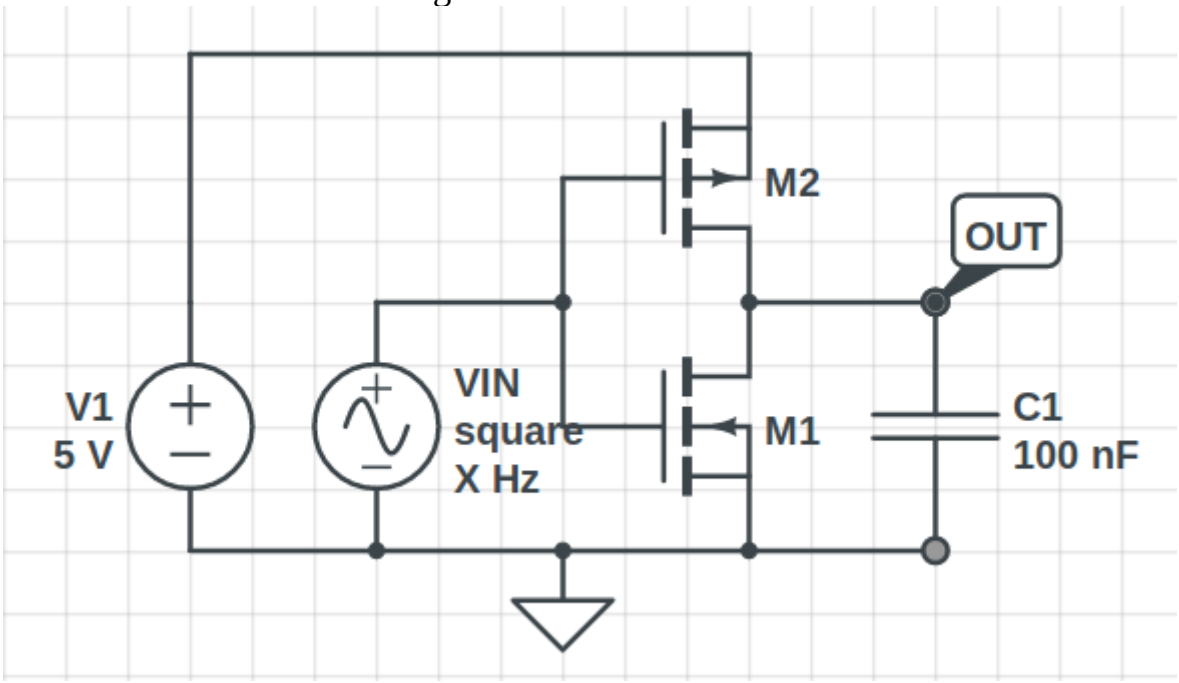
ASSIGNMENT 4

AIM:

To design a CMOS inverter and
a. Calculate rise and fall time with and without load capacitor.
b. Plot VTC for DC input and calculate noise margin.

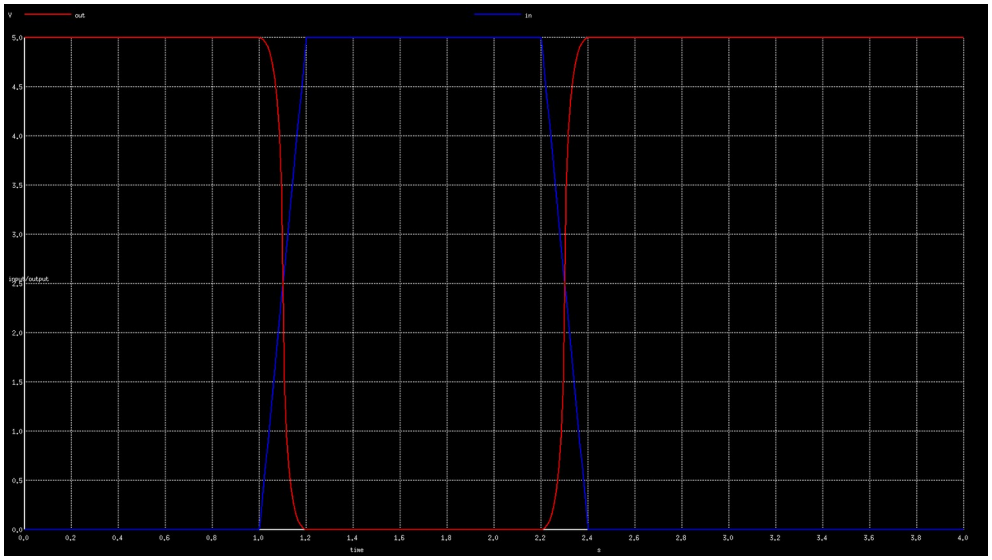
CIRCUIT:

CMOS inverter has been designed as follows -



OBSERVATIONS:

1. Vout and Vin wrt time



We find that with CL = 0.1u

Fall Time, Tf = 6.213165 x 10^{-2} s

Rise Time, Tr = 6.254552 x 10^{-2} s

Propagation Delay, TPHL = 7.151354 x 10^{-3} s

Propagation Delay, TPLH = 7.141256 x 10^{-3} s

We find that without CL

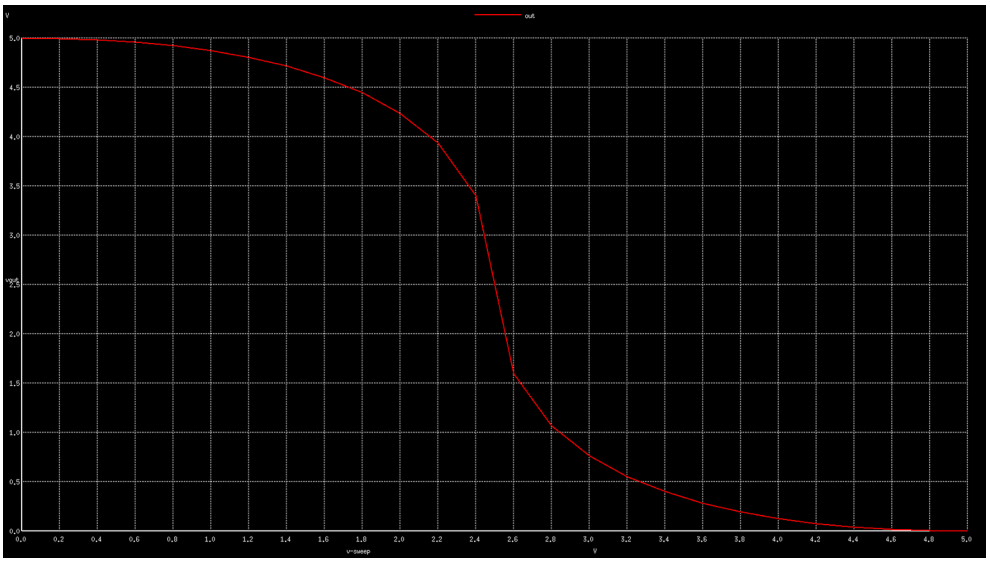
Fall Time, Tf = 6.199314 x 10^{-2} s

Rise Time, Tr = 6.195805 x 10^{-2} s

Propagation Delay, TPHL = 4.918616 x 10^{-7} s

Propagation Delay, TPLH = 4.719901 x 10^{-7} s

2. VTC



Since NGSPICE derivative function wasn't working it was difficult to find out the noise margin.

CONCLUSION:

Addition of capacitive load increased the propagation delay by a large margin while the fall time was hardly affected.