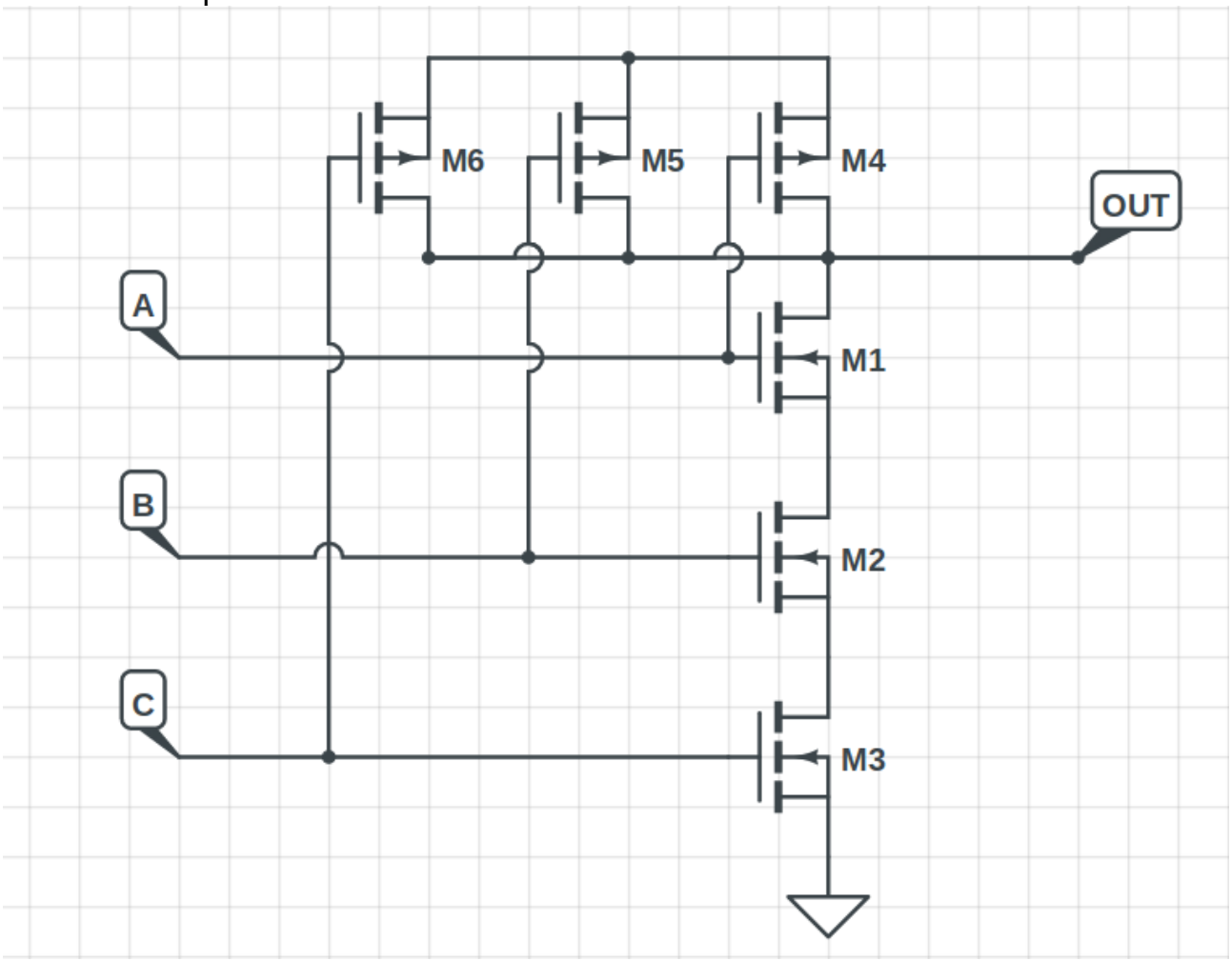
ASSIGNMENT 5

AIM:

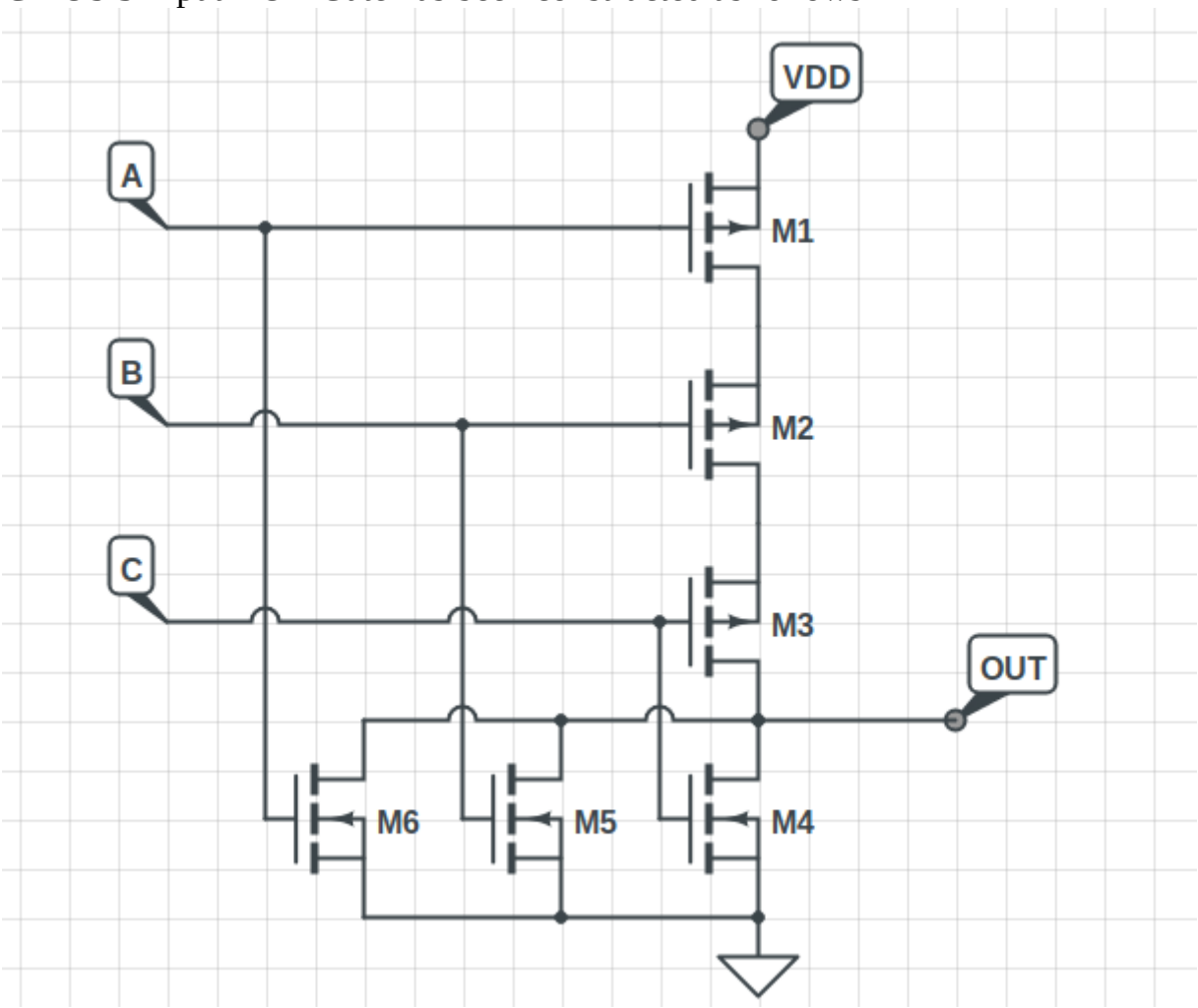
To design 3-input CMOS NAND Gate, 3-input CMOS NOR Gate and 2-input CMOS XOR Gate and study the effect of change of MOSFET sized on gate delays.

CIRCUIT:

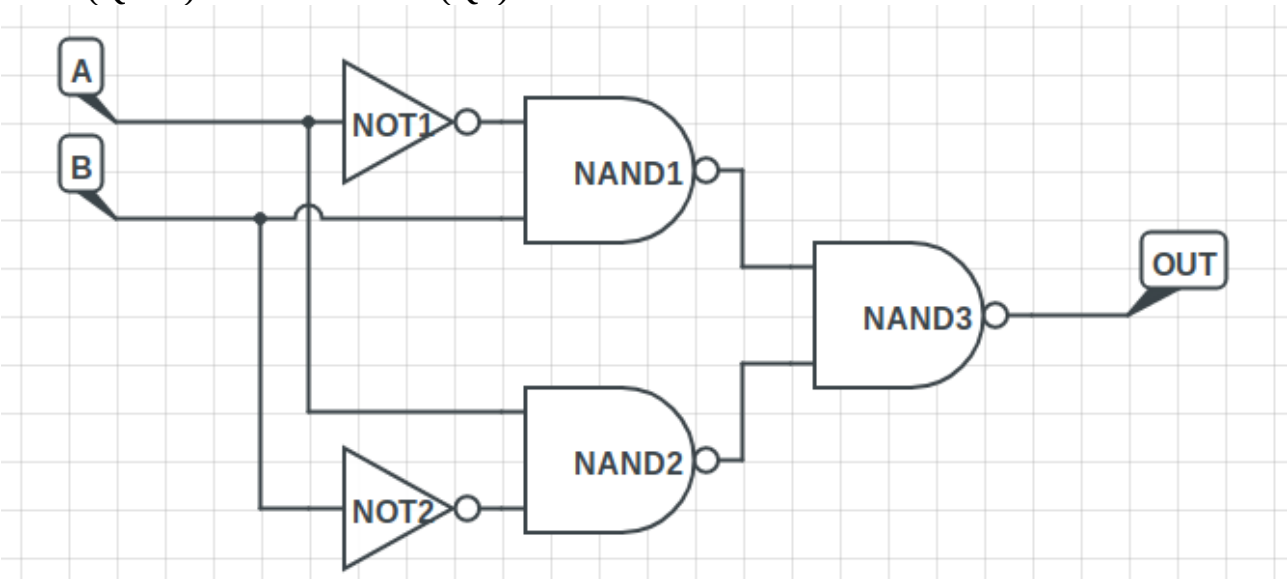
1. CMOS 3-input NAND Gate has been constructed as follows-



2. CMOS 3-input NOR Gate has been constructed as follows-

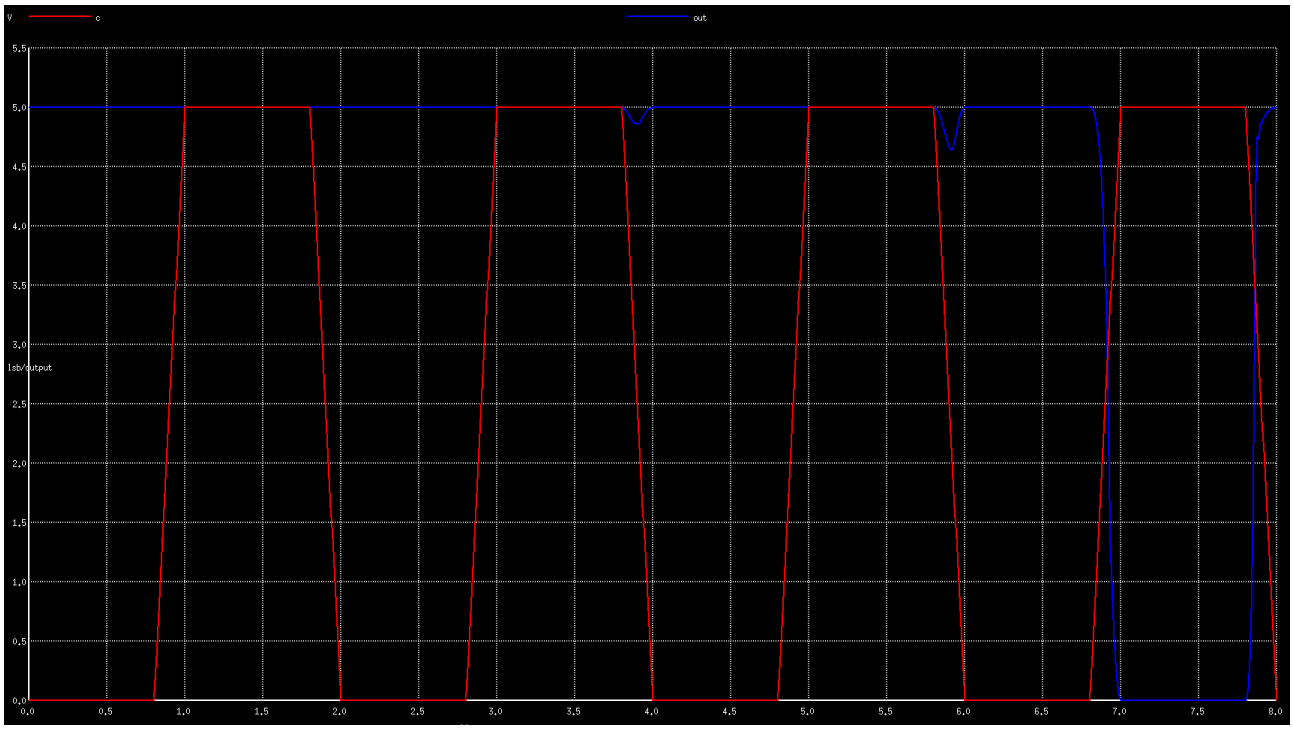


3. CMOS 2-input XOR Gate has been constructed using the 2-input NAND Gates(Q5-A) and NOT Gates(Q4) as follows-

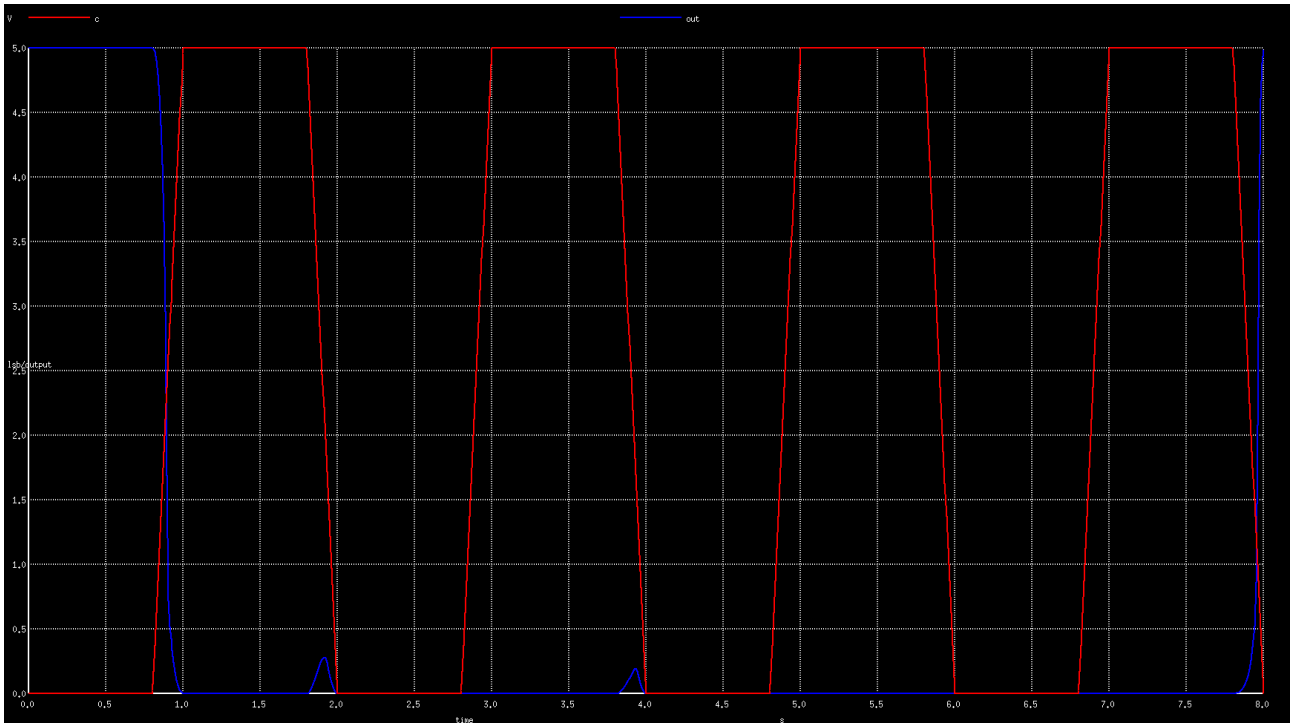


OBSERVATIONS:

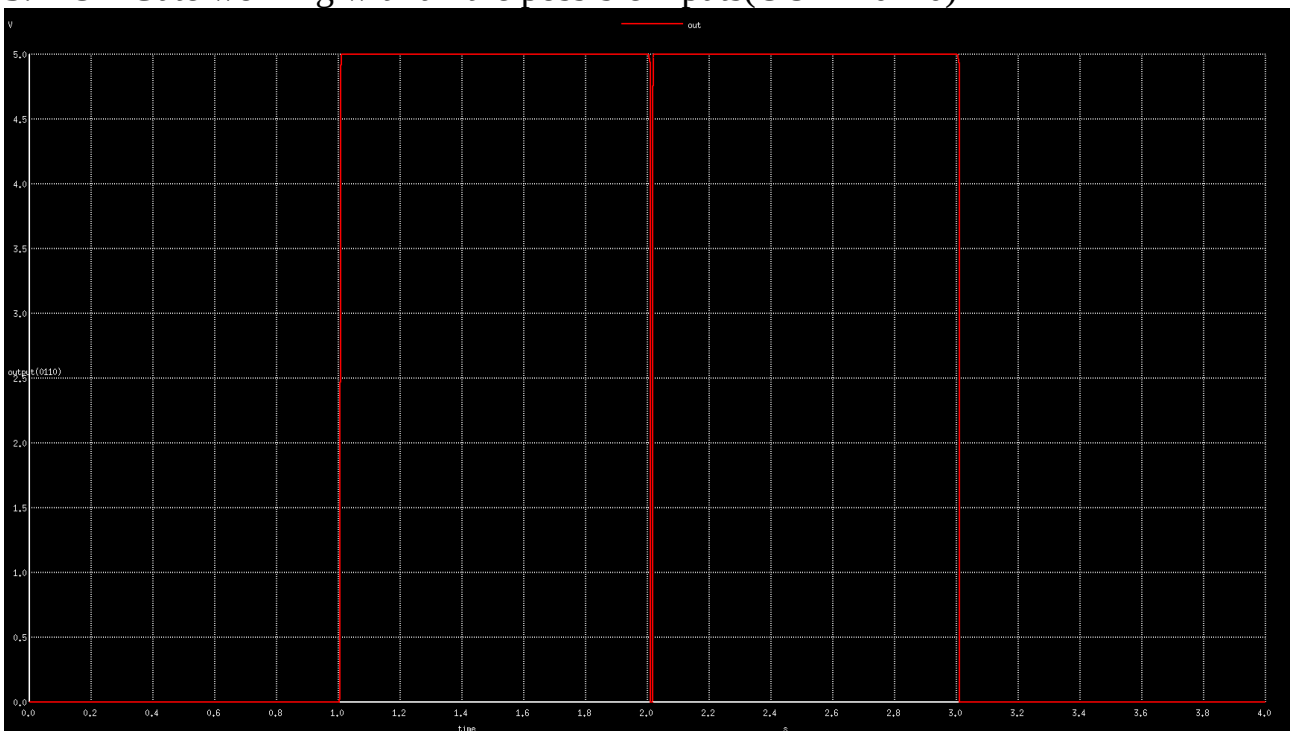
1. NAND Gate working for the possible inputs



2. NOR Gate working with the possible inputs



3. XOR Gate working with all the possible inputs(OUT = 0110)



CONCLUSION:

The gates work as expected except for propagation delays due to non-ideal character