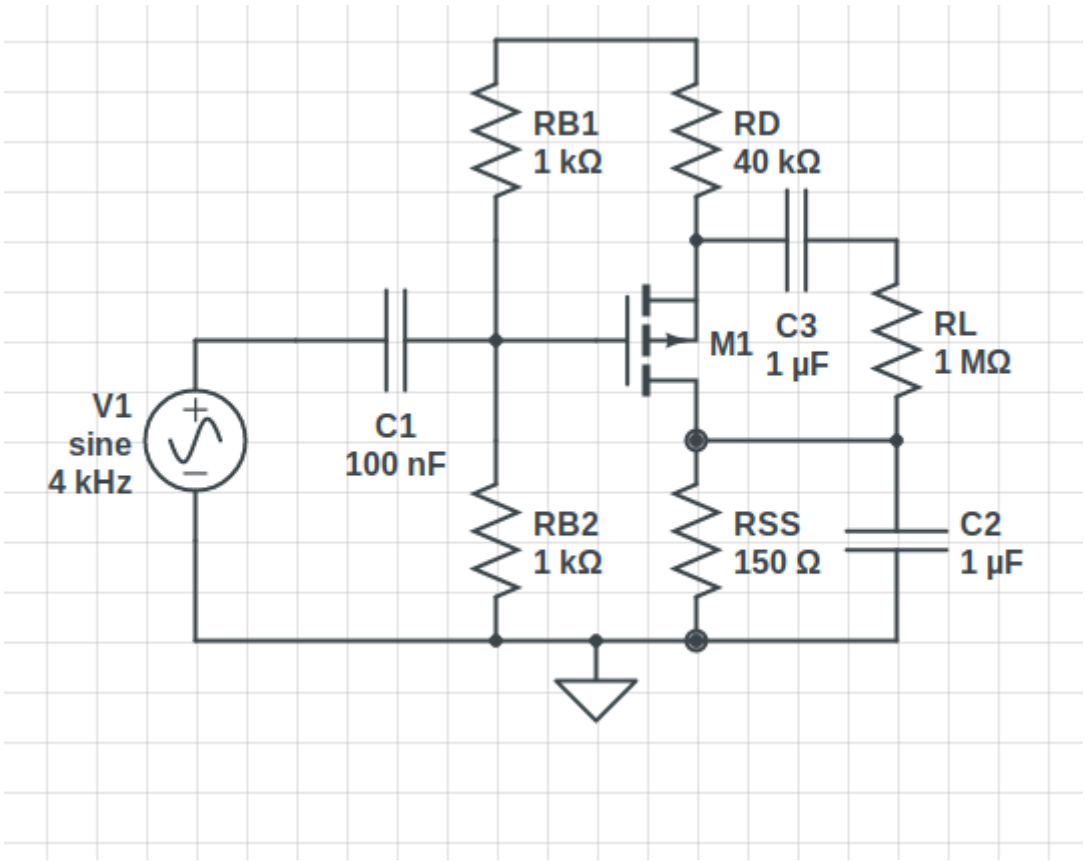
ASSIGNMENT 8

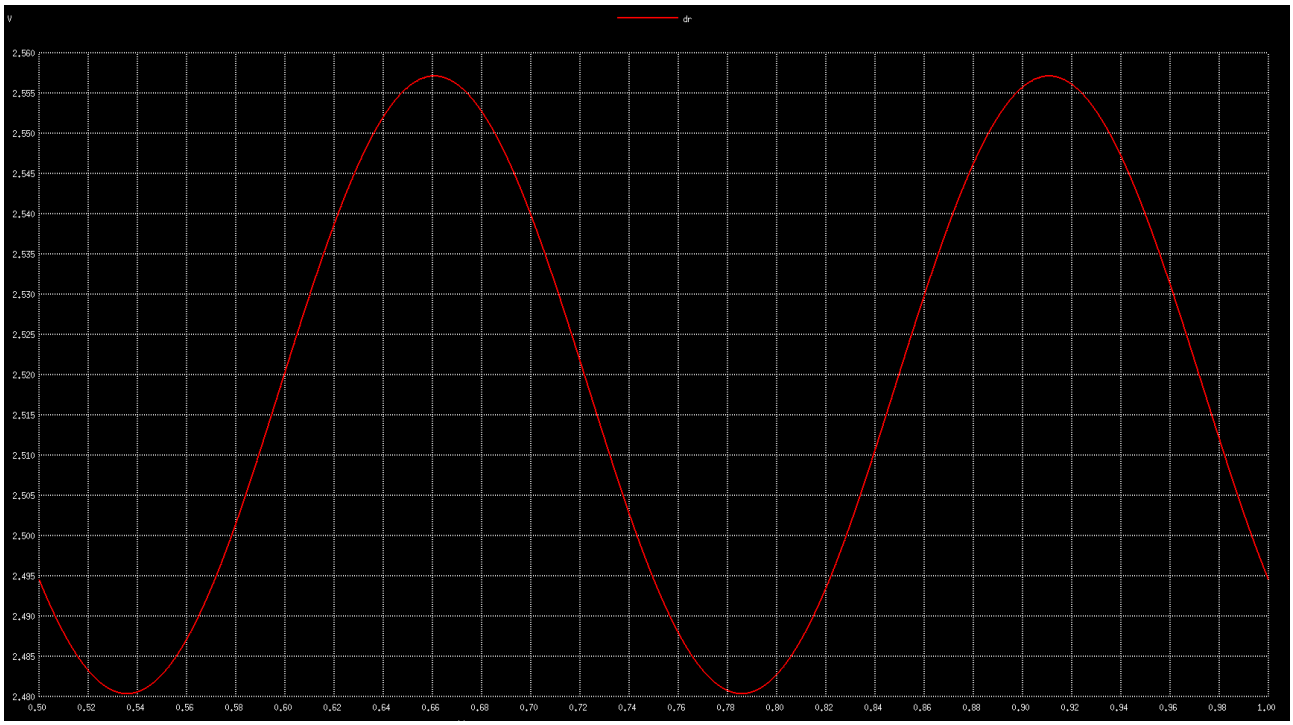
AIM:

To design an NMOS amplifier with voltage divider biasing.

CIRCUIT:



OBSERVATIONS: Without Load resistance.



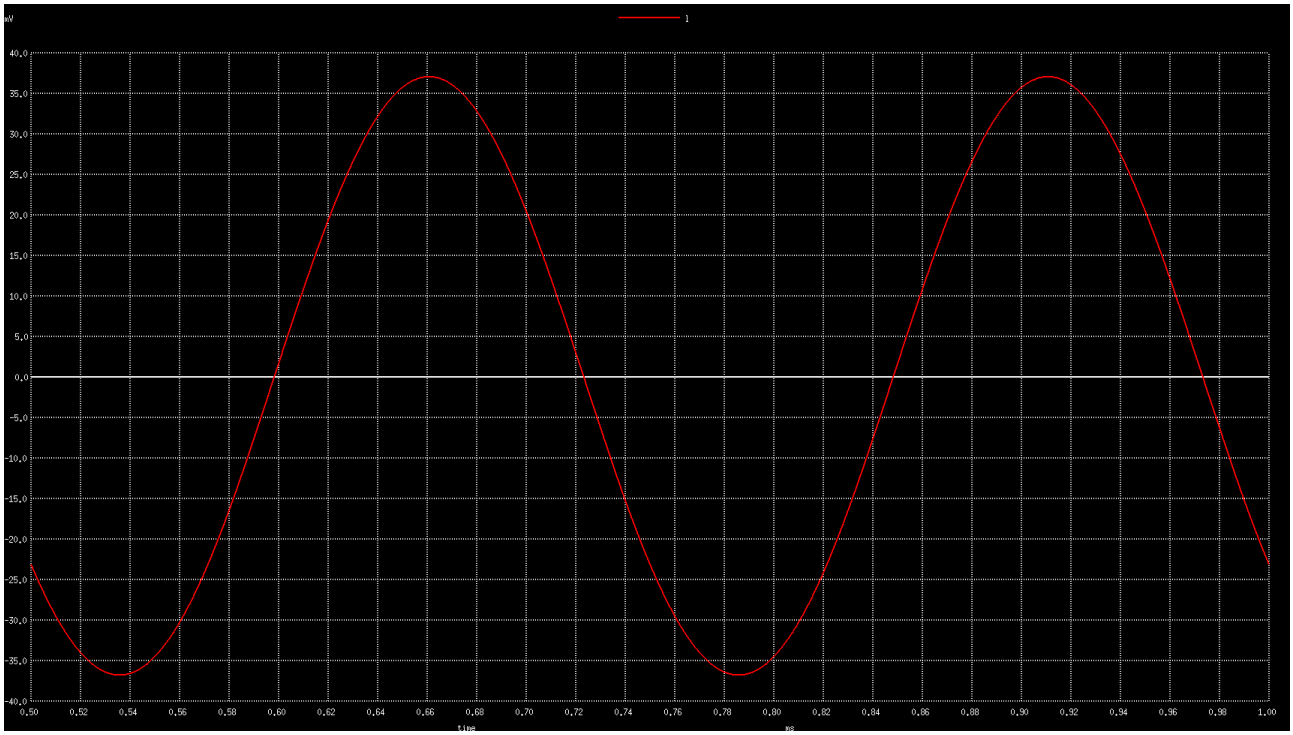
Vout vs t

Data

```
No. of Data Rows : 50001
vmax             =  2.557116e+00 at=  6.607528e-04
vmin             =  2.480348e+00 at=  7.857528e-04
vmax-vmin = 7.676800e-02
```

We see that Vin = 50mVpp, we have Vout ~76.mVpp, hence we have a gain of ~1.536

With RL = 1MOhm



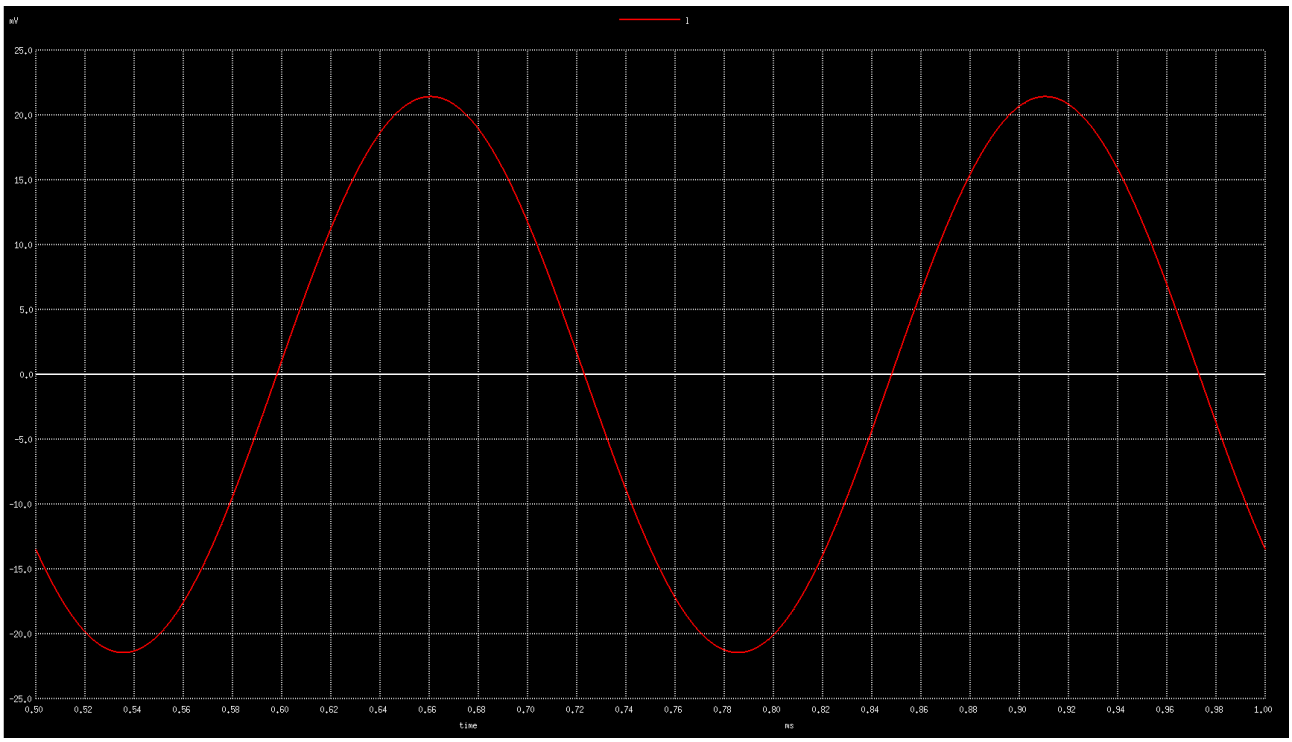
Data -

```
No. of Data Rows : 50001
vmax             =  3.705712e-02 at=  6.607428e-04
vmin             =  -3.680028e-02 at=  7.857328e-04
vmax-vmin = 7.385740e-02
```

Gain ~1.4772

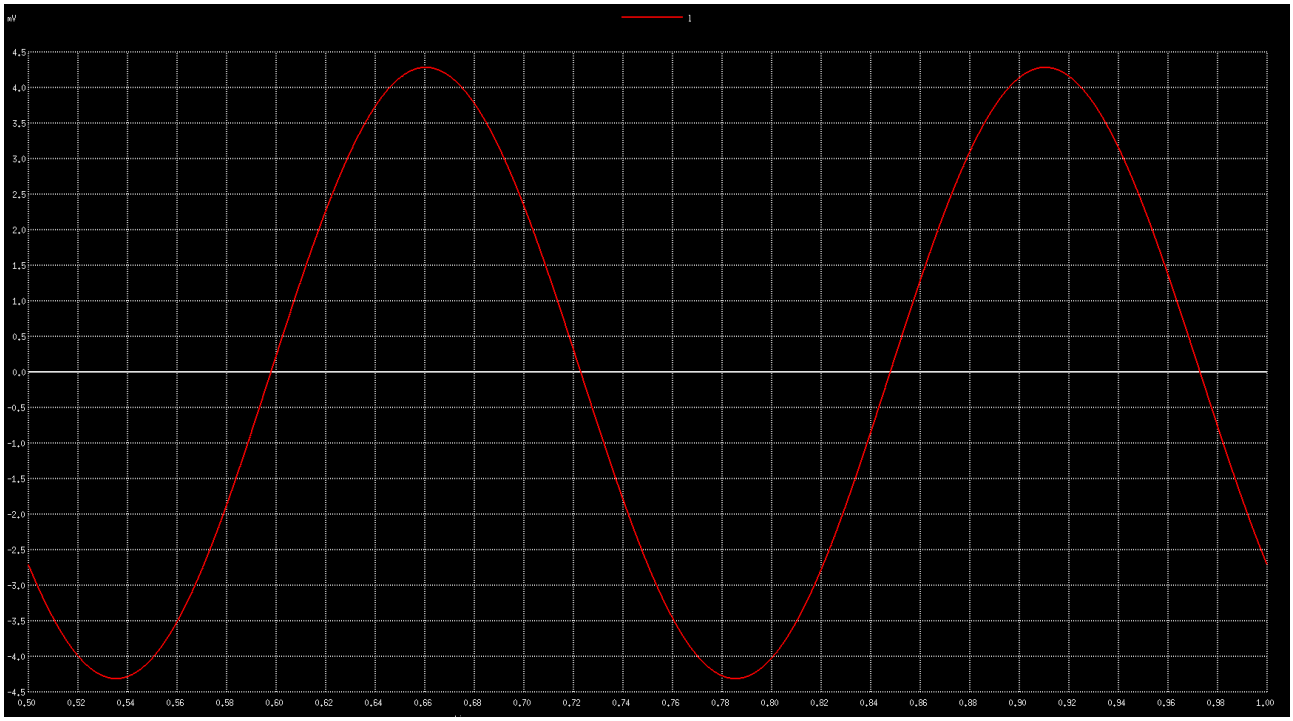
RL = 50KOhm

```
No. of Data Rows : 50001
vmax             =  2.141218e-02 at=  9.105828e-04
vmin             =  -2.146479e-02 at=  5.355828e-04
vmax-vmin = 4.287697e-02
```



Gain ~0.8576

RL = 5KOhm

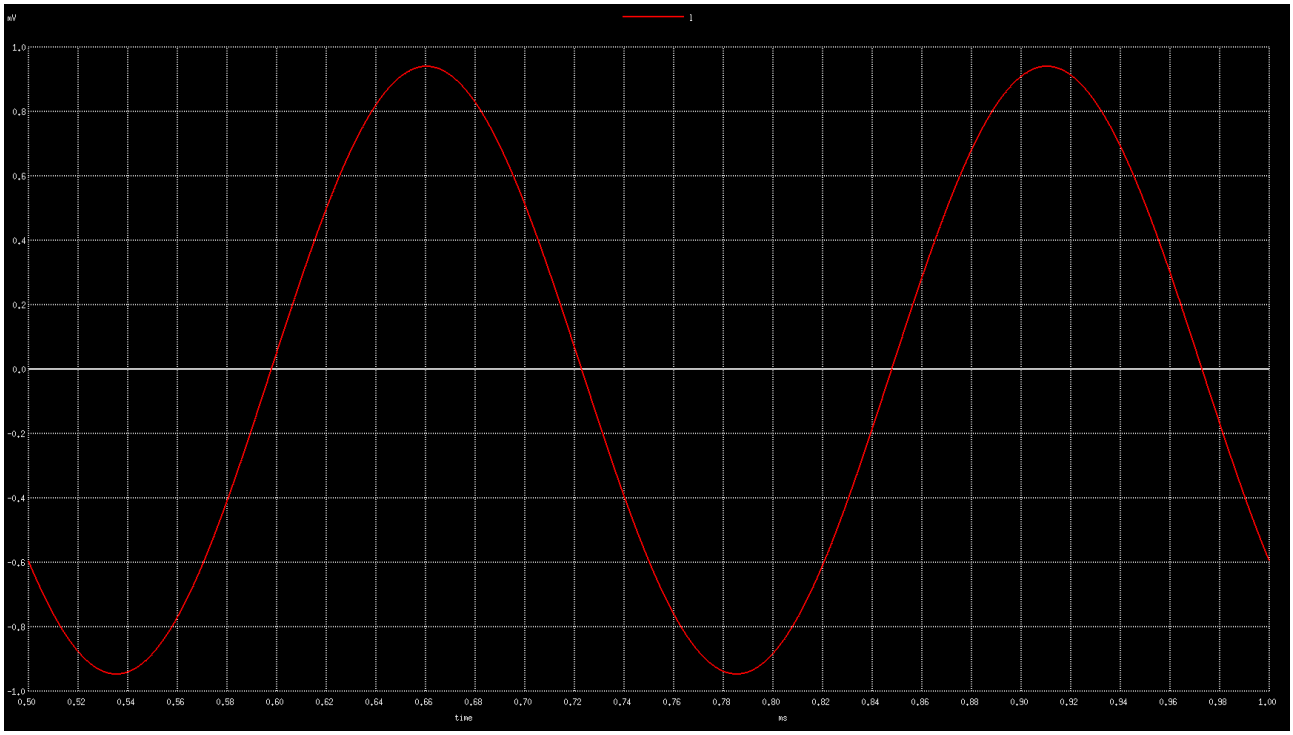


Data

```
No. of Data Rows : 50001
vmax             =  4.283001e-03 at=  9.104028e-04
vmin             =  -4.313592e-03 at=  5.354028e-04
vmax-vmin = 8.596593e-03
```

Gain ~ 0.172

RL = 1KOhm



Data

```
vmax                =  9.401780e-04 at=  9.103628e-04
vmin                =  -9.471151e-04 at=  5.353728e-04
vmax-vmin = 1.887293e-03
```

Gain ~ 0.378

CONCLUSION:

We find that for lower Load Resistance (RL), the gain decreases.