Sample Report 2

PART A: Design a NAND layout from the viewpoint of the schematic

SCHEMATIC OF NAND AND CIRCUIT DESCRIPTION:

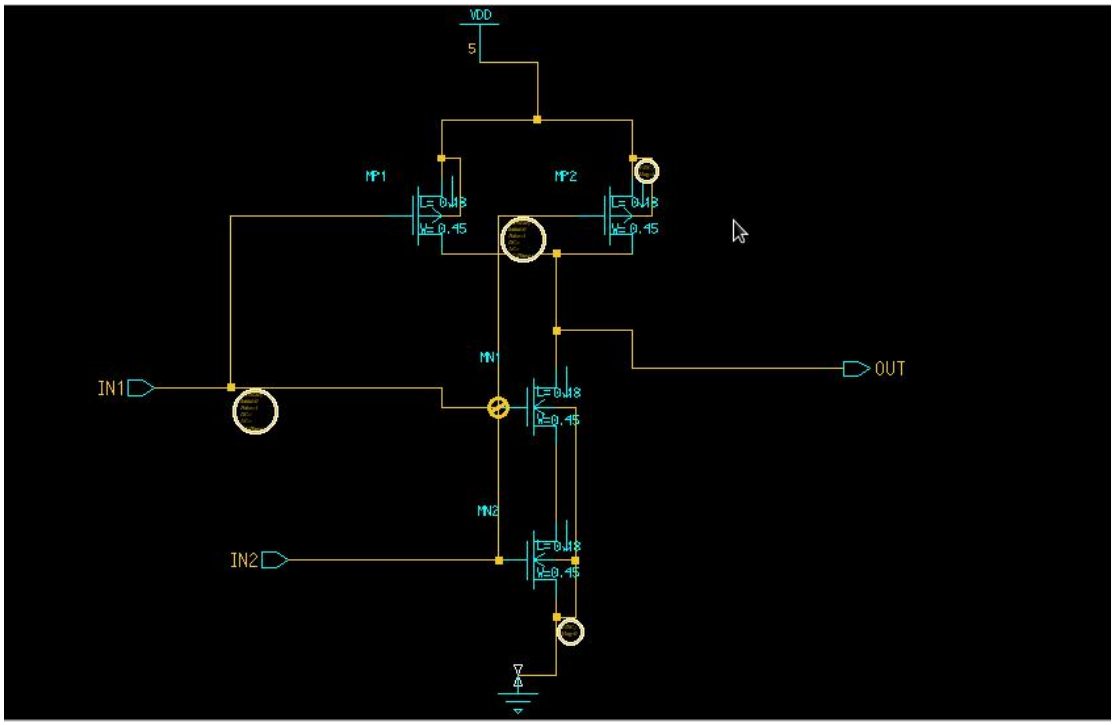


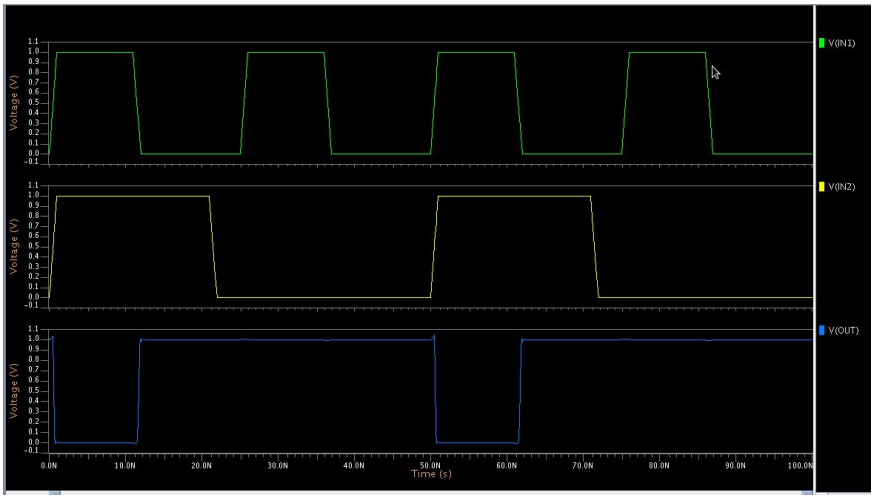
Figure 1 : Schematic of NAND logic using CMOS technology

The above figure shows a NAND gate made using NMOS and PMOS transistors (CMOS Technology). It consists of **2 NMOS connected in series**, together forming the Pull Down part of the logic function along with **2 PMOS connected in parallel**, together forming the Pull Up part of the logic function. IN1 and IN2 are the 2 inputs to the NAND gate and OUT is the output. All transistors are made using **tsmc 0.18um technology** with the **width = 0.27um** and **length = 0.18um**. The supply voltage is given at a constant **DC of 1.8V** magnitude and IN1 and IN2 are given **Pulses of peak voltage 1.8V** with the **time period of IN2 twice that of IN1**.

Expected Behaviour of NAND :

0 0 : 1
0 1 : 0
1 0 : 0
1 1 : 0

TRANSIENT ANALYSIS OF NAND SCHEMATIC:



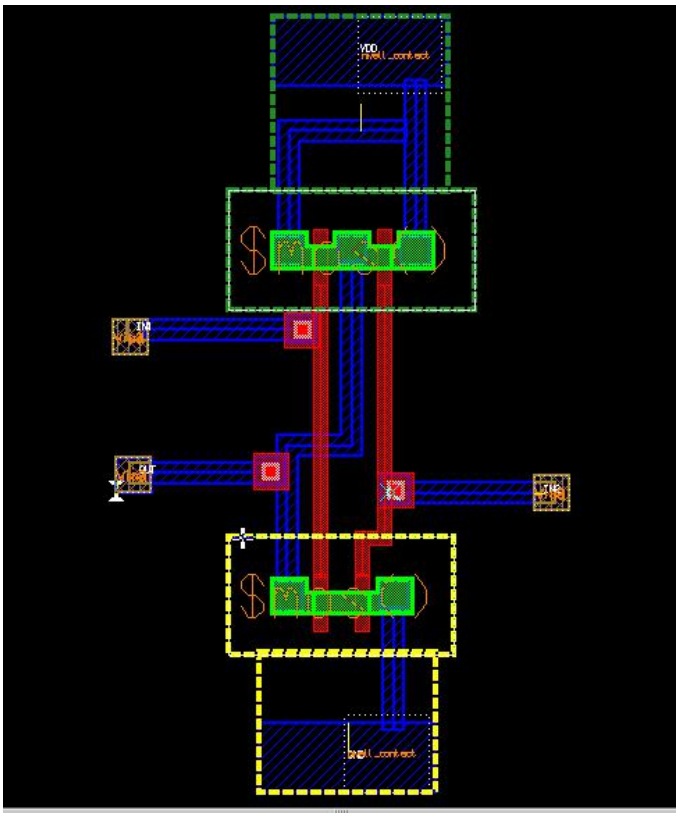
Observation: It is seen that the simulation matches with the expected behaviour of NAND logic.

Using the schematic of the NAND gate we create a layout of the NAND from the existing viewpoint of the schematic using the Pyxis Mentor Graphics Software.

LAYOUT OF NAND GATE:

After building the layout from the existing schematic and connecting the different MOS's, the layout on the right is generated. Then we connect ports IN1, IN2, OUT, VDD and GND to the layout.

We next check if the layout complies with the rules of 0.18um technology by proceeding with the various steps required in layout verification and extraction.



LAYOUT VERIFICATION AND EXTRACTION

Design Rule Check (DRC)

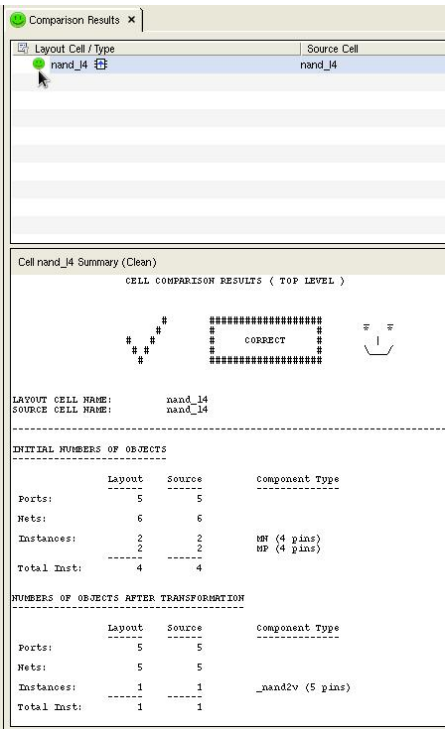
The first stage in layout verification is to check whether the different materials are built to the specifications of 018um technology. This is done by using the DRC tool provided by Pyxis.

DRC has three essential types of rules:

1. Spacing: The minimum distance between materials of different types that must be maintained is checked
2. Width: The specified width of different materials such as metal or poly is checked
3. Enclosure: When a object must be overlapped by another (ex: via and port) , it is checked whether a minimum specified margin exists or not.

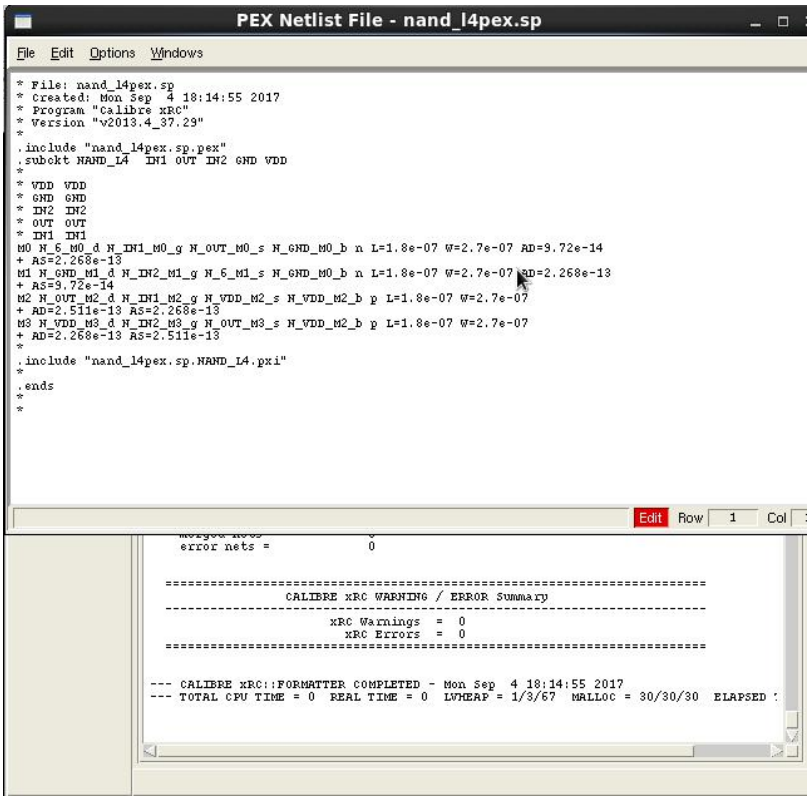
Layout Versus Schematic (LVS)

In the LVS stage the netlist originally generated from the schematic is compared with the netlist that is generated from the layout using a runset that has the relevant rules with respect to 0.18um technology to find any discrepancies.



Parasitic Extraction Analysis (PEX):

We use the PEX tool provided by the Calibre library to extract the parasitic capacitances, resistances and inductances in the circuit. Once the netlist from the PEX tool has been generated, we can run the simulation.

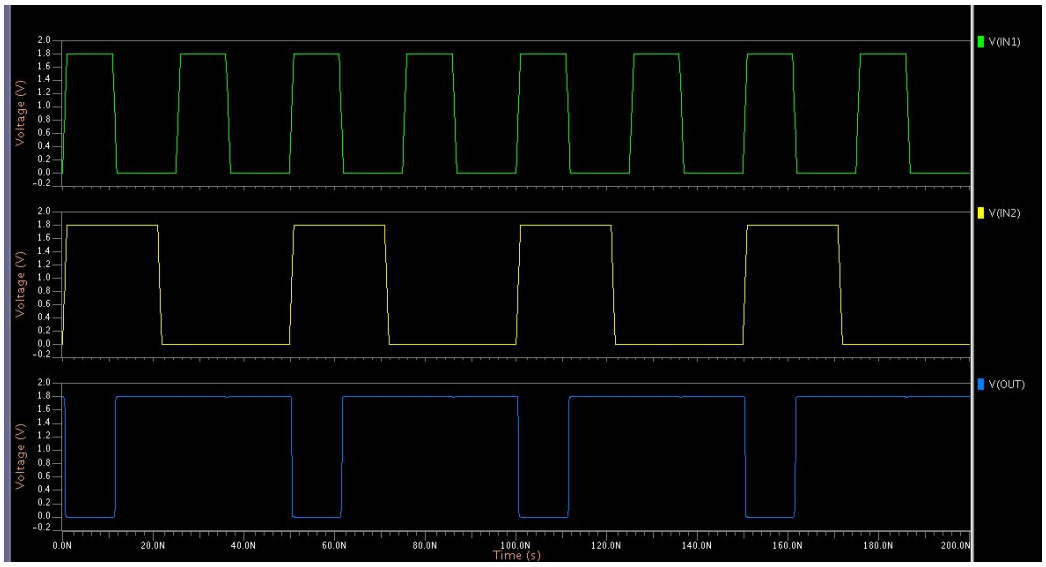


NGSPICE SIMULATION WITH ELDO AND WAVEFORM VIEWING WITH EZWAVE:

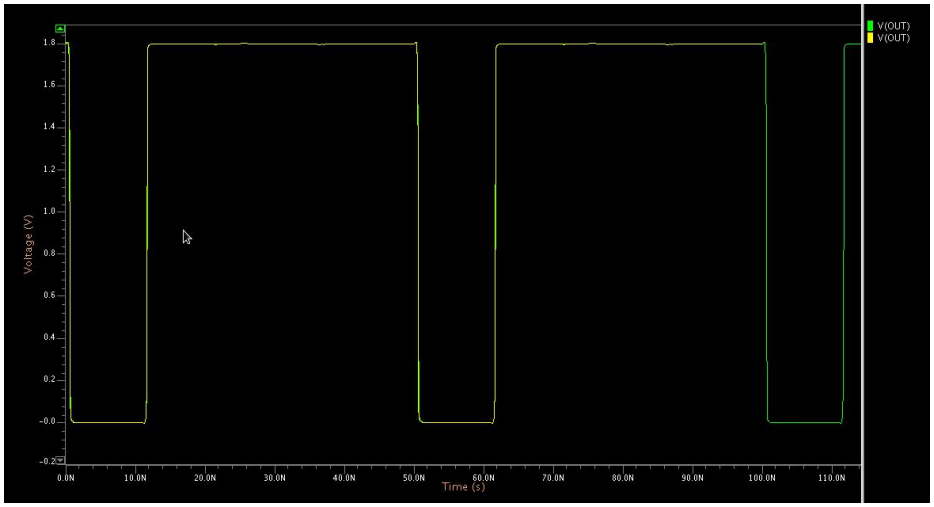
Then we write a ngspice code to run the netlist generated from the PEX analysis. Once ELDO is used to run the simulation, the tool EZWAVE is used to view the waveforms.

```
.lib $ADK/technology/ic/models/tsmc018.mod

.include 'nand_l4pex.sp'


.global vdd gnd
vforce vdd gnd dc 1.8
.connect gnd 0
.option post

v1 in1 gnd pulse(0 1.8 0 1n 1n 10n 25n)
v2 in2 gnd pulse(0 1.8 0 1n 1n 20n 50n)
X1 in1 out in2 gnd vdd NAND_L4

.tran 0.001n 200n
.print v(out)
```

Simulation results of the layout. The first 2 waves are the two inputs and the third wave is the NANDed output:



We then check whether the waveform generated by the schematic matches the waveform generated by the layout.



Conclusions and Precautions:

1. During the construction of the layout, we must take care that the distance between non-contact metals is greater than 3L and that the distance between non-contact polysilicon should also be greater than 3L to pass the DRC check.

2. For LVS analysis, it isnt possible to change the netlist of the layout as that gets generated on running the tool, therefore all discrepancies in the

LVS report must be addressed by changing the netlist of the schematic.

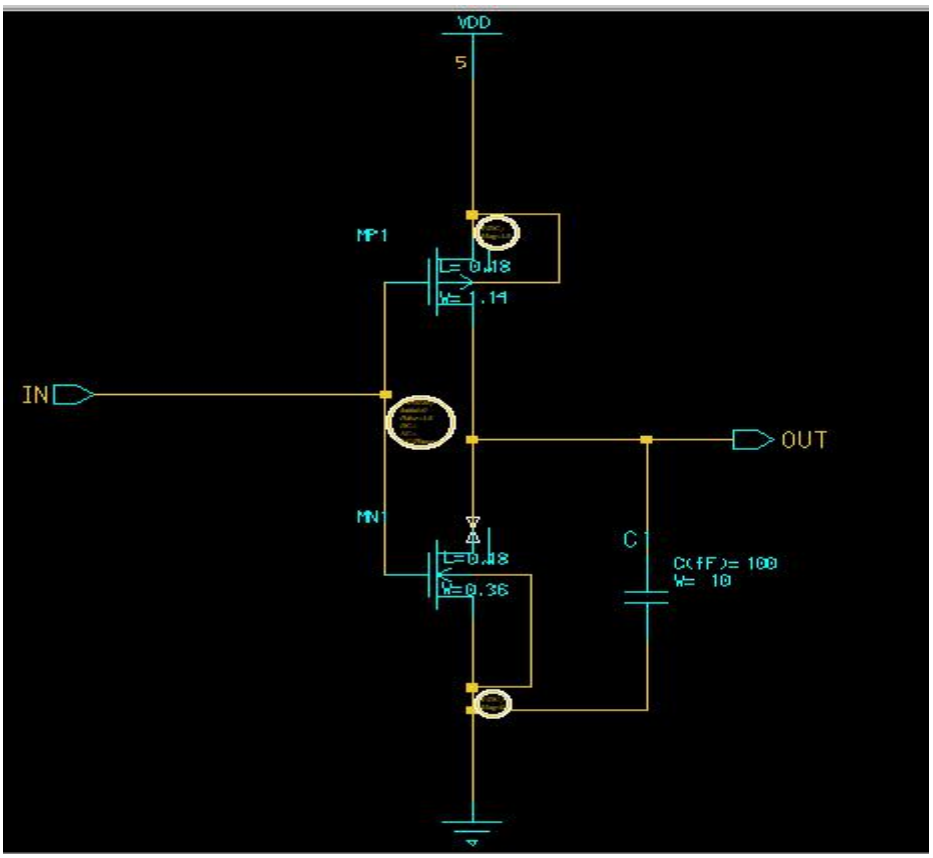
3. It has successfully demonstrated that the layout of the NAND gate generated exhibits NAND behaviour and matches the specifications of the schematic as it has passed LVS and DRC checks.

4. The performance of the layout and schematic are similar as shown from the ELDO simulated waveforms of both the schematic and the layout.

5. One drawback of using the viewpoint of the schematic to generate the layout is that the MOS sizes cannot be changed. This issue can be addressed by generating the layout from scratch.

PART B: Design the layout of an inverter from scratch

SCHEMATIC OF NOT GATE AND CIRCUIT DESCRIPTION

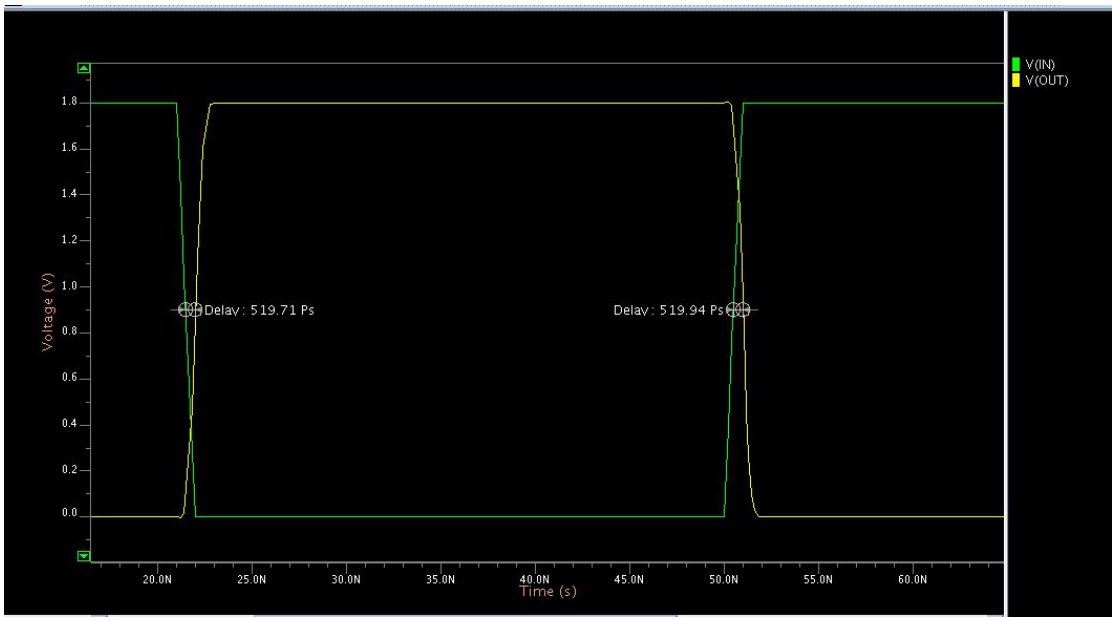


Above is the schematic of the inverter. It consists of an NMOS and PMOS connected in cascade with a common gate input and output connected to the drain of the both transistors. **Tsmc 0.18um technology** is used for the transistors. In order to achieve the same delays(i.e, tphl and tplh are equal), the width and length of the NMOS and PMOS were designed specifically

PMOS : W = 1.14um L = 0.18um
NMOS : W = 0.36um L = 0.18um

A constant DC supply of 1.8V was given and a pulsed input with peak value 1.8V was used as input

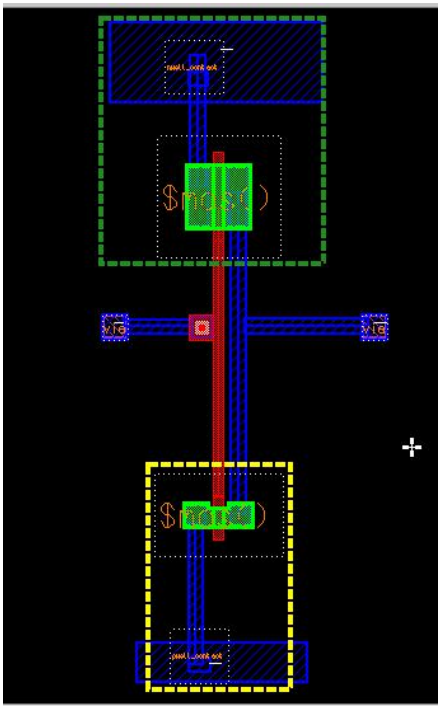
SIMULATION OUTPUT WITH THE I/O WAVEFORMS OVERLAID



As seen the delays of tphl and tplh are approximately equal hence satisfying the design requirement.
TPHL = 519.94Ps
TPLH = 519.71Ps

LAYOUT DESIGN AFTER DRC

The layout was designed and DRC tool was used to locate the errors after which the following layout was created:

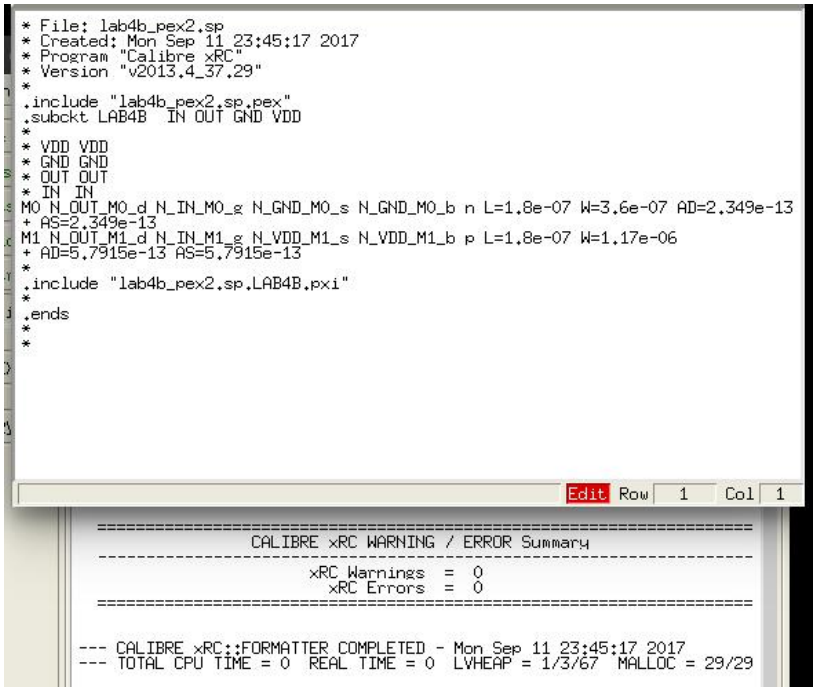


Note: DRC completed. Total RuleChecks: 91; Total Results: 0; Total Original Geometries: 54; CPU Time: 0.04, REAL Time: 0.074713.

LAYOUT VERIFICATION AND SIMULATION

PEX

Using PEX analysis as before the netlist containing the parasitic resistances, capacitances and inductances was generated using which the simulation can be run.



```
* File: lab4b_pex2.sp
* Created: Mon Sep 11 23:45:17 2017
* Program "Calibre xRC"
* Version "v2013.4_37.29"
*
.include "lab4b_pex2.sp.pex"
.subckt LAB4B  IN OUT GND VDD
*
* VDD VDD
* GND GND
* OUT OUT
* IN  IN
M0 N_OUT_M0_d N_IN_M0_g N_GND_M0_s N_GND_M0_b n L=1.8e-07 W=3.6e-07 AD=2.349e-13
+ AS=2.349e-13
M1 N_OUT_M1_d N_IN_M1_g N_VDD_M1_s N_VDD_M1_b p L=1.8e-07 W=1.17e-06
+ AD=5.7915e-13 AS=5.7915e-13
*
.include "lab4b_pex2.sp.LAB4B.pxi"
*
.ends
*
*
```

Edit Row 1 Col 1

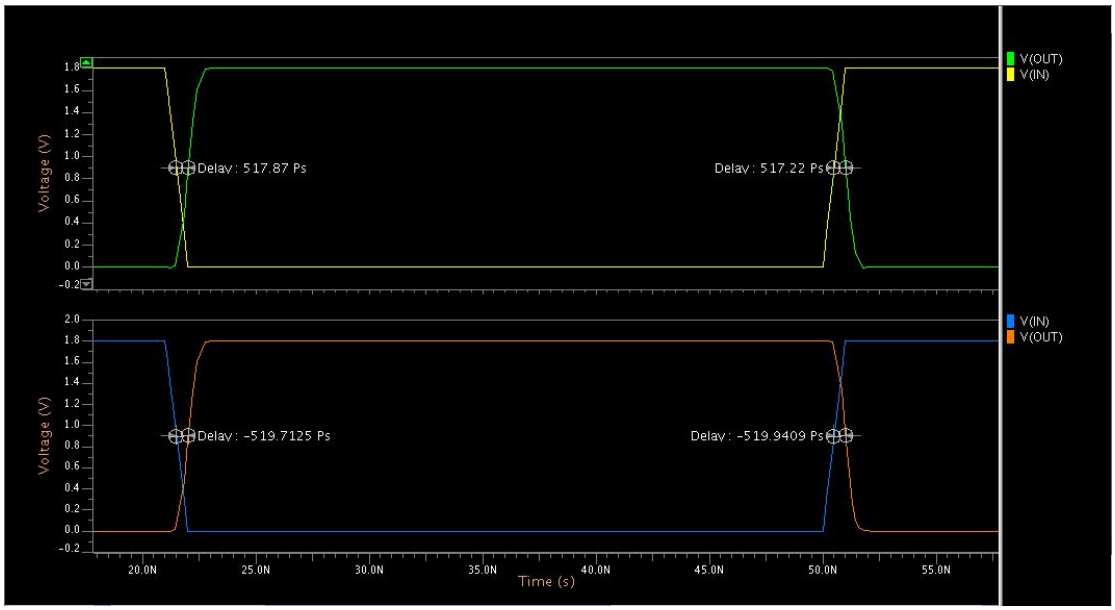
```
==================================================================
                CALIBRE xRC WARNING / ERROR Summary
------------------------------------------------------------------
                      xRC Warnings  =  0
                        xRC Errors  =  0
==================================================================


--- CALIBRE xRC::FORMATTER COMPLETED - Mon Sep 11 23:45:17 2017
--- TOTAL CPU TIME = 0  REAL TIME = 0  LVHEAP = 1/3/67  MALLOC = 29/29
```

ELDO SIMULATION AND EZWAVE

An ngspice code to simulate the generated layout using the PEX tool's subcircuit file was made as shown beside:

```
.lib $ADK/technology/ic/models/tsmc018.mod

.global vdd gnd
vforce_vdd vdd gnd 1.8
.connect gnd 0
.option post

.include 'lab4b_pex.sp'

cap out gnd 100FF
v1 in gnd pulse(0 1.8 0 1n 1n 20n 50n)
X1 in out gnd vdd LAB4B

.tran 0 100n
.print tran v(out)
```

Using the EZWAVE tool the output waveform was simulated and the delays were calculated by adding an additional capacitor of 100fF in between the output and the
ground.



As seen, the first pair of waveforms is generated by the layout and the second pair is generated by the schematic.

Delay (TPHL and TPLH) of the layout inverter are:
TPHL = 517.22Ps
TPLH = 517.87Ps

CONCLUSIONS

1) The delay observed by the layout is slightly lower than that of the schematic. A difference of 2Ps was observed, although between tphl and tplh a difference of less than 1Ps was observed in both cases.

2) The inverter layout from scratch was shown to demonstrate an inverting characteristic as expected and also satisfies the design requirement of having equal tphl and tplh delays.

3) The W of PMOS was 3-3.5 times the W of NMOS to achieve equal delays, which is the expected range from the plot of delay vs transistor ratio.