libreChainEDA

A design for reuse environment
FOSS EDA tool flow scripting project

Free opensourced toolkit for creating IP-Xact based Soc Designs

Concept to programmed FPGA with NO proprietary Software

Supported Opensource EDA Tools

FUSESOC	package manager	KACTUS2	Design Entry
ICARUS	verilog Simulation	VERILATOR	verilog Simulation
COVERED	Code coverage	SOCGEN	IP-Xact utilities
VERILOG-PERL	utilities	YOSYS	Synthesys
ARACHE-PNR	Place and Route	ICESTORM	Fpga creation
FIZZIM	State Machine Design		

System Admistration Support

One stop shopping for all supported tools

Tested and working install scripts

App notes and videos (Real Soon Now)

Design for Reuse Methodologies

W Edwards Demming inspired process control

Coding and Packaging Standards

Correct by Construction Methodology

FPGA Demo Board Support

Nexys2 Digilent Icestick Lattice Semiconductor DE0 nano Board

Alpha Code github.com /ouabache/fossi
Discussion discussion@lists.librecores.org