SOCGEN: Design for Reuse Toolset

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Abstract

Effective design for reuse requires that there is a clear understanding between the component designer and the SOC architect as to exactly what will be delivered to the System-on-chip (SOC). This paper introduces the socgen project.It is a design for reuse toolset that enables the component designer to create and verify their modules and then deliver them to the architects in a package that is easily added into any SOC. Socgen is a free opensource project that is available from the opencores.org site. It includes several demonstration projects that show how an IP-Xact enabled toolset can build the multiple views and codesets needed in todays complex designs. IP-Xact componentGenerators are used to run both socgen scripts that generate registers and verilog files as well as external tools such as the fizzim finite state machine tool.

The project includes a simulation toolflow that uses icarus verilog for simulation, verilator for linting and covered for code coverage. It shows how to use IP-Xact to create testbenches and use them in the myriad of different combinations needed to verify a component with all its variants. A synthesys toolflow using Xilinx ISE webpack can compile the designs and target them for several different fpga demo boards.

Socgen will create a packaged component complete with documentation and a unit test suite that can be easily delivered to an chip design team and inserted using an IP-Xact enabled toolflow.

The example rtl included with the socgen project consists of other selected opencores.org projects that were reworked by adding IP-Xact files and upgrading the code to meet modern design for reuse standards. They also include low level libraries, testbench bus functional models and bus definitions that provide the basis for easily sharing ip between different groups.

1.0 Introduction

Once upon a time Sytem designers designed printed circuit boards. These boards were stuffed with hundreds of different components that you purchased through distributers and each one came with a datasheet that the system designer would use to understand the part and how to config and interconnect it into their design. All datasheets followed the same format. The front page contained the name and part numbers of the component and its variants. You had a graphic showing all the exterior connections along with an explanation of what the signals did. There were sections for the absolute maximun ratings and timing requirements that all uses the same nomenclature.

Somehow in our conversion from PCB system design into a internal IC system design we forgot about datsheets. Todays datasheet for an IP component is a free form document in which the component designer details everything that they think that the architects will need to know. There is no industry wide standard detailing exactly what goes into a IP datasheet and how to present it. Todays system designers are faced with hundreds of components each documented in their own unique way. Are we surprised that trying to use other designers components is a slow process?

Futhermore todays component designers have missed one of the biggest changes that has swept this industry in the last 30 years. Todays component designer does not create a datasheet for the system designers to read. Today the component designers tool flow creates the datasheet for the system designers tool flow to parse. IP-Xact defines a xml schema that details exactly what the component designer must deliver with their IP so that the system designers can easily configure and interconnect it in their chip.

Socgen is demonstration project that provides an IP-Xact enabled tool chain capable of doing full asic/fpga designs

Project Directory

A project is a collection o.

Component Directory

Author & Contact Information

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