

# libreChainEDA Project:

# **Design for Reuse Tool Flow Scripting**

Every IC Design team uses scripts as the "glue" to bind together all of the Hardware and Software IP with the different EDA tools. These scripts create and manage the build environment and run all of the EDA tools in their proper order.

These scripts are the ideal open source project. Everybody needs to do basically the same operations and by working with other designers you can jump start your own efforts and start off with tested and working design scripts.

LibreChainEDA has put together a portfolio of over a dozen FOSS EDA tools into an easy to install package along with sample designs with simulations and FPGA synthesys.

These scripts can be used with your own designs or extended to add new tools as needed.

LibreChainEDA provides One stop shopping with install scripts and mirrored copies of the tools in one simple download.

Alpha code is available on github.com/ouabache/fossi

Discussion and Information discussion@librecores.org

My Email is <u>z3qmtr45@gmail.com</u>

John Eaton

### **Supported Tools**



## Kactus2 Version 3.2.35 <u>sourceforge.net/projects/kactus2/</u>

Kactus2 is a gui based design tool that can enter or modify hardware IP modules.It supports IP-Xact 1685-2014 design files.

#### Fusesoc Version 1.5 github.com/olofk

Fusesoc is a package manager that can fetch component IP from a IP host server such as opencores.org or github.com. It can also run tool flow scripts from the command line.

## Socgen Version 1.0.0 <u>sourceforge.net/projects/socgen/</u>

Socgen is a package of scripts for processing IP-Xact files and running IP-Xact componentGenertors.



## Icarus verilog Version 10 iverilog.icarus.com/

Icarus verilog is a semi complete verilog only simulator

## Verilator Version 3.886 <a href="https://www.veripool.org/projects/verilator/wiki/Installing">www.veripool.org/projects/verilator/wiki/Installing</a>

Verilator is a verilog simulator that is limited to synthesize able only verilog.

## Verilog-perl Version 3.418 <u>www.veripool.org/wiki/</u>verilog-perl

Verilog-perl provides some very useful support utilites.

#### Gtkwave Version 3.3.76 <a href="mailto:gtkwave.sourceforge.net/">gtkwave.sourceforge.net/</a>

Gtkwave is a VCD file wave viewer for simulations.

### **Covered Version 0.7.10 <u>covered.sourceforge.net</u>**

Covered is a VCD file analyzer that provides code coverage metrics for simulations.

### Yosys version 0.6 www.clifford.at/yosys/

Yosys is a HDL synthesizer.

## Arachne-PNR version 0.0 www.clifford.at/arachne-pnr/

Arachhne-pnr performs place and route for fpgas

#### ICE Storm version 0.0 www.clifford.at/icestorm/

Ice Storm creates programming files for fpgas

#### Fizzim version 5.20 www.fizzim.com/

Fizzim uses graphical entry for state machines.

# ${\bf Libre Chain EDA\ Supported\ Development\ Boards}$

Digilent Nexys2 Lattice IceStick DE0\_nano

#### **Installation for Ubuntu**

sudo apt-get install git

download libreChainEDA repo from github.com and install Ubuntu app store tools and local tools

```
ouabache@ouabache: ~/github.com/ouabache/fossi/tools
ouabache@ouabache:~$ cd github.com/
ouabache@ouabache:~/github.com$ mkdir ouabache
ouabache@ouabache:~/github.com$ cd ouabache/
ouabache@ouabache:~/github.com/ouabache$ git clone http://github.com/ouabache/fossi
Cloning into 'fossi'...
remote: Counting objects: 13571, done.
remote: Compressing objects: 100% (326/326), done.
remote: Total 13571 (delta 178), reused 0 (delta 0), pack-reused 13228
Receiving objects: 100% (13571/13571), 203.98 MiB | 901.00 KiB/s, done.
Resolving deltas: 100% (6174/6174), done.
Checking connectivity... done.
Checking out files: 100% (12466/12466), done.
ouabache@ouabache:~/github.com/ouabache$ cd fossi/install/Ubuntu/
ouabache@ouabache:~/github.com/ouabache/fossi/install/Ubuntu$ sudo ls -la
[sudo] password for ouabache:
total 16
drwxrwxr-x 2 ouabache ouabache 4096 Nov 7 09:08 .
drwxrwxr-x 3 ouabache ouabache 4096 Nov 7 09:08 .
                                          7 09:08 ..
-rw-rw-r-- 1 ouabache ouabache 2297 Nov 7 09:08 Makefile
-rw-rw-r-- 1 ouabache ouabache 48 Nov 7 09:08 readme.txt
ouabache@ouabache:~/github.com/ouabache/fossi/install/Ubuntu$ make > logfile.txt
ouabache@ouabache:~/github.com/ouabache/fossi/install/Ubuntu$ cd ../../tools/
ouabache@ouabache:~/github.com/ouabache/fossi/tools$ sudo ./install_all > logfile.txt
The directory '/home/ouabache/.cache/pip/http' or its parent directory is not owned by the current us
er and the cache has been disabled. Please check the permissions and owner of that directory. If exec
uting pip with sudo, you may want sudo's -H flag.
The directory '/home/ouabache/.cache/pip' or its parent directory is not owned by the current user an
d caching wheels has been disabled. check the permissions and owner of that directory. If executing p
ip with sudo, you may want sudo's -H flag.
You are using pip version 8.1.1, however version 9.0.1 is available.
You should consider upgrading via the 'pip install --upgrade pip' command.
```

Check logfile for completion.

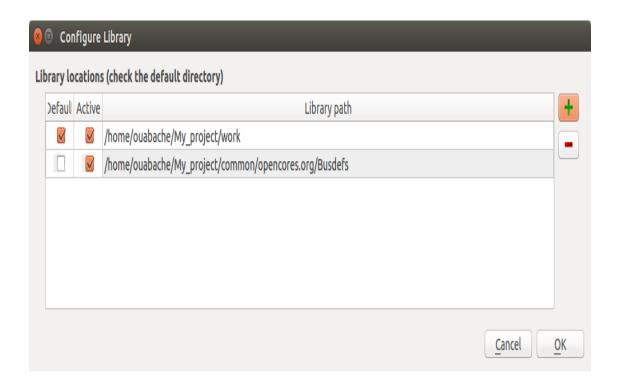
Create a development area:

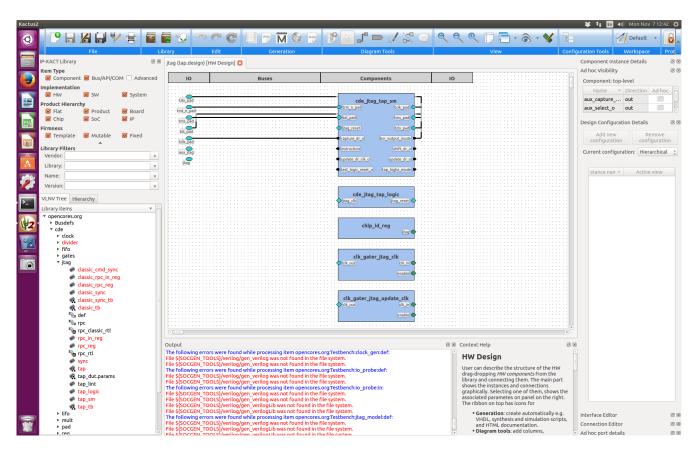
```
cp -r ~/github.com/ouabache/fossi/DESIGN ~/My_Project cd My_Project
```

Run a fusesoc and socgen demo test. Each flow will run a test simulation and display the dumpfile.

```
./test_fusesoc <= run a fusesoc demo
./test_socgen <= run a socgen demo
```

Run Kactus2 and set up the libraries. You will then have access to the socgen sample files.





Run gschem schematic capture. You will have access to the socgen demo modules.

