SOCGEN Design Environment

SOCGEN is a complete EDA design environment that simplifies the creation of component IP and makes it easy to integrate it into a System-on-Chip (SOC). Its tool set uses IP-xact files to build and re-target a complete SOC. It is designed to create complex designs from components sourced from a variety of different designers. It is free ,open sourced and available from opencores.org.

Installation

```
%>  svn co -user <UserName> -passwd <Password>  opencores.org/ocsvn/socgen/socgen/trunk    socgen
```

Install tools from socgen/tools/install and Xilinx webpack

%>make workspace	Creates temporary work area isolated from repositories
%>make build_hw	Builds all verilog code, filelists and tool setups
%>make build_obj	Builds obj code for all firmware
%>make build_sw	Links all firmware code
%>make run_sims	Runs lint checks , verilog test suites and code coverage
%>make build fpgas	Synthesizes Xilinx fpgas
%>make check_sims	Report sims results
%>make check_fpgas	Report synth results

Features

Separate workspace keeps generated files out of source repositories
IP-Xact based tool flow promoting easy exchange of ip
Correct by construction design methodology
Separate design view for each tool flow
Easy to re-target designs into different processes
Builds verilog files from ip-xact descriptions
Prevents name collisions from modules and `macros
Packages each component into a single library file
Eliminates search paths
Supports IP-Xact bus definitions
Builds testbenches from ip-xact descriptions

Tool flows

Icarus verilog simulations
Code coverage using covered
Rtl checking using verilator
Synthesys using Xilinx webpack
Waveform viewing using gtkwave
Finite state machines with fizzim
Control and status register generator

Projects and Libraries

RTL code examples from opencores projects (Three embedded microcomputers with led,switch,uart ,video and ps2 interfaces)
Sample library for non-synthesizable macros (pads,srams,pll's etc)
Basic Testbench bus functional models (clock and reset gen, uart etc)
IP-xact busDefinition examples (clock,reset,microbus,pads)
Sample fpgas for digilent Nexys2 and Basys boards

Further Information

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