Fossi-Foundation EDA Standards

libreChainEDA
User Manual

3 Sep 2016

Manifesto

The four different classes of intellectual property(IP) in the Electronic Design Automation (EDA) world are Hardware,Software ,Tools and Tool Flows. The software world has made great strides in the availability of open sourced IP. Hardware and Tool IP are starting to become more readily available but remain about 10 to 20 years behind the software world.

LibreChainEDA is a program by the fossi-foundation to create and support a completely open sourced EDA tool flow. The program goals are to:

1) Identify a set of open sourced EDA tools to be supported under this program.

2) Provide system administration support over the internet to all users

Create install scripts for all major linux distros.

Provide mirrors for all tool installs from one location

Work with the tool design teams to provide tool installs from major linux app servers (ex: Ubuntu)

Work with the tool design teams to identify and fill needs in open sourced tools.

3) Create a packaging and coding guidelines document for hardware IP designers.

4) Create a document for tool smiths of best practices for EDA tool design.

LibreChainEDA Is/Is Not list.

LibreChainEDA is designed to meet the needs of a professional IC design team. It may be used for FPGA design as well but all flows will be suitable for use by IC design teams

All IP will conform to the IP-Xact 1685-2014 packaging standard. A set of vendorExtensions will be created to augment the standard where needed.

All work will be licensed under ?????????????????????????? All libreChainEDA will be open source non-commercial but there are no restrictions on using libreChainEDA to create commercial designs.

All flows will be completely automated with no human intervention required

Tool flows will be designed for parallel execution where ever possible.

Tool flows will be self checking and fatal errors will not be buried deep in some log file.

LibreChainEDA Supported Tools

kactus2

Version 3.1.2

sourceforge.net/projects/kactus2/

fusesoc

Version 1.5

github.com/olofk

icarus verilog

Version 10

iverilog.icarus.com/

`github.com/steveicarus/iverilog.git`

verilator

Version 3.886

www.veripool.org/projects/verilator/wiki/Installing

Most engineers will spend their entire career without ever encountering a problem that is so new that it has never been seen before now. Some of our problems are so old that their original names are in Latin.

ghdl

Version 0.29.1

`ghdl.free.fr/site/pmwiki.php?n=Main.Download`

gtkwave

Version 3.3.76

gtkwave.sourceforge.net/

covered

Version 0.7.10

covered.sourceforge.net

yosys

version 0.6

www.clifford.at/yosys/

ICE Storm

Version
www.clifford.at/icestorm/

Xilinx Webpack

Version 14.7

www.xilinx.com/products/design-tools/ise-design-suite/ise-webpack.html

Altera quatrus prime lite

Version 16.0

www.altera.com/downloads/download-center.html

LibreChainEDA Supported Development Boards

After a System-on-chip design is created it will then be retargeted into any number of FPGA or ASIC designs. The pad ring module for a design targeted into a FPGA development board will be almost identical to any other SOC design targeted to that same board. Only the module names and parameters will be different.

LibreChainEDA will maintain template designs for the most popular FPGA development boards in order to vacillate retargeting designs to other boards.

Supported boards are

Digilent Nexys2

DE0_nano

Introduction

Eda tool flows are all the various scripts and utilities that set up and run all of the EDA tools needed to build and test a System-on-chip SOC design. Tool flows are initiated by the user from the command line and terminate by creating a tool command line and executing it. The only EDA tools that are run under a Graphics User Interface (GUI) are those tasks that are usually only run one time such as design entry or debugging. Any task that must be rerun every time anything is changed must be run from the command line.

Most EDA tool flows used in the industry are a joke. Makefiles calling perl scripts calling EDA tools and then calling SED a few times to fix an output file. Then you hack the whole thing to run recursively.

Some companies have dedicated teams to design, test and support these tool flows but these companies tend to have internal IC fabs and lots of design starts. They get advanced notice for all new IC processes and can design and test these scripts long before they are needed for any real IC designs.

Companies without their own fabs must select and partner with an IC silicon design house in order to design an ASIC. Both teams come to the initial kickoff meeting without ever having seen any of the other teams requirements. If you are the first chip on a new process node then the silicon design house engineers may be seeing their own requirements for the first time.

There is zero time in the schedule to design and test any new tool flow scripts. You have to do that on the actual ASIC that you are designing. The ASIC is the #1 priority for both teams so tool flow design and testing usually only gets the bare minimum of needed resources.

LibreChainEDA is a program designed to harness the power of open source to create a powerful collection of EDA tool flows and make then available to all designers in the industry for ASIC and FPGA designs.