SOCGEN A design for reuse environment

Free opensourced toolkit and libraries for creating SoC designs

Available on opencores.org [Project: socgen]

IP−Xact based toolflow promoting easy exchange of ip between users

Correct by construction design methodology

Separate design view for each toolflow

Easy to retarget designs into different processes

Builds verilog files from ip−xact descriptions

Prevents name space collisions from module names and verilog ‘(tic) macros

Packages each component into single library file

Eliminates search paths

Supports IP−Xact bus definitions

Icarus verilog simulation suites

RTL checking using Verilator

Fizzim State Machine tool

Code Coverage using Covered

Synthesys using Xilinx WebPack

Control and status register generator

```
SOCGEN
    DOC
    TOOLS
        BIN
        INSTALL
    PROJECTS
        VENDOR1
            LIBRARY1
                IP
                  COMPONENT
                SW
                  PROGRAM
    WORK
```

```
WORK
    LIBRARY
        IP
          COMPONENT
            IP−XACT
            RTL
                XML
                    COMP_VER_CFG.XML
                    COMP_VER_CFG.DESIGN.XML
                VERILOG
                VIEWS
                 FSM
            SIM
                XML
                   COMP_VER_TB
                ICARUS
                   COMP_VER_CFG_TEST
                COV
                   COMP_VER_TB
                LINT
                   COMP_VER_TB
                VERILOG

            SYN
                ISE
                   COMP_VER_CFG

    CHILDREN
            LIBRARY
```