SOCGEN

A design for reuse environment

Free opensourced toolkit and libraries for creating SoC designs

Available on opencores.org

IP−Xact based toolflow promoting easy exchange of ip

Correct by construction design methodology

Separate design view for each toolflow

Easy to retarget designs into different processes

Builds verilog files from ip−xact descriptions

Prevents name collisions from modules and ‘macros

Packages each component into single library file

Eliminates search paths

Supports IP−Xact bus definitions

Icarus verilog simulations

Code coverage using covered

Rtl checking using verilator

Synthesys using Xilinx webpack

Waveform viewing using gtkwave

Finite state machines with fizzim

Control and status register generator