FuseSoC Documentation

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FuseSoC is a package manager and a set of build tools for HDL (Hardware Description Language) code.

Its main purpose is to increase reuse of IP (Intellectual Property) cores and be an aid for creating, building and simulating SoC solutions.

The package manager part can be seen as an apt, portage, yum, dnf, pacman for FPGA (Field-Programmable Gate Array)/ASIC (Application-Specific Integrated Circuit) IP cores. A simple ini file describes mainly which files the IP core contains, which other IP cores it depends on and where FuseSoC shall fetch the code.

A collection of cores together with a top-level is called a system, and systems can be simulated or passed through the FPGA vendor tools to build a loadable FPGA image.

Currently FuseSoc supports simulations with ModelSim, Icarus Verilog, Verilator, Isim and Xsim. It also supports building FPGA images with Xilinx ISE, Xilinx Vivado and Altera Quartus.

FuseSoC itself does not contain any actual hardware cores, but instead is configured to look them up in your filesystem.

The main documentation for users is found in the *User Documentation*. If you are a developer of a hardware core or a system-on-chip, the *Core Documentation* are your starting point.

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