Han-Mo Ou

PhD Candidate

411 Coordinated Science Laboratory (CSL), 1308 W Main St, Urbana, IL 61801

hanmoou2@illinois.edu | hanmo-ou

Education

University of Illinois at Urbana-Champaign *Urbana, IL*

PhD Candidate, Electrical and Computer Engineering *August 2020 - present*

- Adviser: Prof. Naresh R. Shanbhag
- **Research Focus: High Speed and Energy Efficient VLSI Implementations for Communications/Connectivity**
- Completed Coursework: Optical Communication Systems, Digital IC Design, Analog IC Design, Introduction to Optimization, Numerical Analysis, Random Processes, Pattern Recognition, Digital Signal Processing II, Statistical Inference, Advanced Digital Communications, Information Theory, Deep Learning in Hardware, Broadband Wireline Circuits
- GPA: 4.00/4.0

University of Illinois at Urbana-Champaign *Urbana, IL*

MS, Electrical and Computer Engineering *August 2020 - August 2022*

- Adviser: Prof. Naresh R. Shanbhag
- **Research Focus: Error Compensation for In-memory Computing Architectures**
- Thesis Title: Signal Processing Methods to Enhance the Accuracy of MRAM-based In-memory Architectures
- GPA: 4.00/4.0

National Taiwan University *Taipei, Taiwan*

BS in Engineering, Electrical Engineering *September 2016 - June 2020*

- **Research Focus: Machine Learning for Communications**
- Research Adviser: Prof. An-Yeu (Andy) Wu
- GPA: 4.22/4.3 (3.99/4.0)
- Class Rank: 10th/177

Research Projects

Quantum Control Hardware Design *Yorktown Heights, NY*

IBM Research (Summer Internship) *2024*

- Worked on VLSI for qubit control

Forward Error Correction for Connectivity (CICC'25) *Urbana, IL*

University of Illinois at Urbana-Champaign *2023-present*

- Investigating the feasibility of using forward error correction in connectivity applications
- Implemented and taped-out baseline BCH decoder characterization chip in Intel16 process

Statistical Compensation for In-Memory Computing (ICASSP'23, JSSC'24) *Urbana, IL*

University of Illinois at Urbana-Champaign *2020-2023*

- Devised statistical compensation methods for non-idealities in resistive in-memory architectures
- Implemented method in 22nm process and integrated with MRAM-based IMC core

Machine Learning-based Equlization and Decoding Methods (MLSP'20) *Taipei, Taiwan*

National Taiwan University *2019-2020*

- Investigated the use of deep neural networks for communication systems to enhance end-to-end accuracy
- Applied neural network-aided Viterbi algorithm for joint equalization and decoding, enhancing coding gain

Teaching Experience

Fall 2022 **ECE 498 NSU/NSG Resource-efficient Machine Learning for the Edge**, Teaching Assistant *Urbana, IL*

Professional Experience

2024	**Quantum Hardware Research Intern**, IBM Research, Yorktown Heights, NY
2020-pres.	**Graduate Research Assistant**, Coordinated Science Laboratory, University of Illinois
2020-pres.	**Research Scholars Program**, Semiconductor Research Corporation
2022	**Graduate Teaching Assistant**, Electrical and Computer Engineering, University of Illinois
2019	**Software Engineering Intern**, Cadence Design Systems, Hsinchu, Taiwan

Publications

Journal Publications

Saion K. Roy, **Han-Mo Ou**, Mostafa G. Ahmed, Peter Deaville, Bonan Zhang, Naveen Verma, Pavan K. Hanumolu, and Naresh R. Shanbhag, "Compute SNDR-boosted 22nm MRAM-based In-Memory Computing Macro using Statistical Error Compensation," IEEE Journal of Solid-State Circuits (JSSC), 2024.

Conference Publications

Han-Mo Ou, Gene Lee, and Naresh R. Shanbhag, "Forward Error Correction Requirements for Data Center Connectivity," 2025 Custom Integrated Circuit Conference (CICC), Boston, MA.

Saion K. Roy, **Han-Mo Ou**, Mostafa G. Ahmed, Peter Deaville, Bonan Zhang, Naveen Verma, Pavan K. Hanumolu, and Naresh R. Shanbhag, "Compute SNR-boosted 22nm MRAM-based In-Memory Computing Macro using Statistical Error Compensation," 2023 European Conference on Solid-State Circuits (ESSCIRC), Lisbon, Portugal, 2023.

Han-Mo Ou and Naresh R. Shanbhag, "Enhancing the Accuracy of Resistive In-Memory Architectures using Adaptive Signal Processing," 2023 IEEE International Conference on Acoustics, Speech and Signal Processing (ICASSP), Rhodes Island, Greece, 2023, pp. 1-5.

Wen-Chiao Tsai, Chieh-Fang Teng, **Han-Mo Ou**, and An-Yeu (Andy) Wu, "Neural Network-Aided BCJR Algorithm for Joint Symbol Detection and Channel Decoding," 2020 IEEE Workshop on Signal Processing Systems (SiPS), Coimbra, Portugal, 2020, pp. 1-6.

Han-Mo Ou, Chieh-Fang Teng, Wen-Chiao Tsai, and An-Yeu (Andy) Wu, "A Neural Network-Aided Viterbi Receiver for Joint Equalization and Decoding," 2020 IEEE 30th International Workshop on Machine Learning for Signal Processing (MLSP), Espoo, Finland, 2020, pp. 1-6.

Chieh-Fang Teng, **Han-Mo Ou**, and An-Yeu (Andy) Wu, "Neural Network-based Equalizer by Utilizing Coding Gain in Advance," 2019 IEEE Global Conference on Signal and Information Processing (GlobalSIP), Ottawa, ON, Canada, 2019, pp. 1-5.

Skills

Programming	Verilog, Python (PyTorch), MATLAB, C++
EDA Tools	Design Compiler, Genus, Innovus, Virtuoso, HSPICE, Vivado
Tape-out Exp.	UMC 180nm, GlobalFoundries 22nm-FDSOI, Intel 16

Service, Awards, & Grants

2024	**Taiwan Study Abroad Fellowship**, Ministry of Education, Taiwan	*US$16,000*
2024	**Scholar Leadership Award**, Center for Ubiquitous Connectivity (CUbiC)	
2023	**Circuits and Systems Session Chair**, CSL Student Conference	
2023	**Conference Presentation Grant**, University of Illinois Graduate College	*US$250*
2020	**First Prize, Undergraduate Standard Cell, IC Design Contest**, Ministry of Education, Taiwan	
2019-2020	**Undergraduate Research Project Grant**, Ministry of Science and Technology, Taiwan	*US$1,600*
2019	**Third Prize, EE Undergraduate Innovation Award**, National Taiwan University	
2017	**Spring & Fall Academic Awards**, National Taiwan University	