Most frequented questions

This document is only meant for INE3 SESNum students and it is **strictly forbidden to share** it.
Sharing this would even lead to firing people from their jobs, or worse, having them sued .

Safran :

- Qu'est ce qu'un temps réel?
- Pourquoi travailler avec machine learning et non pas par simple comparaison?
- la différence entre une variable et un signal en vhdl
- testbench?
- FPGA / UVM / VERILOG

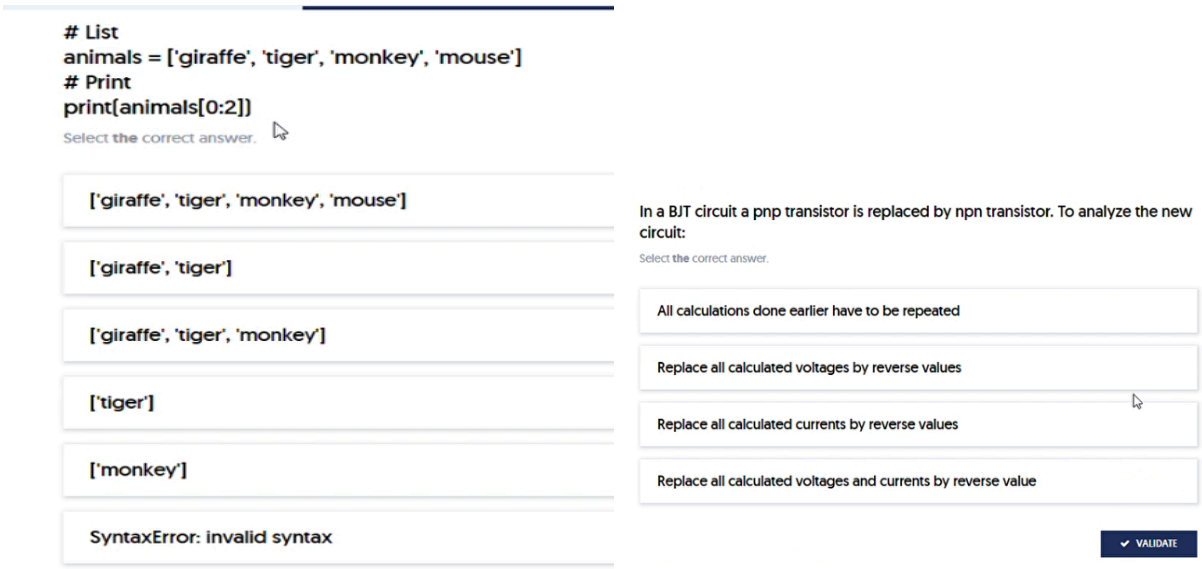
Alten :

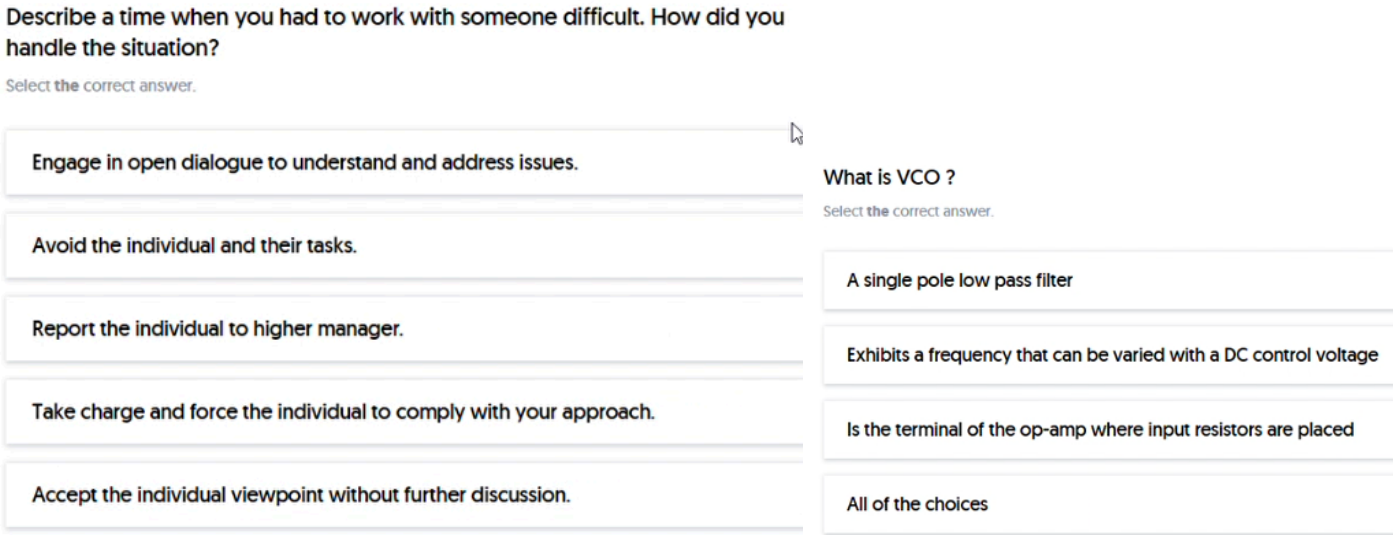
- Pour un composant important dans la voiture, utiliserez- vous Can ou LIN? Pourquoi?
- Connaissez-vous Matlab? La norme ISO26262? ASIL?
- C'est quoi le cycle V? Quelles sont ses étapes?
- Connaissez-vous Autosar?
- tests en C (comme dans le site sanfoundry)
- Quels sont les protocoles de communication que vous connaissez?
- Your motivation in English
- c'est quoi MDB?

- c’est quoi autosar? les couches de Autosar
- CANoe
- Les composants d'automobile
- C'est quoi une exigence ?

Sondrel : (3 rounds)

50 questions en 1 heure
(Images capturées from a screen recording)





```
ENTITY convert IS
PORT(b: IN STD_LOGIC_VECTOR(3 DOWNTO 0);
          x : OUT STD_LOGIC_VECTOR(7 DOWNTO 0));
END convert;
ARCHITECTURE convertor OF covert IS
BEGIN
PROCESS(b)
BEGIN
CASE b IS
WHEN “0000” => x <= “1111110”;
WHEN “0001” => x <= “0110000”;
WHEN “0010” => x <= “1101101”;
WHEN “0011” => x <= “1111001”;
WHEN “0100” => x <= “0110011”;
WHEN “0101” => x <= “1011011”;
WHEN “0110” => x <= “1011111”;
WHEN “0111” => x <= “1110000”;
WHEN “1000” => x <= “1111111”;
WHEN “1001” => x <= “1110011”;
WHEN OTHERS => x <= “0000000”;
END CASE;
END PROCESS;
```

```
END CASE;
END PROCESS;
END convertor;
```

The given code represents a convertor. Which kind of convertor it is ?

Select the correct answer.

- Gray to BCD
- 7 segment to BCD
- BCD to gray
- BCD to 7 segment display

What will be the value of **b** and **c** in the following C code?

```
int a, b, c;
int main() {
  a = 7;
  b = a++;
  c = ++a;
  printf(“b=%d, c=%d”,b,c);
  return 0;
}
```

Select the correct answer.

- b=7, c=7
- b=7, c=8
- b=8, c=9
- b=7, c=9

To properly bias an NPN transistor, what polarity voltage is applied to the collector, and what is its relationship to the base voltage ?

Select the correct answer.

- Positive, more negative
- Positive, more positive
- Negative, more positive
- Negative, more negative

If SUNDAY is coded as 012345 and BIG is coded as 678, how will SANDBAY be coded in the same code:

Select the correct answer.

- 0234456
- 0423645
- 0432645
- 0342456
- None of the choices.

To use a comparator for zero-level detection, the inverting input is connected to:

Select the correct answer.

- A negative reference voltage
- The DC supply voltage
- A positive reference voltage
- Ground

```
LIBRARY IEEE;
USE IEEE.std_logic_1164.all;
ENTITY my_logic IS
GENERIC n : INTEGER := 8;
PORT (sig1 : bit_vector(n-1 DOWNTO 0);
            Sig2 : bit_vector(n-1 DOWNTO 0));
END my_logic;
ARCHITECTURE test OF my_logic IS
COMPONENT or2
   PORT(a0, a1 : IN BIT;
                z          : OUT BIT);
END COMPONENT or
BEGIN
ORARRAY : FOR i IN (n-1) DOWNTO 0 GENERATE
                    or_gate : or2
PORT MAP ( a0 => sig1(i),
                       A1 => sig2(i),
                         z => y(i));
END GENERATE ORARRAY;
END test;
```

What is realized in the code given above ?

```
                    or_gate : or2
PORT MAP ( a0 => sig1(i),
                       A1 => sig2(i),
                         z => y(i));
END GENERATE ORARRAY;
END test;
```

What is realized in the code given above ?

Select the correct answer.

- 7- Bit parallel adder ignoring the carry
- 7- Bit parallel adder including the carry
- 8- Bit parallel adder ignoring the carry
- 8- bit parallel adder including the carry

```
class student
{
    int marks;
}
student s1;
student s2=2;
```

Choose the correct option for the code:

Select the correct answer.

- Object s1 should be passed with argument
- Object s2 should not be declared
- Object s2 will not be created, but program runs
- Program gives compile time error

The field effect transistors compared with bipolar transistors we have:

Select the correct answer.

- Have small input resistance
- Have small noise coefficient
- The current is at the same time conditioned by electrons and holes
- Provide current amplification
- The performance is mainly conditioned by injection of minority carriers

When faced with conflicting priorities or tasks, how do you prioritize and manage your workload?

Select the correct answer.

- Prioritize tasks based on personal preference.
- Delegate tasks to others to manage conflicting priorities.
- Assess urgency and importance to prioritize the tasks.
- Randomly choose tasks to execute first.
- Tackle easy tasks first then move to complex ones.

What provides a parameter specifying the maximum rate of change of the output when driven by a large step-input signal ?

Select the correct answer.

- Step rate
- Dynamic rate
- Slew rate
- Stable rate

```
begin
    -- (Process 1)
    process(CLK)
    begin
        if rising_edge(CLK) then
            current_state <= next_state;
        end if;
    end process;

    -- (Process 2)
    process(A, current_state)
    begin
        case current_state is
            when S0 =>
                if A = '1' then
                    Z <= '1';
                    next_state <= S1;
                else
                    Z <= '0';
                    next_state <= S0;
                end if;
            when S1 =>
                if A = '1' then
                    Z <= '0';
                    next_state <= S0;
                else
                    Z <= '1';
                    next_state <= S1;
                end if;
            when others =>
                Z <= '0';
                next_state <= S0;
        end case;
    end process;

    Y <= Z;
end quiz_fsm_arc;
```

What type of Finite State Machine (FSM) is implemented in the provided VHDL code?

Select the correct answer.

- Mealy machine
- Moore machine
- Both Mealy and Moore
- Neither Mealy nor Moore

```
#include<stdio.h>
 int xyz=10;
 int main() {
   int xyz=20;
   printf("%d",xyz);
   return 0;
 }
```

What would be the output of the above C program?

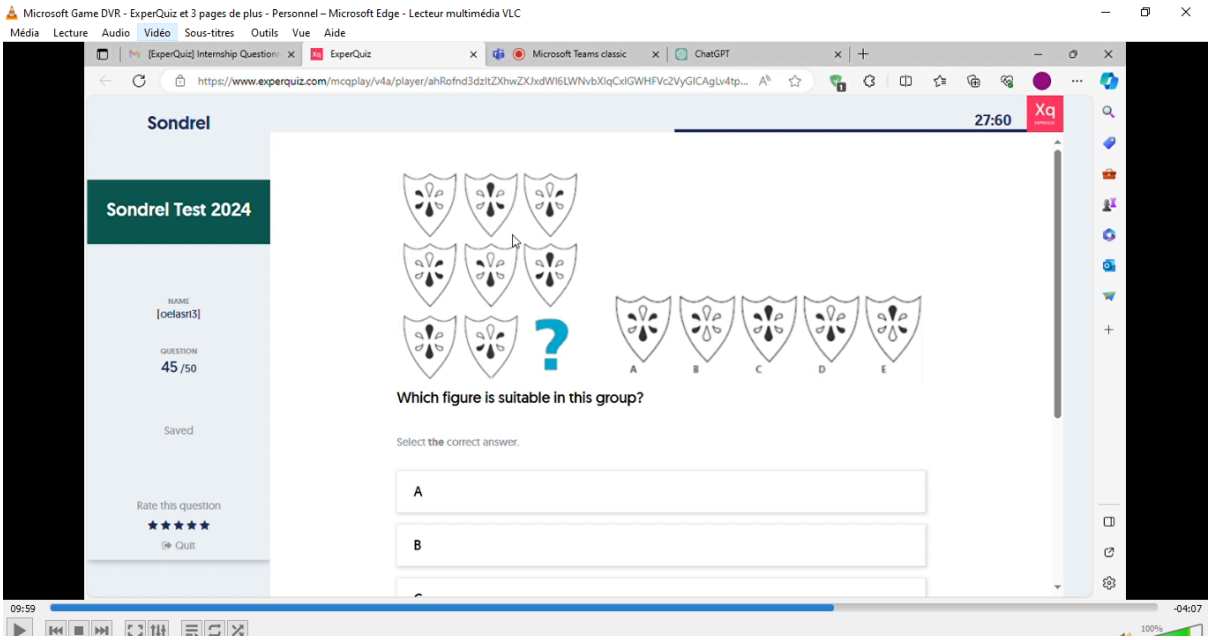
Select the correct answer.

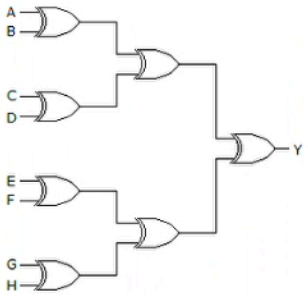
- xyz
- 10
- 20

Which step not belong to the Place and Route flow ?

Select the correct answer.

- Floorplan
- Clock Tree Synthesis
- Synthesis
- Routing





The 8-input XOR circuit shown has an output of Y = 1. Which input combination below (ordered A – H) is correct ?

Select the correct answer.

10111100

10111000

11100111

00011101

```
entity quiz_fsm is
    Port ( A    : in  STD_LOGIC;
           Y    : out STD_LOGIC;
           CLK  : in STD_LOGIC);
end quiz_fsm;

architecture quiz_fsm_arc of quiz_fsm is
    type State_Type is (S0, S1);
    signal current_state, next_state : State_Type;
    signal Z : STD_LOGIC;
begin
    -- (Process 1)
    process(CLK)
    begin
        if rising_edge(CLK) then
            current_state <= next_state;
        end if;
    end process;

    -- (Process 2)
    process(A, current_state)
    begin
        case current_state is
            when S0 =>
                if A = '1' then
                    Z <= '1';
                    next_state <= S1;
                else
                    Z <= '0';
                    next_state <= S0;
                end if;
            when S1 =>
                if A = '1' then
                    Z <= '0';
                    next_state <= S0;
                else
                    Z <= '1';
```

```
                    next_state <= S0;
                else
                    Z <= '1';
                    next_state <= S1;
                end if;
            when others =>
                Z <= '0';
                next_state <= S0;
        end case;
    end process;

    Y <= Z;
end quiz_fsm_arc;
```

Considering the provided FSM code, what modifications would you make to implement a 3-state machine with states S0, S1, and S2 ?

Select the correct answer.

- Add an additional elsif branch for S2 in Process 2
- Change the type definition to type State_Type is (S0, S1, S2)
- Add a third output signal
- Modify the clock edge condition in Process 1

Which is valid C expression ?

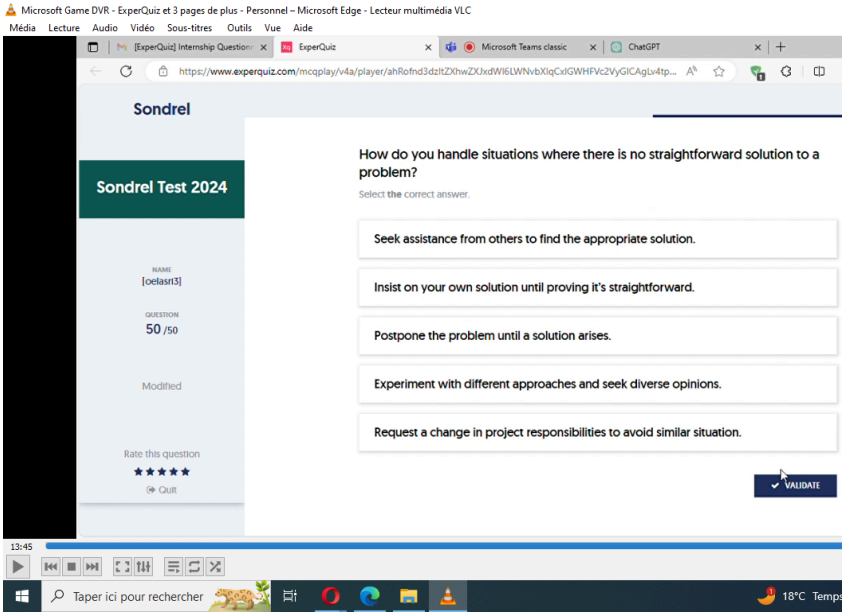
Select the correct answer.

- int my_num = 10_0000;
- int my_num = 100,000;
- int my_num = 100000;
- int my num = 100000;
- int my_num = 100,000;
- int $my_num = 100000;
- int my num = 10.0000;

Which of the below mentioned statements is wrong for electronic lithography ?

Select the correct answer.

- In this method the electron beams are used as a source of radiation
- The method of electron beam lithography is based on non-thermal influence left by electron beam on resist
- The ultraviolet beams fall on resist surface at electron beam lithography
- It is possible to reduce diffraction effects by increasing the electron accelerating voltage in electron beam lithography
- The correct answer is missing



2nd round : (1h in English)

- What’s an ASIC? What's a FPGA? What's the difference between them?
- How are asics created?
- What is the difference between a flip-flop and a latch?
- What is Setup time and hold time?
- How do you start a project?
- When facing a problem, what do you do?
- Do you prefer teamwork or individuals? Why?
- Tell us about a time you faced a problem while working on a project and how did you manage to find a solution?

3rd round : (30 min in English)

- Talk to us about yourself
- How does communication happen in a team?
- What thing that a team should have to succeed?
-

Siemens: (30 min via teams)

- What a VLSI?
- Development cycle of an IC?
- How do you implement a program on an FPGA board?
-