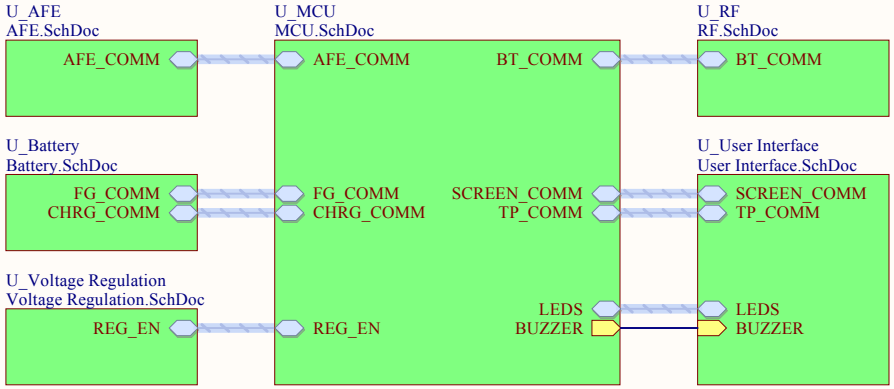
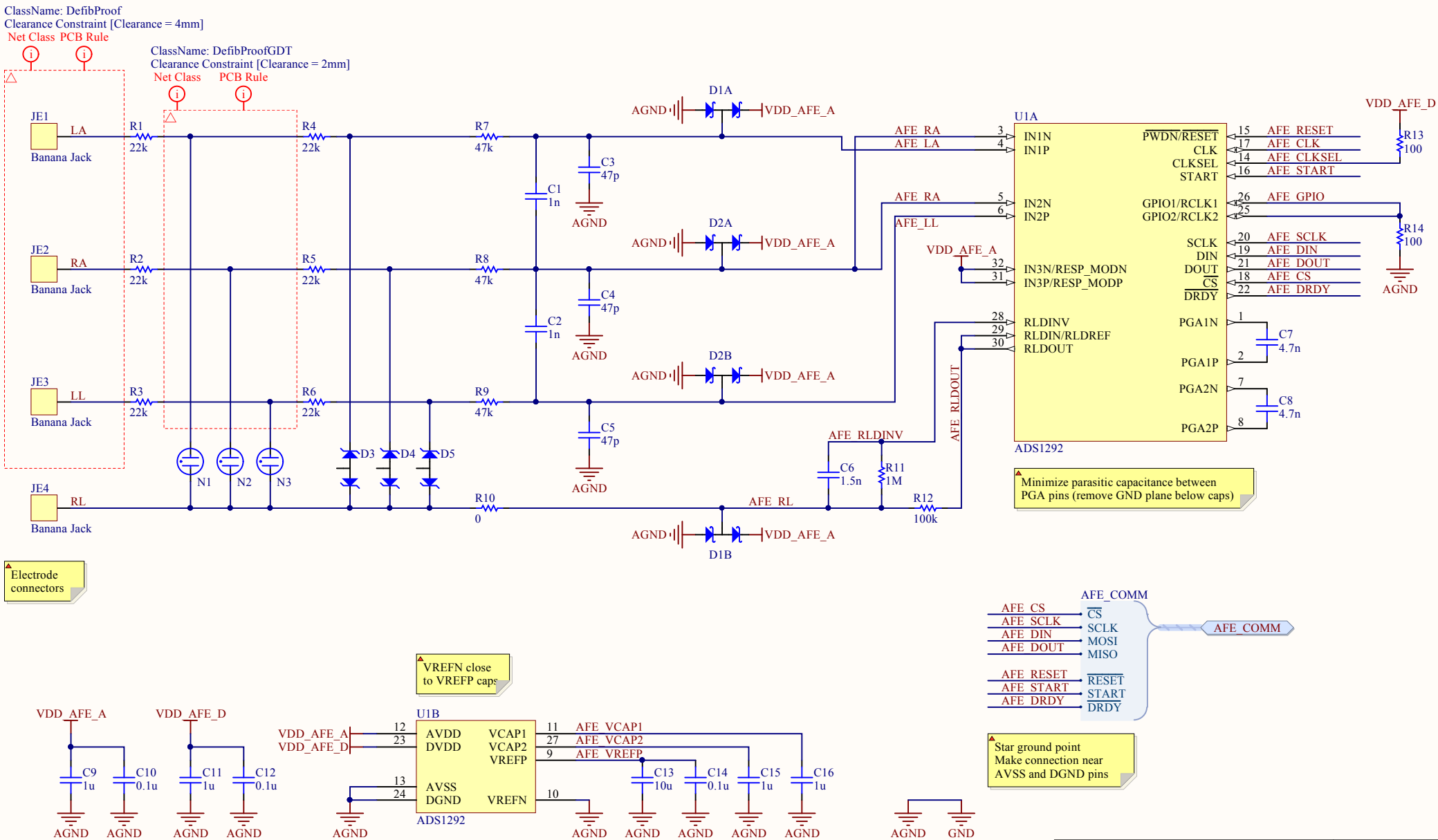
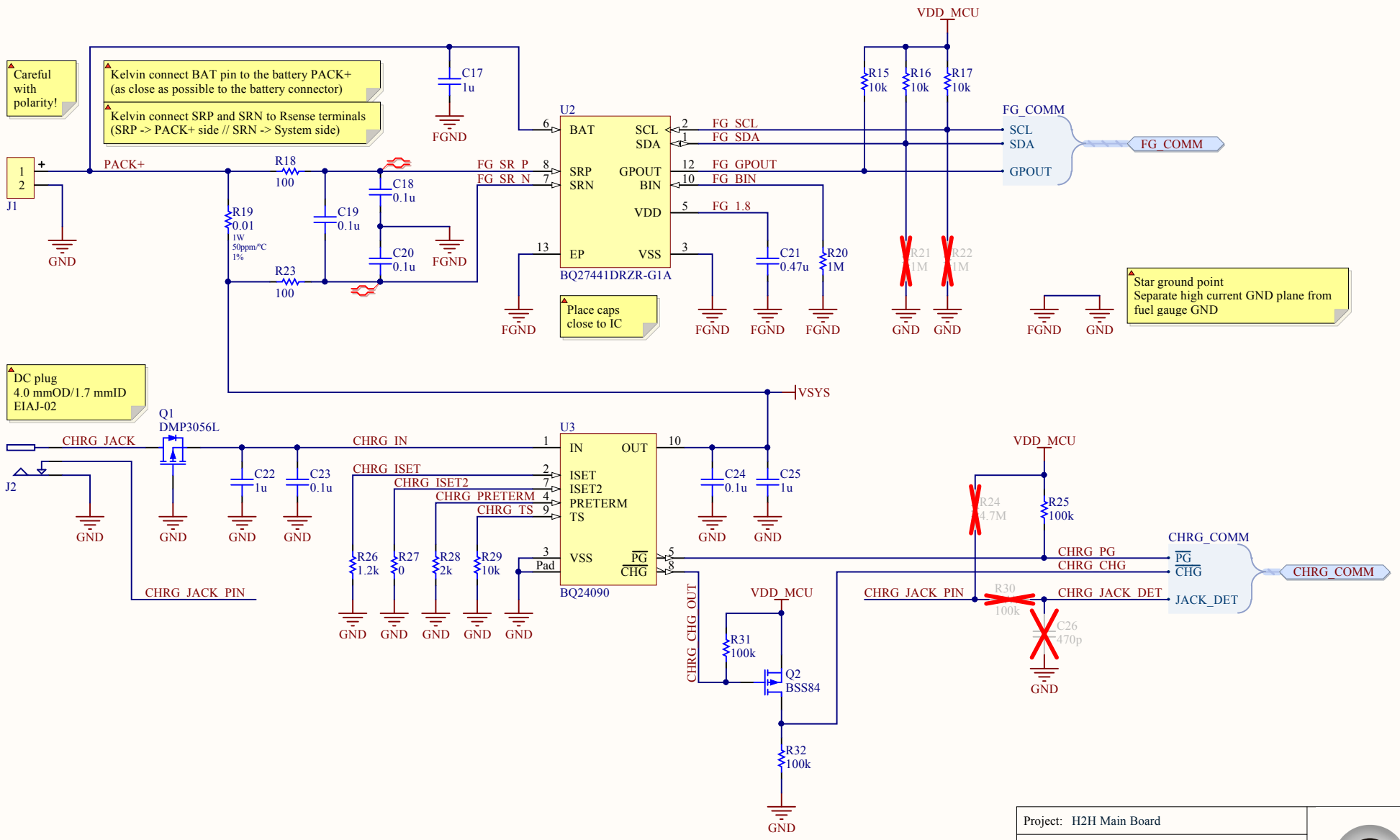
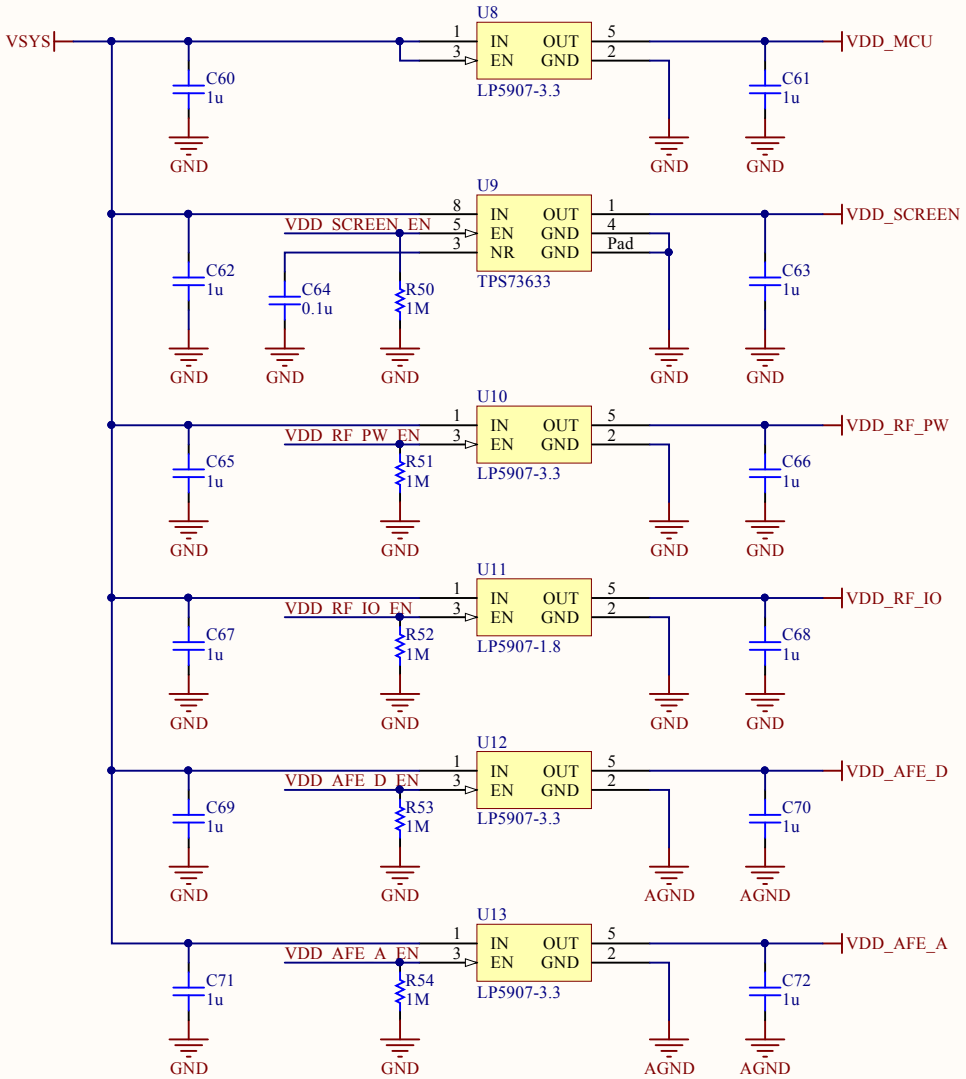


Project:	H2H Main Board
Title:	Main Board
Author:	Samuel López
Sheet 1 of 7	Date: 2016/01/06


ClassName: DefibProof
Clearance Constraint [Clearance = 4mm]
Net Class PCB Rule
ClassName: DefibProofGDT
Clearance Constraint [Clearance = 2mm]
Net Class PCB Rule
JE1
LA
Banana Jack
JE2
RA
Banana Jack
JE3
LL
Banana Jack
JE4
RL
Banana Jack
R1 22k
R2 22k
R3 22k
R4 22k
R5 22k
R6 22k
R7 47k
R8 47k
R9 47k
R10 0
C1 1n
C2 1n
C3 47p
C4 47p
C5 47p
N1
N2
N3
D1A
D2A
D2B
D1B
D3
D4
D5
AGND
VDD_AFE_A
AFE_RA
AFE_LA
AFE_LL
AFE_RL
U1A
IN1N
IN1P
IN2N
IN2P
IN3N/RESP_MODN
IN3P/RESP_MODP
RLDINV
RLDIN/RLDREF
RLDOUT
PWDN/RESET
CLK
CLKSEL
START
GPIO1/RCLK1
GPIO2/RCLK2
SCLK
DIN
DOUT
CS
DRDY
PGA1N
PGA1P
PGA2N
PGA2P
ADS1292
AFE_RESET
AFE_CLK
AFE_CLKSEL
AFE_START
AFE_GPIO
AFE_SCLK
AFE_DIN
AFE_DOUT
AFE_CS
AFE_DRDY
VDD_AFE_D
R13 100
R14 100
C7 4.7n
C8 4.7n
AFE_RLDINV
AFE_RLDOUT
C6 1.5n
R11 1M
R12 100k
Minimize parasitic capacitance between PGA pins (remove GND plane below caps)
Electrode connectors
AFE_COMM
AFE_CS
AFE_SCLK
AFE_DIN
AFE_DOUT
AFE_RESET
AFE_START
AFE_DRDY
CS
SCLK
MOSI
MISO
RESET
START
DRDY
VREFN close to VREFP caps
U1B
AVDD
DVDD
VREFP
AVSS
DGND
VREFN
AFE_VCAP1
AFE_VCAP2
AFE_VREFP
C9 1u
C10 0.1u
C11 1u
C12 0.1u
C13 10u
C14 0.1u
C15 1u
C16 1u
Star ground point
Make connection near
AVSS and DGND pins
GND
Project: H2H Main Board
Title: Analog Front End
Author: Samuel López
Sheet 2 of 7
Date: 2016/01/04


Careful with polarity!
Kelvin connect BAT pin to the battery PACK+ (as close as possible to the battery connector)
Kelvin connect SRP and SRN to Rsense terminals (SRP -> PACK+ side // SRN -> System side)
Place caps close to IC
Star ground point
Separate high current GND plane from fuel gauge GND
DC plug
4.0 mmOD/1.7 mmID
EIAJ-02
J1
J2
PACK+
U2
BQ27441DRZR-G1A
BAT
SCL
SDA
SRP
SRN
GPOUT
BIN
VDD
EP
VSS
FG_SR_P
FG_SR_N
FG_SCL
FG_SDA
FG_GPOUT
FG_BIN
FG_1.8
FG_COMM
R15 10k
R16 10k
R17 10k
R18 100
R19 0.01 1W 50ppm/°C 1%
R20 1M
R21 1M
R22 1M
R23 100
C17 1u
C18 0.1u
C19 0.1u
C20 0.1u
C21 0.47u
VDD_MCU
GND
FGND
Q1
DMP3056L
CHRG_JACK
CHRG_JACK_PIN
VSYS
U3
BQ24090
IN
OUT
ISET
ISET2
PRETERM
TS
VSS
PG
CHG
Pad
CHRG_IN
CHRG_ISET
CHRG_ISET2
CHRG_PRETERM
CHRG_TS
C22 1u
C23 0.1u
C24 0.1u
C25 1u
R24 4.7M
R25 100k
R26 1.2k
R27 0
R28 2k
R29 10k
R30 100k
R31 100k
R32 100k
C26 470p
Q2
BSS84
CHRG_CHG_OUT
CHRG_PG
CHRG_CHG
CHRG_JACK_DET
CHRG_COMM
Project: H2H Main Board
Title: Battery
Author: Samuel López
Sheet 3 of 7
Date: 2016/01/04



VDD_MCU:
Microcontroller supply
(always enabled)

VDD_SCREEN:
LCD screen and touchpad supply

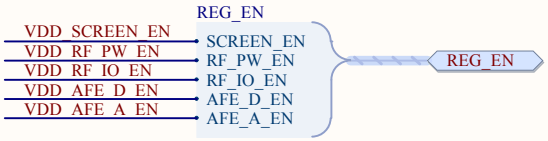
NR capacitor at Screen LDO should connect directly to the GND pin of the device

VDD_RF_PW:
Bluetooth radio power supply

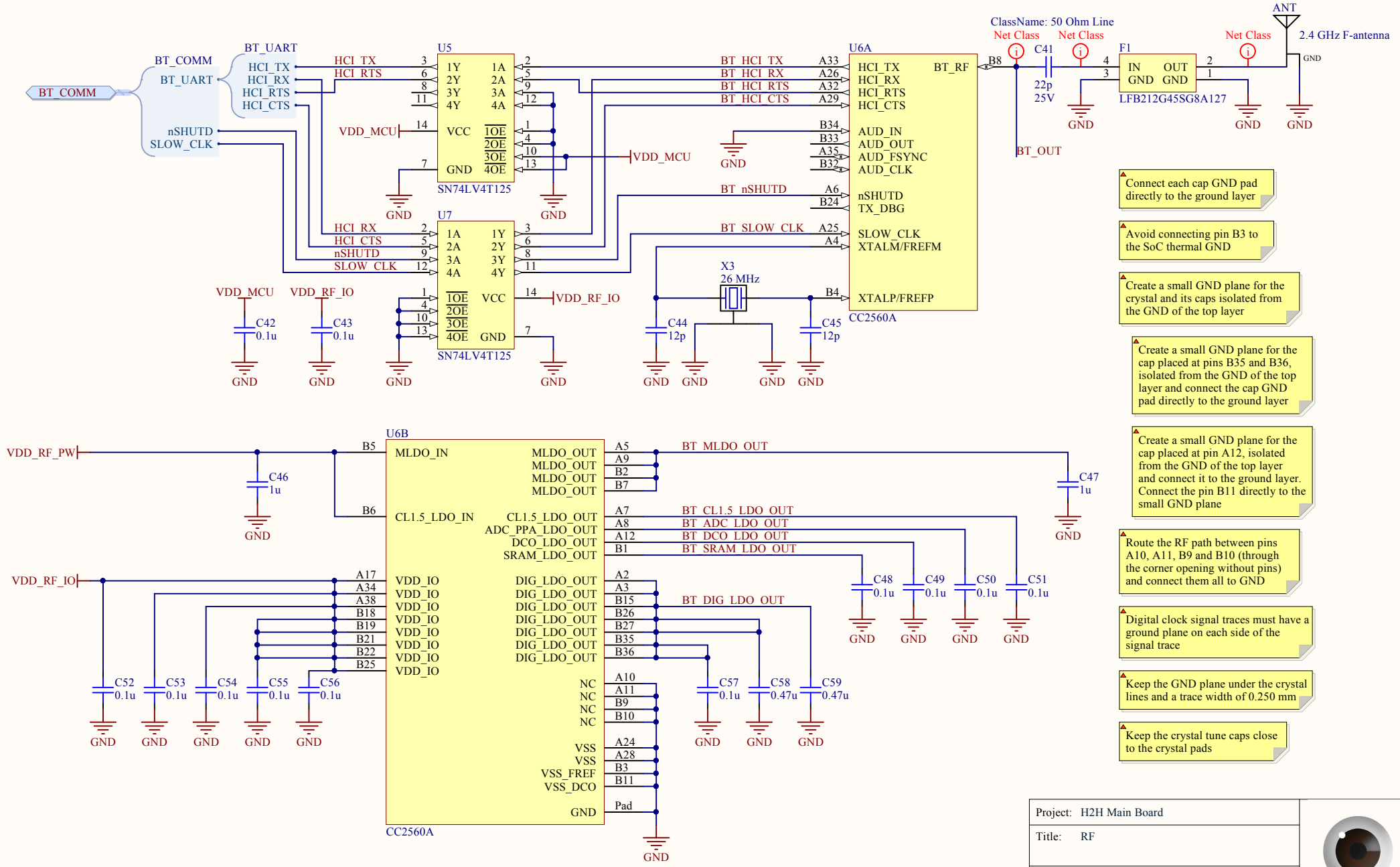
VDD_RF_IO:
Bluetooth radio I/O supply (1.8 V)

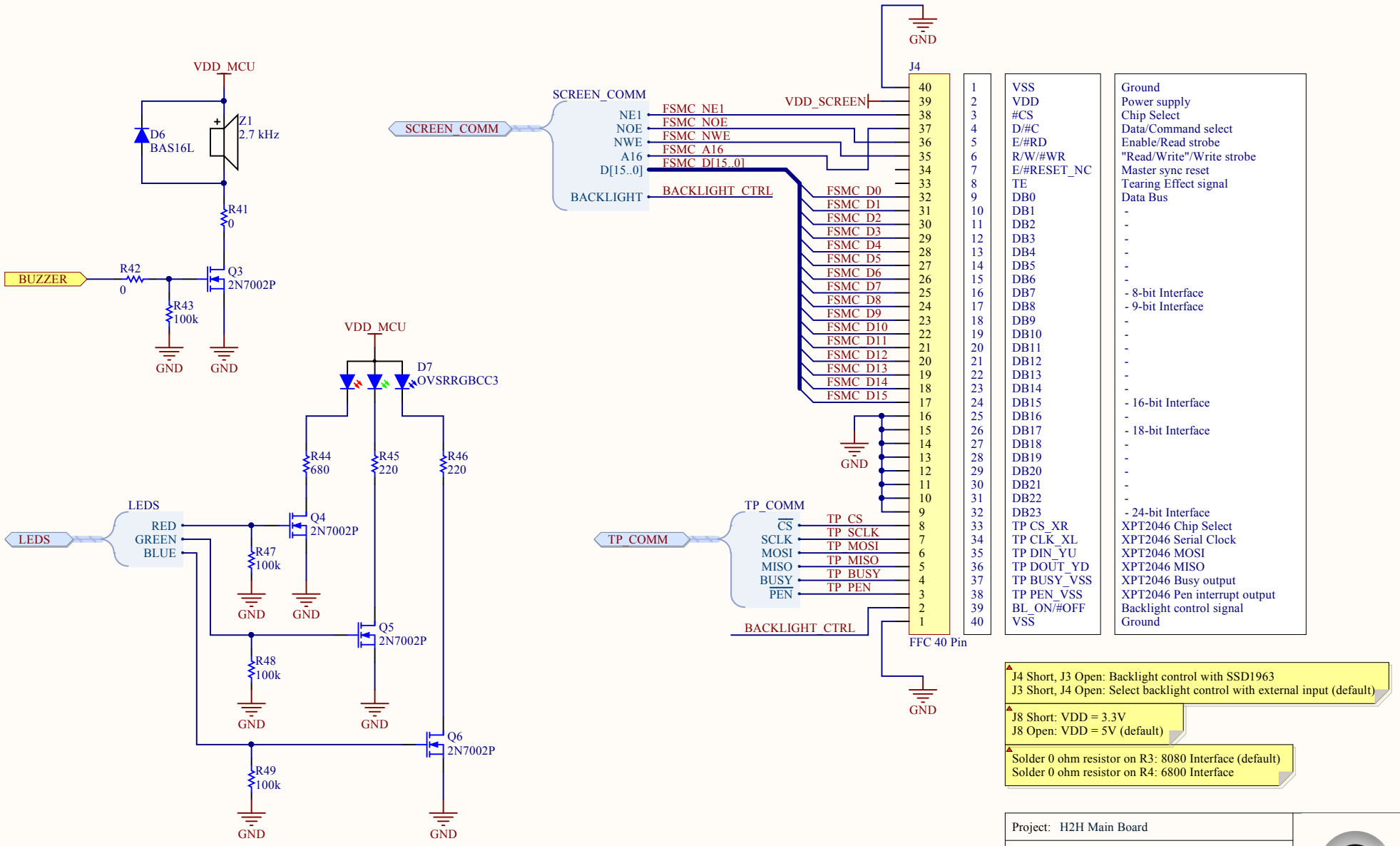
VDD_AFE_D:
Analog front end digital supply

VDD_AFE_A:
Analog front end analog supply



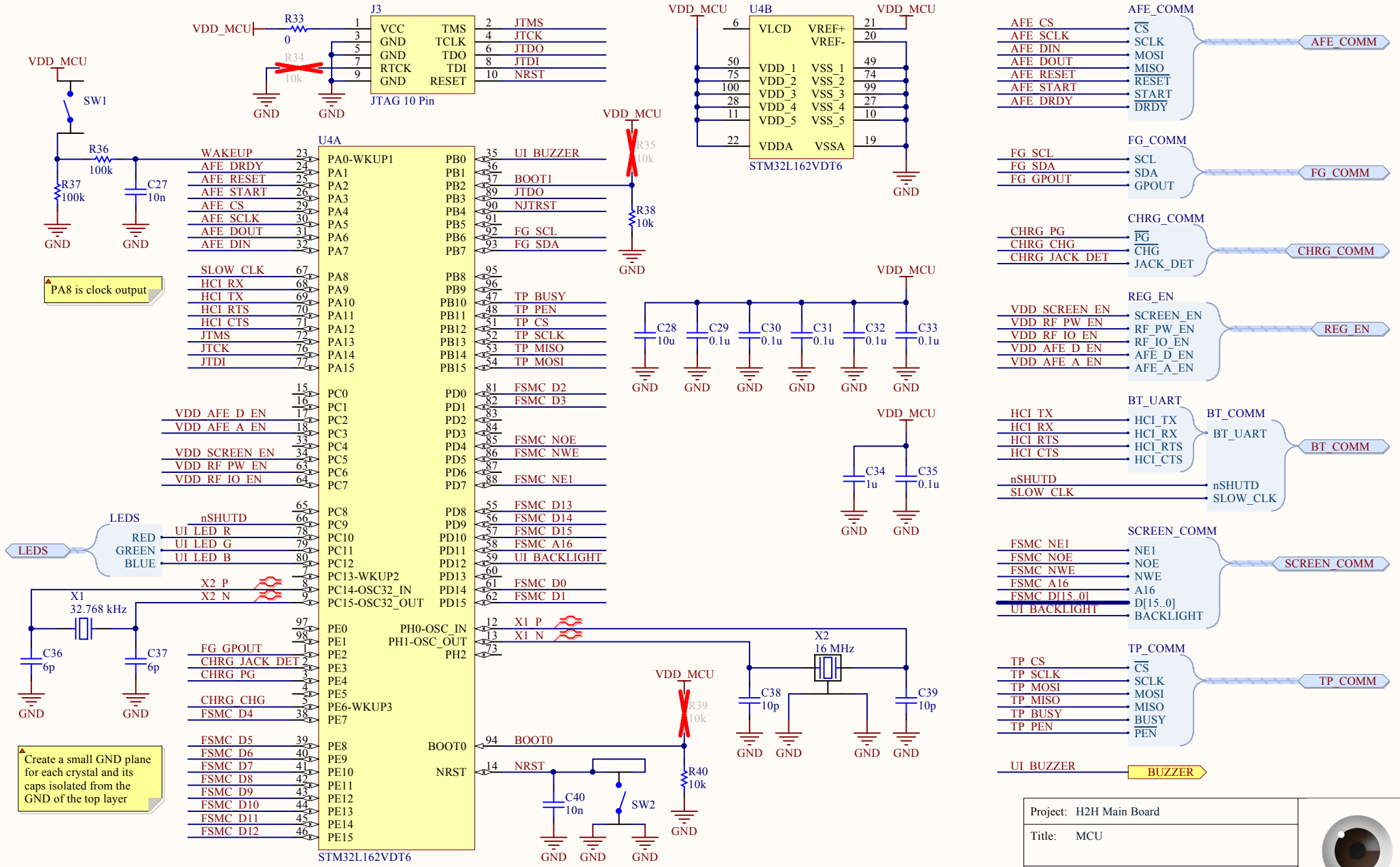
Project:	H2H Main Board
Title:	Voltage Regulation
Author:	Samuel López
Sheet 4 of 7	Date: 2016/01/05


BT_COMM
BT_UART
HCI_TX
HCI_RX
HCI_RTS
HCI_CTS
nSHUTD
SLOW_CLK
U5
SN74LV4T125
U7
SN74LV4T125
VDD_MCU
VDD_RF_IO
GND
C42 0.1u
C43 0.1u
U6A
CC2560A
BT_HCI_TX
BT_HCI_RX
BT_HCI_RTS
BT_HCI_CTS
BT_nSHUTD
BT_SLOW_CLK
AUD_IN
AUD_OUT
AUD_FSYNC
AUD_CLK
TX_DBG
XTALM/FREFM
XTALP/FREFP
BT_RF
X3
26 MHz
C44 12p
C45 12p
ClassName: 50 Ohm Line
Net Class
C41
22p
25V
F1
LFB212G45SG8A127
ANT
2.4 GHz F-antenna
BT_OUT
U6B
VDD_RF_PW
MLDO_IN
CL1.5_LDO_IN
VDD_IO
MLDO_OUT
CL1.5_LDO_OUT
ADC_PPA_LDO_OUT
DCO_LDO_OUT
SRAM_LDO_OUT
DIG_LDO_OUT
NC
VSS
VSS_FREF
VSS_DCO
Pad
BT_MLDO_OUT
BT_CL1.5_LDO_OUT
BT_ADC_LDO_OUT
BT_DCO_LDO_OUT
BT_SRAM_LDO_OUT
BT_DIG_LDO_OUT
C46 1u
C47 1u
C48 0.1u
C49 0.1u
C50 0.1u
C51 0.1u
C52 0.1u
C53 0.1u
C54 0.1u
C55 0.1u
C56 0.1u
C57 0.1u
C58 0.47u
C59 0.47u
Connect each cap GND pad directly to the ground layer
Avoid connecting pin B3 to the SoC thermal GND
Create a small GND plane for the crystal and its caps isolated from the GND of the top layer
Create a small GND plane for the cap placed at pins B35 and B36, isolated from the GND of the top layer and connect the cap GND pad directly to the ground layer
Create a small GND plane for the cap placed at pin A12, isolated from the GND of the top layer and connect it to the ground layer. Connect the pin B11 directly to the small GND plane
Route the RF path between pins A10, A11, B9 and B10 (through the corner opening without pins) and connect them all to GND
Digital clock signal traces must have a ground plane on each side of the signal trace
Keep the GND plane under the crystal lines and a trace width of 0.250 mm
Keep the crystal tune caps close to the crystal pads
Project: H2H Main Board
Title: RF
Author: Samuel López
Sheet 5 of 7
Date: 2016/01/05



1	VSS	Ground	
2	VDD	Power supply	
3	#CS	Chip Select	
4	D/#C	Data/Command select	
5	E/#RD	Enable/Read strobe	
6	R/W/#WR	"Read/Write"/Write strobe	
7	E/#RESET_NC	Master sync reset	
8	TE	Tearing Effect signal	
9	DB0	Data Bus	
10	DB1	-	
11	DB2	-	
12	DB3	-	
13	DB4	-	
14	DB5	-	
15	DB6	-	
16	DB7	- 8-bit Interface	
17	DB8	- 9-bit Interface	
18	DB9	-	
19	DB10	-	
20	DB11	-	
21	DB12	-	
22	DB13	-	
23	DB14	-	
24	DB15	- 16-bit Interface	
25	DB16	-	
26	DB17	- 18-bit Interface	
27	DB18	-	
28	DB19	-	
29	DB20	-	
30	DB21	-	
31	DB22	-	
32	DB23	- 24-bit Interface	
33	TP_CS_XR	XPT2046 Chip Select	
34	TP_CLK_XL	XPT2046 Serial Clock	
35	TP_DIN_YU	XPT2046 MOSI	
36	TP_DOUT_YD	XPT2046 MISO	
37	TP_BUSY_VSS	XPT2046 Busy output	
38	TP_PEN_VSS	XPT2046 Pen interrupt output	
39	BL_ON/#OFF	Backlight control signal	
40	VSS	Ground	

Project:	H2H Main Board
Title:	User Interface
Author:	Samuel López
Sheet	6 of 7
Date:	2016/01/05


J3
JTAG 10 Pin
U4A
STM32L162VDT6
U4B
STM32L162VDT6
PA8 is clock output
Create a small GND plane for each crystal and its caps isolated from the GND of the top layer
LEDS
X1 32.768 kHz
X2 16 MHz
SW1
SW2
AFE_COMM
FG_COMM
CHRG_COMM
REG_EN
BT_UART
BT_COMM
SCREEN_COMM
TP_COMM
BUZZER
Project: H2H Main Board
Title: MCU
Author: Samuel López
Sheet 7 of 7
Date: 2016/01/06