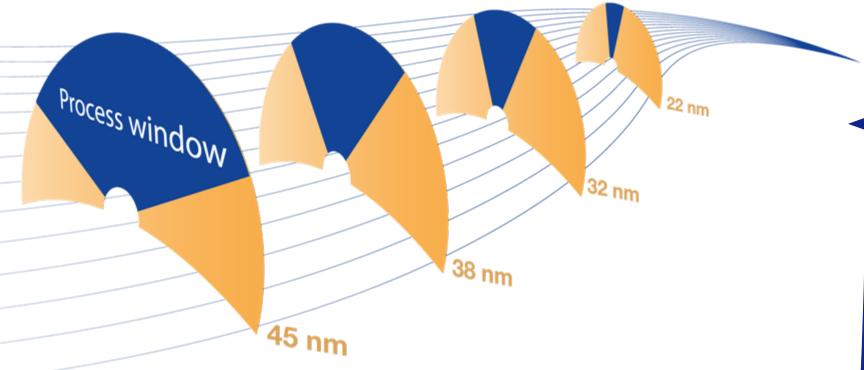


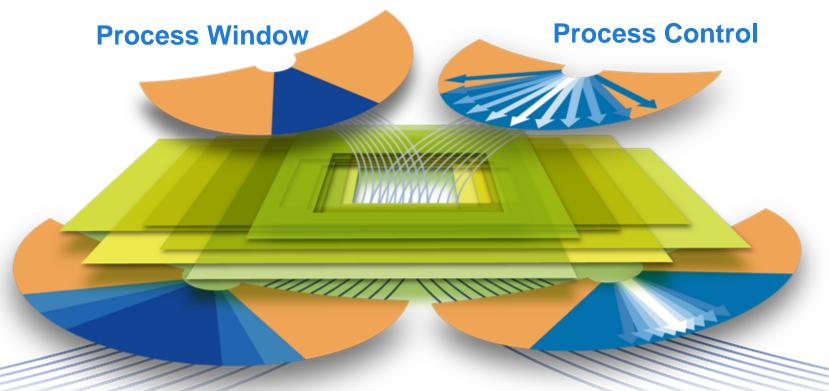
### Shrink is good...except when it's not



- Shrink reduces manufacturing cost and improves device performance
- However, shrink results in smaller process windows which compromise yield by restricting production tolerances



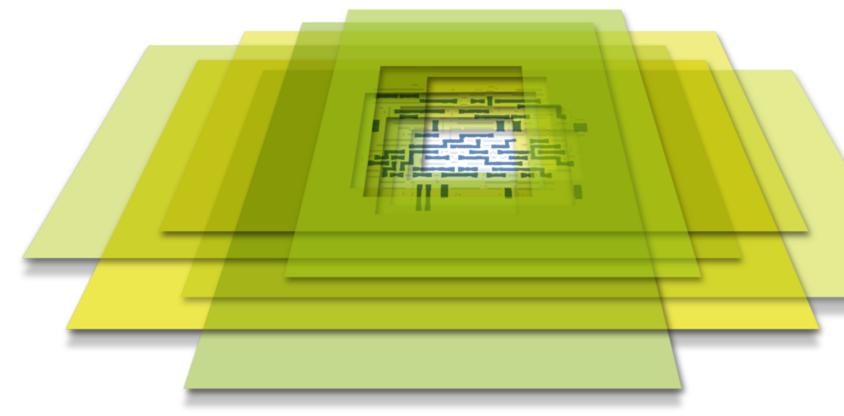
### Holistic lithography provides a window to shrink



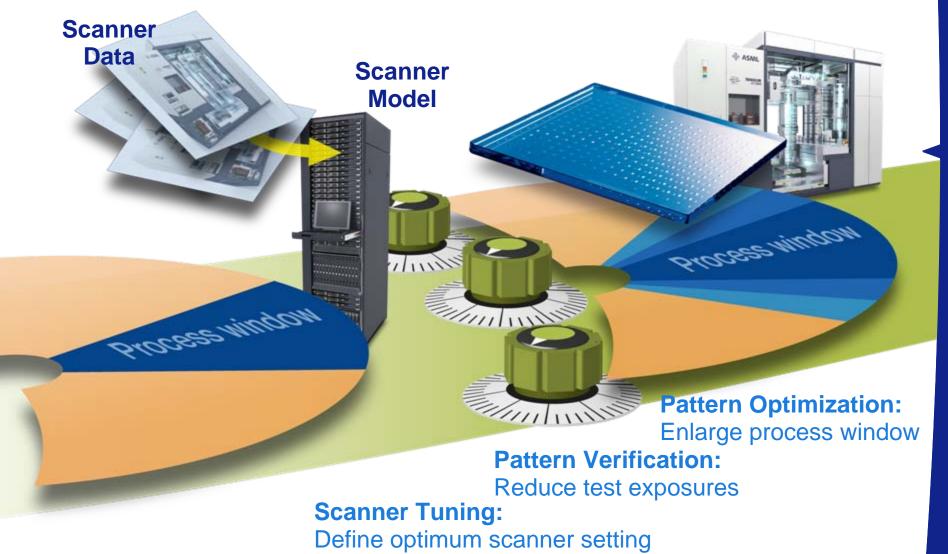
- Holistic lithography is the intelligent integration of computational lithography, wafer lithography and process control.
  - Before manufacturing, holistic lithography optimizes the process window at lower R&D cost
  - During manufacturing, holistic lithography keeps the process in the "sweet spot" of the window.



# **Optimized process window**

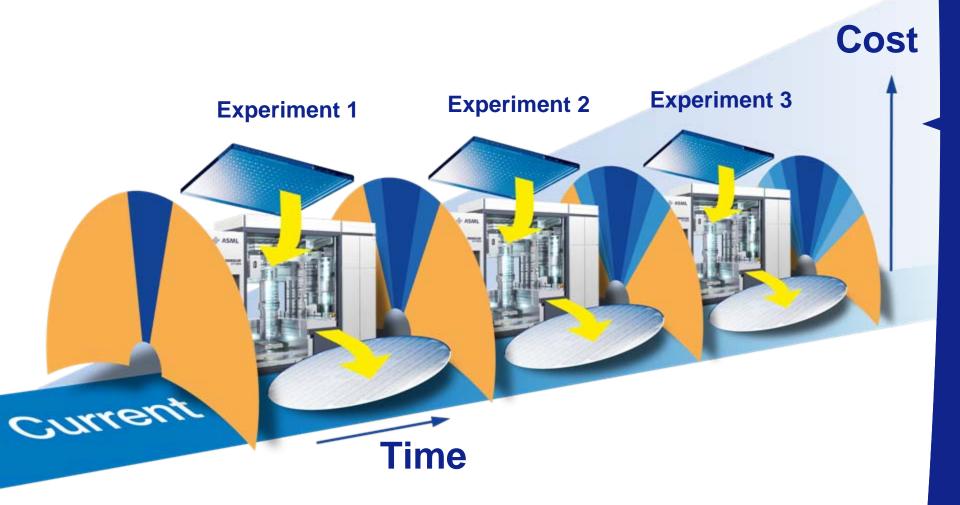


## Actual scanner data enables better process window





# **Faster time-to-money**





**Faster time-to-money** 



Design verification is known much earlier:

- reducing design proofs
- reducing R&D cost
- reducing time to volume ramp-up
- higher yield at ramp to volume

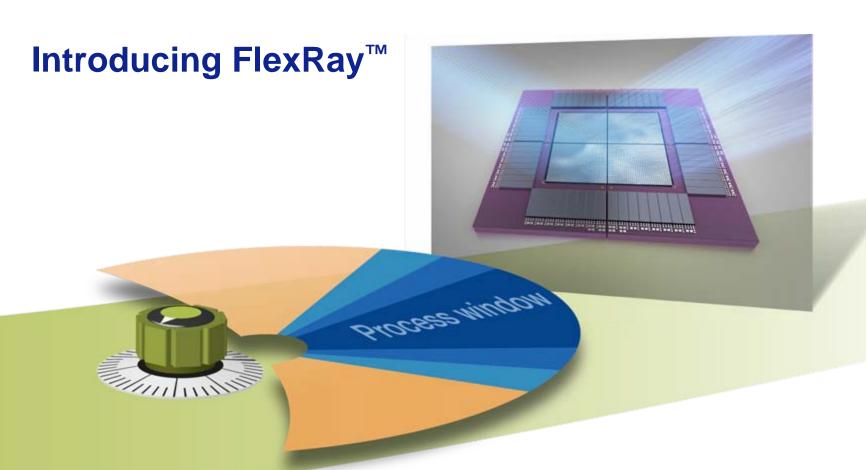


# **Tachyon SMO (Source Mask Optimization)**



By co-optimizing the illumination and reticle, SMO will calculate perfect light conditions and line shapes for an optimal process window.





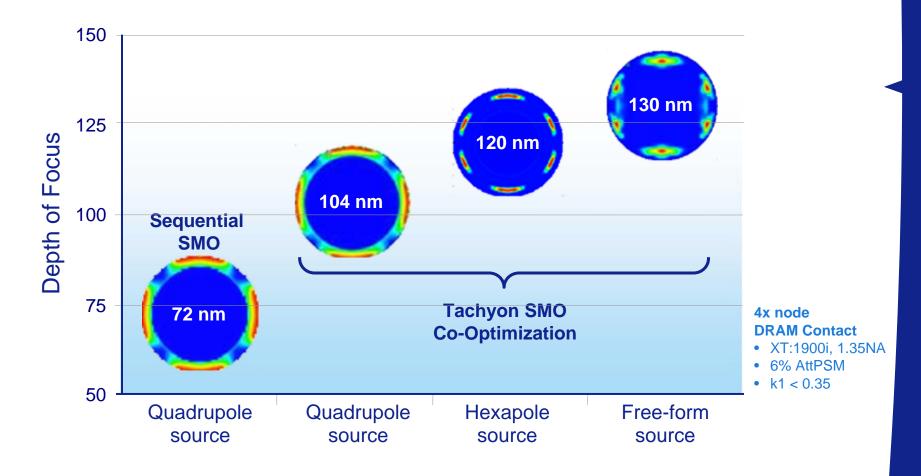
FlexRay freeform illumination technology replaces a traditional illuminator and DOE\* combination with a programmable micro-mirror array. This allows it to render any SMO\*\* defined pupil shape in a matter of minutes.



<sup>\*</sup> diffractive optical element

<sup>\*\*</sup> source mask optimization

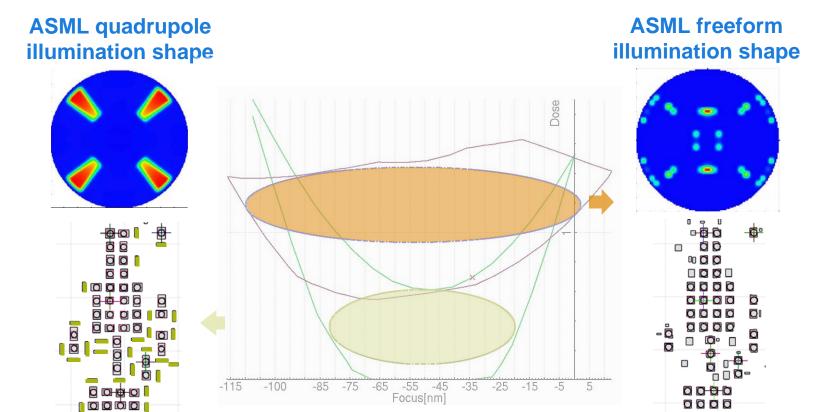
# Mask and freeform source co-optimization improve process window





# Tachyon SMO & FlexRay in Logic contact pattern:

Results in larger process window and lower mask complexity

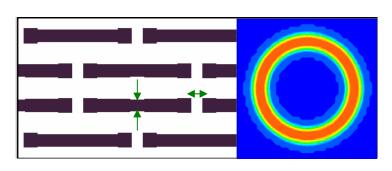


74 nm Depth of Focus @ 5% EL 110 nm Depth of Focus @ 5% EL



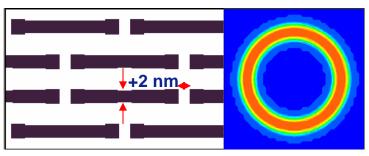
# Reticle Specific Optimization combined with FlexRay illumination source adjustment

Compensating reticle bias errors while maintaining OPC validity



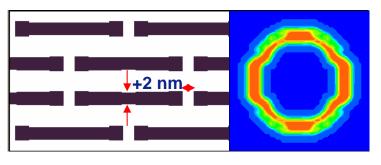
Wafer CD

Width = 44.1 nm Gap = 58.4 nm



+2 nm bias error yields 6.5 nm gap error

Width = 44.1 nm Gap = 51.9 nm

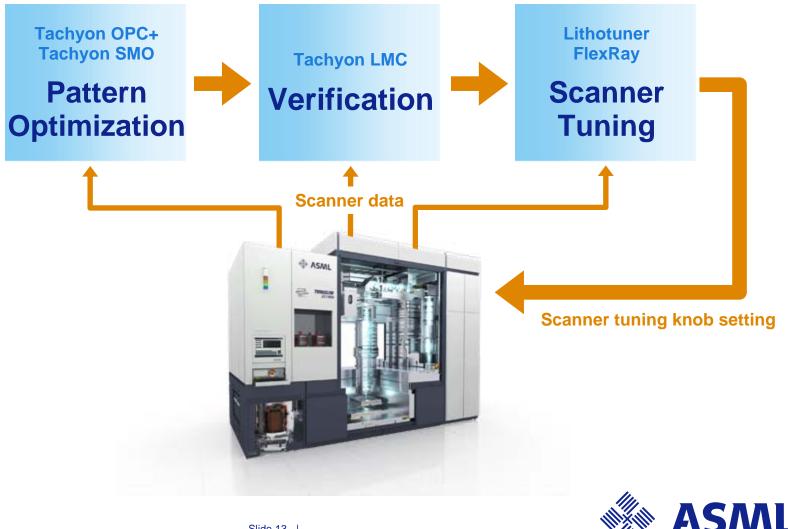


Source adjustment

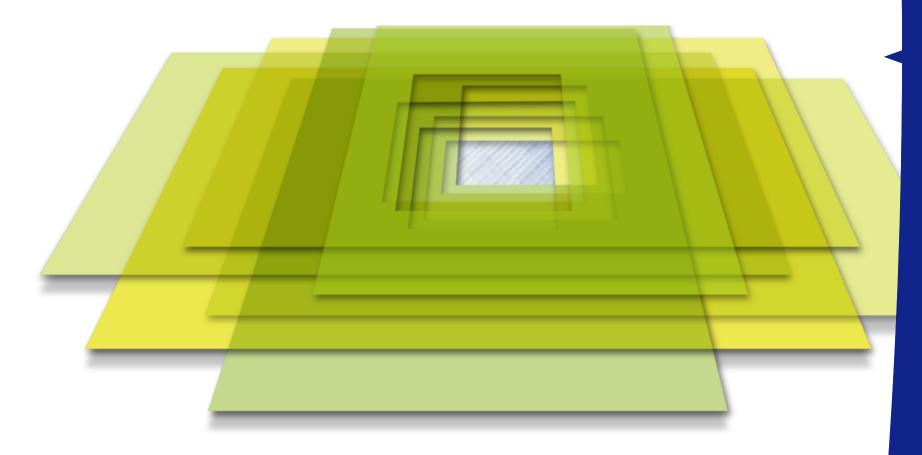
Width = 44.1 nm Gap = 58.4 nm



# ASML holistic lithography application flow to optimize the process window



# Improved production control





# Scanner tuning pre-sets and control loops for better production control



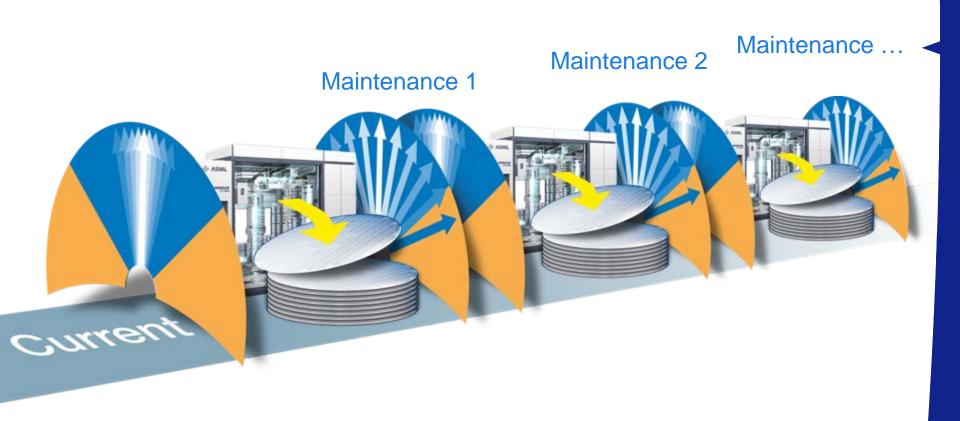
Mask design Monitor wafers Process wafers

### **Tuning**

Scanner tuning
Scanner Setting Verification
Process Control

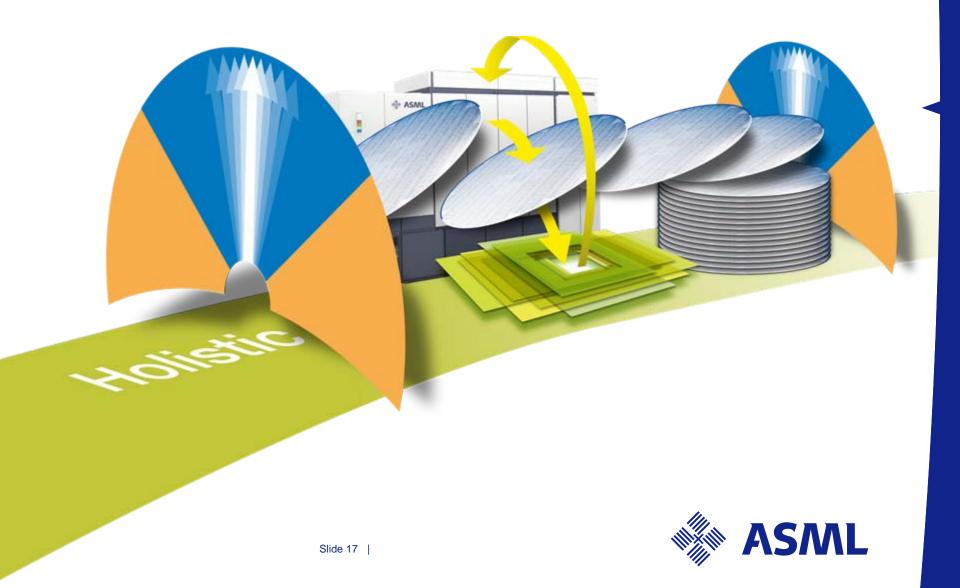


# Better control for higher yield

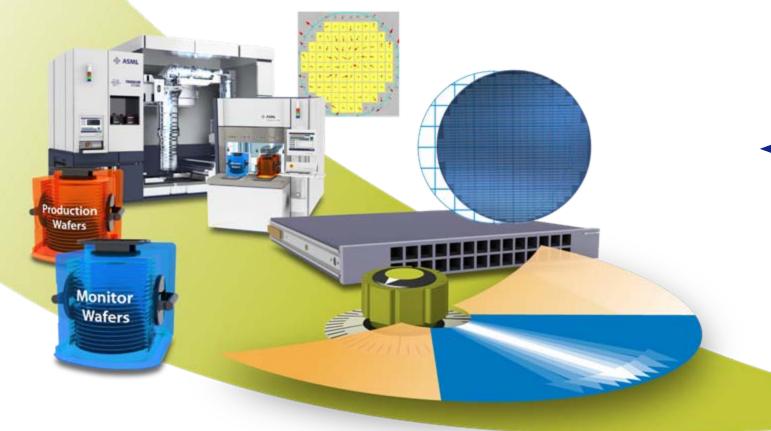




# Better control for higher yield



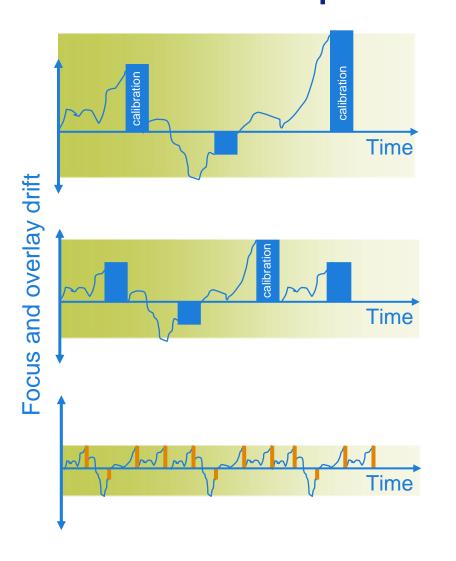
# **BaseLiner™** scanner stability



BaseLiner scanner stability is a complete scanner enhancement solution which maintains overlay and focus stability of TWINSCAN while increasing system availability.



# BaseLiner: Smaller variation in process window, increased availability



#### **System standard**

System drift is countered by performing regular on-tool calibrations according to the ASML maintenance schedule to maintain the system within specified performance.

# Tighter control to support smaller process window

The process window can be maintained by performing more frequent calibrations, but this reduces availability/productivity and therefore decreases wafers-per-day.

#### **BaseLiner**

BaseLiner eliminates additional calibrations and applies corrections more frequently.

Measurements are done off-tool using monitor wafers. Tighter control with increased wafersper-day



### **BaseLiner: overlay stability improvement\***

Including strategy to maintain stability

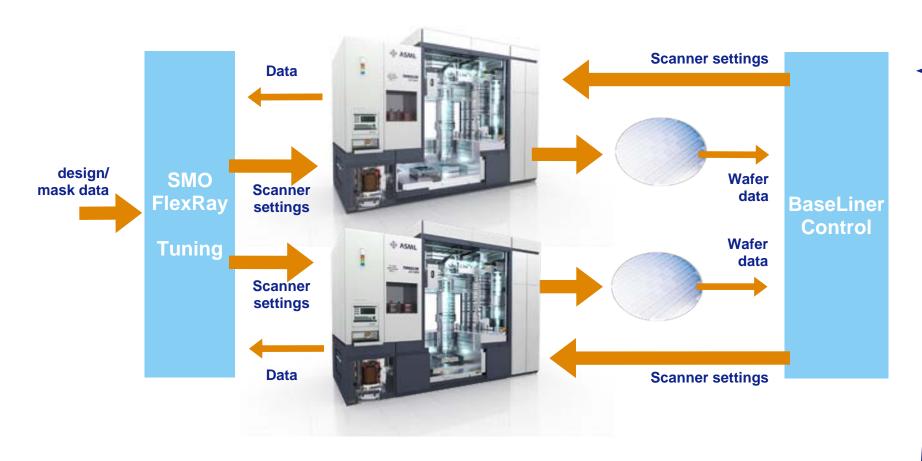




<sup>\*</sup> Matched, full wafer on XT:1900i

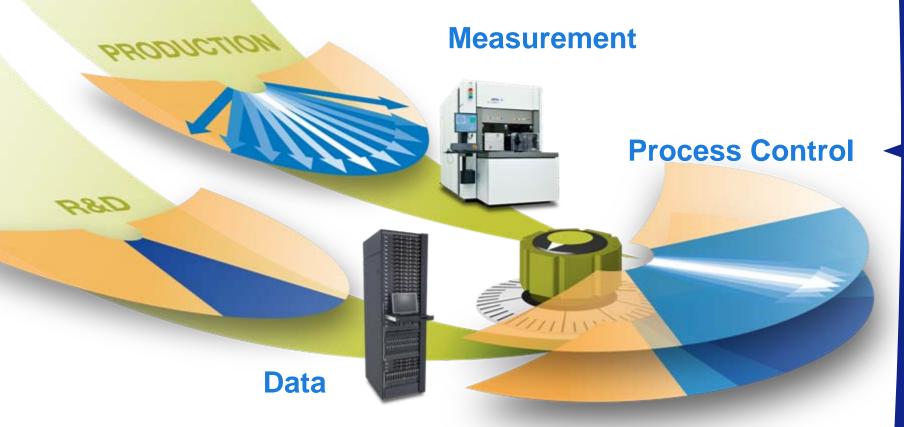
# **ASML** holistic lithography flow for manufacturing

Faster ramp up and higher yield





### Holistic lithography provides a window to shrink



- Holistic lithography is the intelligent integration wafer lithography, computational lithography and process control
- Holistic lithography leverages increased and improved data integration to provide more control, better performance and higher yield

# Eclipse<sup>TM</sup> Holistic Lithography packages



## **ASML** makes Holistic Litho available via Eclipse



- Eclipse is a package of application- and node-specific products and services from our Holistic Lithography portfolio
- Eclipse packages provide chipmakers a window to shrink with cost reduction beyond traditional cost-per-layer



### **ASML** makes Holistic Litho available via Eclipse

