FAIRCHILD SEMICONDUCTOR™ 仙童

April 1988
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74F181
4位算数逻辑单元

简介:

74F181是一个4位的算术逻辑单元(ALU)在两个输入变量上执行所有可能的16个逻辑操作以及有各种各样的算术运算。这比肖特基ALU快40%但只消耗30%的电量。

特征

■ 丰富的超前加法器对于长字节的高速逻辑运算

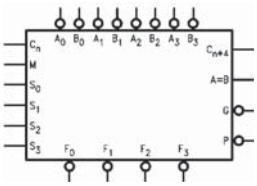
Ordering Code:

Order Number	Package Number	Package Description
74F181SC	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74F181PC	N24A	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-010, 0.600 Wide
74F181SPC	N24C	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-100, 0.300 Wide

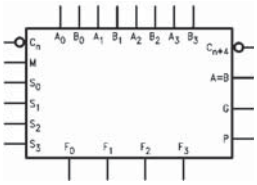
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

逻辑符号

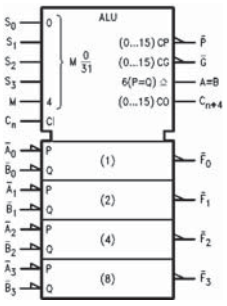
高有效逻辑图



低有效逻辑图



世界标准



引脚图

单位加载/扇出

引脚名称	描述	U.L. HIGH/LOW	输入I_{IH}/I_{IL} 输出I_{OH}/I_{OL}
$\overline{A}_0 - \overline{A}_3$	A 数输入(低有效)	1.0/3.0	20 μA/–1.8 mA
$\overline{B}_0 - \overline{B}_3$	B 数输入(低有效)	1.0/3.0	20 μA/–1.8 mA
$S_0 - S_3$	功能选择输入	1.0/4.0	20 μA/–2.4 mA
M	模式控制输入	1.0/1.0	20 μA/–0.6 mA
C_n	进位输入	1.0/5.0	20 μA/–3.0 mA
$\overline{F}_0 - \overline{F}_3$	结果输出(低有效)	50/33.3	–1 mA/20 mA
A = B	比较输出	OC (Note 1)/33.3	(Note 1)/20 mA
$\overline{G}$	进位产生输出(低有效)	50/33.3	–1 mA/20 mA
$\overline{P}$	进位传播输出 (低有效)	50/33.3	–1 mA/20 mA
C_{n+4}	进位输出	50/33.3	–1 mA/20 mA

Note 1: 集电极开路

功能性说明：

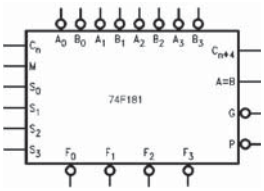
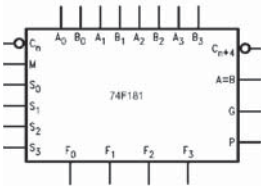
74F181是一个4位高速并行运算逻辑单元(ALU)。由四个函数选择输入控制(s0-s3)和模式控制输入(M)，它可以执行所有16种可能的逻辑操作或16种不同的算术运算对于高低有效操作数上。函数表列出了这些操作。

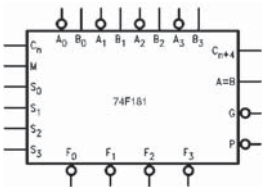
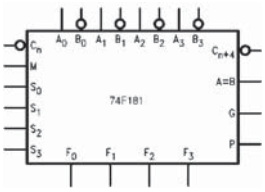
当模式控制输入(M)为高时，所有内部的进位传输都被抑制，设备在被列出的各个位上执行逻辑操作。当模式控制输入很低时，就启用了进位，设备对这两个4位字节进行算术运算。该设备包含了完整的内部进位，并提供了使用Cn+4输出的设备之间的连锁反应，或者是使用信号P′(进位传播)和G′(进位生成)的集成电路之间的进位。在加法模式中，P′表示F是15或更多，而G′表示F是16或更多。在相减模式下，P′表示F等于零或更少，而G′表示F小于零。P′和G′不受进位的影响。当速度要求不严格时，74F181可以在一个简单的串行进位模式中使用，通过连接将输出(Cn+4)信号传输到下一个单元的进位输入(Cn)。为了高速运转，该设备使用了超前进位电路。每组（4个）74F181需要一个进位检查芯片（74F182）。超前进位加法器可以在不同的级别提供进位，并且提供高速的能力，超过了非常长的字节长度。

设备的A=B输出将在所有4个F′输出值都变成四位相同且在逻辑单元处于减法模式可以指示相等时变为高电平，由于A=B输出是集电极开路，所以它可以与其他A=B输出进行连接，以便对超过4位的数据进行比较。A=B信号也可以用在Cn+4信号上，表示A>B或A<B。

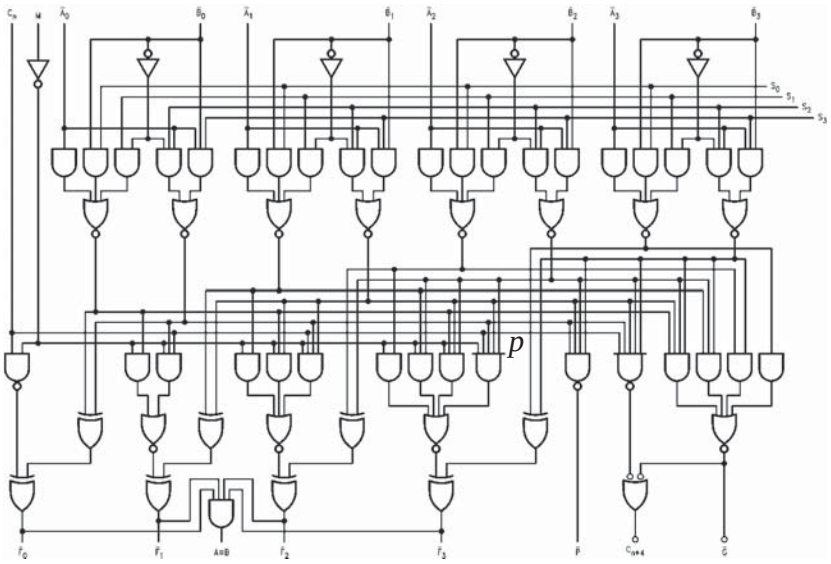
函数表列出了在没有进位的情况下执行的算术运算。输入的进位将为每个字节添加一个“1”。因此，选择代码“LHHL”会生成一个A-B-1(2s补充笔记)而不带进位输入且会在进位输入时生成A-B。因为减法实际上是通过补充加法(1补充笔记)来执行的，所以执行的意思是借';因此，当没有溢出的时候就产生了一个进位，当没有溢出的时候就不产生进位。如文章所示，该设备可用于低有效输入，输出低有效；高有效输入，输出高有效。对于这两种情况，表都列出了执行逻辑符号中标记的操作字符的方法。

Operation Table

	S_0	S_1	S_2	S_3	Logic (M=H)	Arithmetic (M=L, C_0=Inactive)	Arithmetic (M=L, C_0=Active)
	L	L	L	L	$\overline{A}$	A minus 1	A
	H	L	L	L	$\overline{A} \cdot \overline{B}$	A • B minus 1	A • B
	L	H	L	L	$\overline{A} + B$	A • $\overline{B}$ minus 1	A • $\overline{B}$
	H	H	L	L	Logic “1”	minus 1 (2s comp.)	Zero
	L	L	H	L	$\overline{A + B}$	A plus (A + $\overline{B}$)	A plus (A + $\overline{B}$) plus 1
	H	L	H	L	$\overline{B}$	A • B plus (A + $\overline{B}$)	A • B plus (A + $\overline{B}$) plus 1
	L	H	H	L	$\overline{A \oplus B}$	A minus B minus 1	A minus B
	H	H	H	L	A + $\overline{B}$	A + $\overline{B}$	A + $\overline{B}$ plus 1
	L	L	L	H	$\overline{A} \cdot B$	A plus (A + B)	A plus (A + B plus 1
	H	L	L	H	A⊕B	A plus B	A plus B plus 1
	L	H	L	H	B	A • $\overline{B}$ plus (A + B)	A • $\overline{B}$ plus (A + B) plus 1
	H	H	L	H	A + B	A + B	A + B plus 1
	L	L	H	H	Logic “0”	A plus A (2 × A)	A plus A (2 × A) plus 1
	H	L	H	H	A • $\overline{B}$	A plus A • B	A plus A • B plus 1
	L	H	H	H	A • B	A plus A • $\overline{B}$	A plus A • $\overline{B}$ plus 1
	H	H	H	H	A	A	A plus 1
a. All Input Data Inverted							
	L	L	L	L	$\overline{A}$	A	A plus 1
	H	L	L	L	$\overline{A + B}$	A + B	A + B plus 1
	L	H	L	L	$\overline{A} \cdot B$	A + $\overline{B}$	A + $\overline{B}$ plus 1
	H	H	L	L	Logic “0”	minus 1 (2s comp.)	Zero
	L	L	H	L	$\overline{A} \cdot \overline{B}$	A plus (A • $\overline{B}$)	A plus A • $\overline{B}$ plus 1
	H	L	H	L	$\overline{B}$	A • $\overline{B}$ plus (A + B)	A • B plus (A + B) plus 1
	L	H	H	L	A ⊕ B	A minus B minus 1	A minus B
	H	H	H	L	A • $\overline{B}$	A • $\overline{B}$ minus 1	A • $\overline{B}$
	L	L	L	H	$\overline{A} + B$	A plus A • B	A plus A • B plus 1
	H	L	L	H	$\overline{A \oplus B}$	A plus B	A plus B plus 1
	L	H	L	H	B	A • B plus (A + $\overline{B}$)	A • B plus (A + $\overline{B}$) plus 1
	H	H	L	H	A • B	A • B minus 1	A • B
	L	L	H	H	Logic “1”	A plus A (2 × A)	A plus A (2 × A) plus 1
	H	L	H	H	A + $\overline{B}$	A plus (A + B)	A plus (A+B) plus 1
	L	H	H	H	A + B	A plus (A + $\overline{B}$)	A plus (A+$\overline{B}$) plus 1
	H	H	H	H	A	A minus 1	A
b. All Input Data True							

	S_0	S_1	S_2	S_3	Logic (M=H)	Arithmetic (M=L, C_0=Inactive)	Arithmetic (M=L, C_0=Active)
	L	L	L	L	$\overline{A}$	A minus 1	A
	H	L	L	L	$\overline{A} + B$	$A \cdot \overline{B}$ minus 1	$A \cdot B$
	L	H	L	L	$\overline{A} \cdot \overline{B}$	$A \cdot B$ minus 1	$A \cdot B$
	H	H	L	L	Logic "1"	minus 1 (2s comp.)	Zero
	L	L	H	L	$\overline{A} \cdot B$	A plus $(A + B)$	A plus $(A + B)$ plus 1
	H	L	H	L	B	$A \cdot \overline{B}$ plus $(A + B)$	$A \cdot \overline{B}$ plus $(A + B)$ plus 1
	L	H	H	L	$A \oplus B$	A plus B	A plus B plus 1
	H	H	H	L	$A + B$	$A + B$	$A + B$ plus 1
	L	L	L	H	$\overline{A + B}$	A plus $(A + \overline{B})$	A plus $(A + \overline{B})$ plus 1
	H	L	L	H	$\overline{A \oplus B}$	A minus B minus 1	A minus B
	L	H	L	H	$\overline{B}$	$A \cdot B$ plus $(A + \overline{B})$	$A \cdot B$ plus $(A + \overline{B})$ plus 1
	H	H	L	H	$A + \overline{B}$	$A + \overline{B}$	$A + \overline{B}$ plus 1
	L	L	H	H	Logic "0"	A plus A $(2 \times A)$	A plus A $(2 \times A)$ plus 1
	H	L	H	H	$A \cdot B$	A plus $A \cdot \overline{B}$	A plus $A \cdot \overline{B}$ plus 1
	L	H	H	H	$A \cdot \overline{B}$	A plus $A \cdot B$	A plus $A \cdot B$ plus 1
	H	H	H	H	A	A	A plus 1
c. A All Input Data Inverted; B Input Data True							
	L	L	L	L	$\overline{A}$	A	A plus 1
	H	L	L	L	$\overline{A} \cdot B$	$A + \overline{B}$	$A + \overline{B}$ plus 1
	L	H	L	L	$\overline{A + B}$	$A + B$	$A + B$ plus 1
	H	H	L	L	Logic "0"	minus 1 (2s comp.)	Zero
	L	L	H	L	$\overline{A} + B$	A plus $A \cdot B$	A plus $A \cdot B$ plus 1
	H	L	H	L	B	$A \cdot B$ plus $(A + \overline{B})$	$A \cdot \overline{B}$ plus $(A + B)$ plus 1
	L	H	H	L	$\overline{A \oplus B}$	A plus B	A plus B plus 1
	H	H	H	L	$A \cdot B$	$A \cdot B$ minus 1	$A \cdot B$
	L	L	L	H	$\overline{A} \cdot \overline{B}$	A plus $A \cdot \overline{B}$	A plus $A \cdot B$ plus 1
	H	L	L	H	$A \oplus B$	A minus B minus 1	A minus B
	L	H	L	H	$\overline{B}$	$A \cdot \overline{B}$ plus $(A + B)$	$A \cdot \overline{B}$ plus $(A + B)$ plus 1
	H	H	L	H	$A \cdot \overline{B}$	$A \cdot \overline{B}$ minus 1	$A \cdot \overline{B}$
	L	L	H	H	Logic "1"	A plus A $(2 \times A)$	A plus A $(2 \times A)$ plus 1
	H	L	H	H	$A + B$	A plus $(A + \overline{B})$	A plus $(A + \overline{B})$ plus 1
	L	H	H	H	$A + \overline{B}$	A plus $(A + B)$	A plus $(A + B)$ plus 1
	H	H	H	H	A	A minus 1	A
d. A Input Data True; B Input Date Inverted							

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 2)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 3)	−0.5V to +7.0V
Input Current (Note 3)	−30 mA to +5.0 mA
Voltage Applied to Output	
in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
3-STATE Output	−0.5V to +5.5V
Current Applied to Output	
in LOW State (Max)	twice the rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	4000V

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

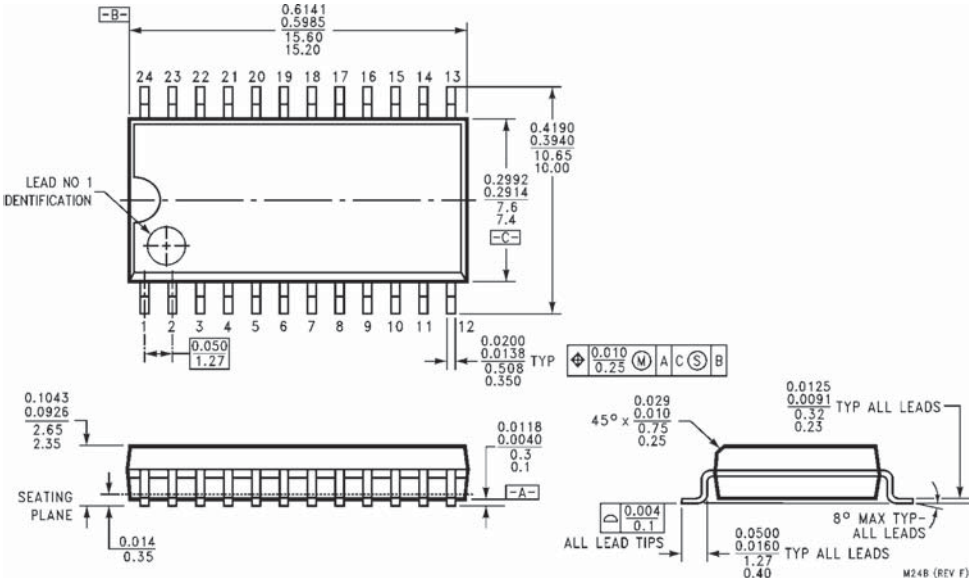
Note 2: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 3: Either voltage limit or current limit is sufficient to protect inputs.

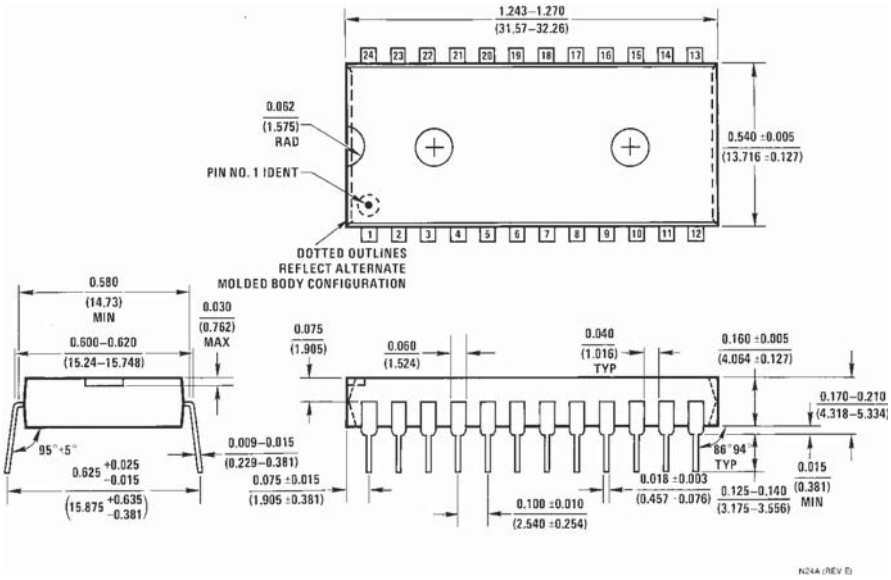
DC Electrical Characteristics

Symbol	Parameter		Min	Typ	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	10% V_{CC}	2.5			V	Min	I_{OH} = −1 mA
		5% V_{CC}	2.7					I_{OH} = −1 mA
V_{OL}	Output LOW Voltage	10% V_{CC}			0.5	V	Min	I_{OL} = 20 mA
I_{IH}	Input HIGH Current				5.0	µA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test				7.0	µA	Max	V_{IN} = 7.0V
I_{CEX}	Output HIGH Leakage Current				50	µA	Max	$V_{OUT} = V_{CC}$ ($\overline{F}_n$, $\overline{G}$, $\overline{P}$, C_{n+4})
V_{ID}	Input Leakage Test		4.75			V	0.0	I_{ID} = 1.9 µA All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current				3.75	µA	0.0	V_{IOD} = 150 mV All Other Pins Grounded
I_{IL}	Input LOW Current				−0.6	mA	Max	V_{IN} = 0.5V (M)
					−1.8			V_{IN} = 0.5V ($\overline{A}_0$, $\overline{A}_1$, $\overline{A}_3$, $\overline{B}_0$, $\overline{B}_1$, $\overline{B}_3$)
					−2.4			V_{IN} = 0.5V (S_n, $\overline{A}_2$, $\overline{B}_2$)
					−3.0			V_{IN} = 0.5V (C_n)
I_{OS}	Output Short-Circuit Current		−60		−150	mA	Max	V_{OUT} = 0V ($\overline{F}_n$, $\overline{G}$, $\overline{P}$, C_{n+4})
I_{OHC}	Open Collector, Output OFF Leakage Test				250	µA	Min	$V_O = V_{CC}$ (A = B)
I_{CCH}	Power Supply Current			43	65.0	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current			43	65.0	mA	Max	V_O = LOW

Physical Dimensions inches (millimeters) unless otherwise noted



24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M24B

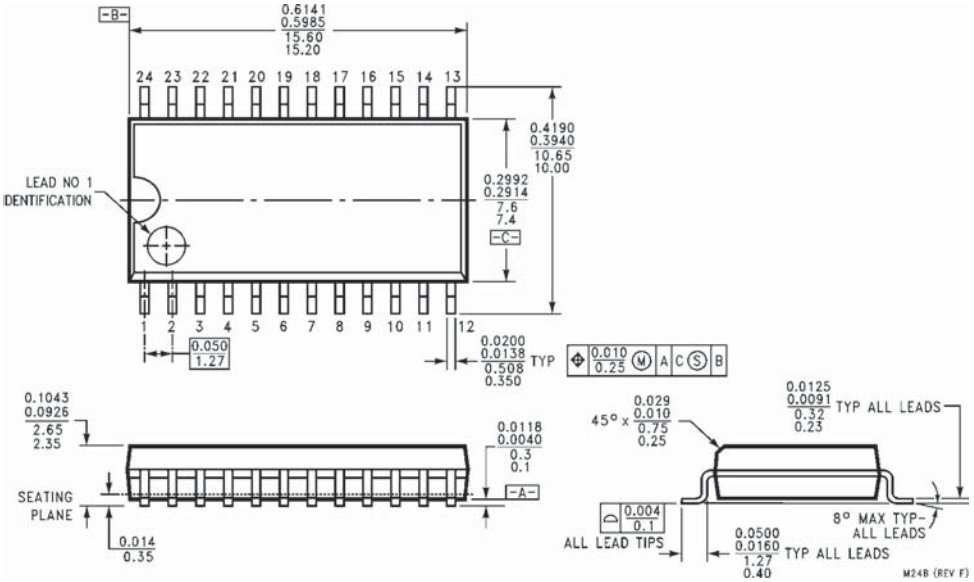


24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-010, 0.600 Wide
Package Number N24A

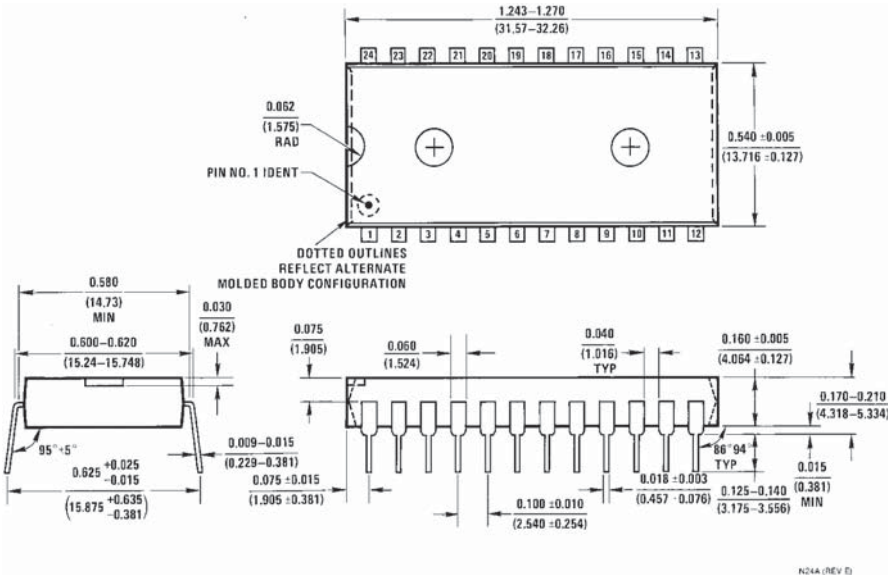
AC Electrical Characteristics

Symbol	Parameter		$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF			$T_A = -55°C$ to $+125°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF		$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF		Units
	Path	Mode	Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}	Propagation Delay		3.0	6.4	8.5	3.0	10.0	3.0	9.5	ns
t_{PHL}	C_n to C_{n+4}		3.0	6.1	8.0	3.0	9.5	3.0	9.0	
t_{PLH}	Propagation Delay		5.0	10.0	13.0	5.0	15.5	5.0	14.0	ns
t_{PHL}	$\overline{A}$ or $\overline{B}$ to C_{n+4}	Sum	4.0	9.4	12.0	3.5	16.5	4.0	13.0	
t_{PLH}	Propagation Delay		5.0	10.8	14.0	5.0	17.0	5.0	15.0	ns
t_{PHL}	$\overline{A}$ or $\overline{B}$ to C_{n+4}	Dif	5.0	10.0	13.0	4.0	15.0	5.0	14.0	
t_{PLH}	Propagation Delay		3.0	6.7	8.5	2.5	16.0	3.0	9.5	ns
t_{PHL}	C_n to $\overline{F}$	Any	3.0	6.5	8.5	2.5	12.0	3.0	9.5	
t_{PLH}	Propagation Delay		3.0	5.7	7.5	2.5	9.0	3.0	8.5	ns
t_{PHL}	$\overline{A}$ or $\overline{B}$ or $\overline{G}$	Sum	3.0	5.8	7.5	2.5	9.5	3.0	8.5	
t_{PLH}	Propagation Delay		3.0	6.5	8.5	2.5	11.5	3.0	9.5	ns
t_{PHL}	$\overline{A}$ or $\overline{B}$ to $\overline{G}$	Dif	3.0	7.3	9.5	2.5	11.0	3.0	10.5	
t_{PLH}	Propagation Delay		3.0	5.0	7.0	2.5	8.5	3.0	8.0	ns
t_{PHL}	$\overline{A}$ or $\overline{B}$ to $\overline{P}$	Sum	3.0	5.5	7.5	3.0	9.5	3.0	8.5	
t_{PLH}	Propagation Delay		3.0	5.8	7.5	2.5	11.0	3.0	8.5	ns
t_{PHL}	$\overline{A}$ or $\overline{B}$ to $\overline{P}$	Dif	4.0	6.5	8.5	3.0	11.0	4.0	9.5	
t_{PLH}	Propagation Delay		3.0	7.0	9.0	3.0	14.5	3.0	10.0	ns
t_{PHL}	$\overline{A}_i$ or $\overline{B}_i$ to $\overline{F}_i$	Sum	3.0	7.2	10.0	3.0	14.5	3.0	10.0	
t_{PLH}	Propagation Delay		3.0	8.2	11.0	3.0	17.5	3.0	12.0	ns
t_{PHL}	$\overline{A}_i$ or $\overline{B}_i$ to $\overline{F}_i$	Dif	3.0	5.0	11.0	3.0	14.5	3.0	12.0	
t_{PLH}	Propagation Delay		4.0	8.0	10.5	3.5	16.5	4.0	11.5	ns
t_{PHL}	Any $\overline{A}$ or $\overline{B}$ to Any $\overline{F}$	Sum	4.0	7.8	10.0	4.0	13.5	4.0	11.0	
t_{PLH}	Propagation Delay		4.5	9.4	12.0	3.5	17.5	4.5	13.0	ns
t_{PHL}	Any $\overline{A}$ or $\overline{B}$ to Any $\overline{F}$	Dif	3.5	9.4	12.0	3.0	14.0	3.5	13.0	
t_{PLH}	Propagation Delay		4.0	6.0	9.0	3.5	14.5	4.0	10.0	ns
t_{PHL}	$\overline{A}$ or $\overline{B}$ to $\overline{F}$	Logic	4.0	6.0	10.0	3.0	15.5	4.0	11.0	
t_{PLH}	Propagation Delay		11.0	18.5	27.0	8.0	35.0	11.0	29.0	ns
t_{PHL}	$\overline{A}$ or $\overline{B}$ to A = B	Dif	6.0	9.8	12.5	5.5	21.0	6.0	13.5	

Physical Dimensions inches (millimeters) unless otherwise noted



24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M24B



24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-010, 0.600 Wide
Package Number N24A