CMPE-160 DSD1

Laboratory Exercise 06

Binary Addition and Subtraction Circuits

By submitting this report, I attest that its contents are wholly my individual writing about this exercise and that they reflect the submitted code. I further acknowledge that permitted collaboration for this exercise consists only of discussions of concepts with course staff and fellow students. Other than code provided by the instructor for this exercise, all code was developed by me.

Oliver Vinneras
21 February 2021

Lab Section:	3
Instructor:	Mr. Lange
TA:	Henry Bang
	Harrison Barnes
	Ian Chasse
	Shubhang Mehrotra
Lecture Section:	1
Lecture Instructor:	Mr. Cliver

Abstract

The purpose of this exercise was to design and implement binary addition and subtraction using a 1 bit full adder, built using basic logic gates, and a 4 bit full adder. These full adders are used for 1 bit addition/subtraction and 4 bit addition/subtraction. The design and implementation of both the 1 bit full adder and 4 bit full adder was successful and a physical representation of this boolean arithmetic circuit.

Design Methodology

A full adder has two inputs, A and B, and a Carry In that determines the Sum and Carry Out values. If the full adder has more than one bit, the Carry Out becomes the Carry In for the next bit.

Table 1: Karnaugh Map for Sum

		AB			
		00	01	11	10
Cin	0	0	1	0	1
	1	1	0	1	0

The Karnaugh Map shown in Table 1 shows the Sum output of A B Cin. This K-Map can be written as the boolean expression $S = A'B'C + A'BC' + ABC + AB'C'$. This can be simplified to $S = C\ XOR\ (A\ XOR\ B)$.

Table 2: Karnaugh Map for Cout

		AB			
		00	01	11	10
Cin	0	0	0	1	0
	1	0	1	1	1

The Karnaugh Map in Table 2 shows the Carry Out output of A B Cin. If written as a boolean expression, this K-Map is the same as $Cout = AB + BC + AC$.

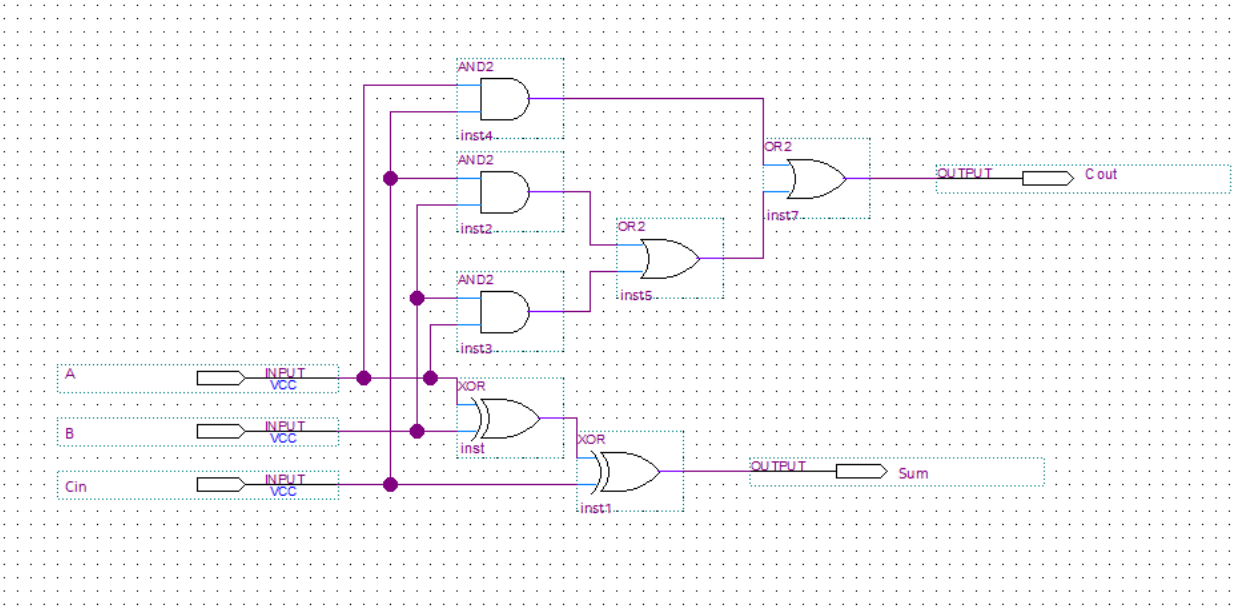


Figure 1: 1 Bit Full Adder Diagram

The block diagram shown in Figure 1 shows the logic gates used to build a 1 bit full adder. In this case, an overflow error would not be accounted as a 1 bit full adder can only account for 1 bit.

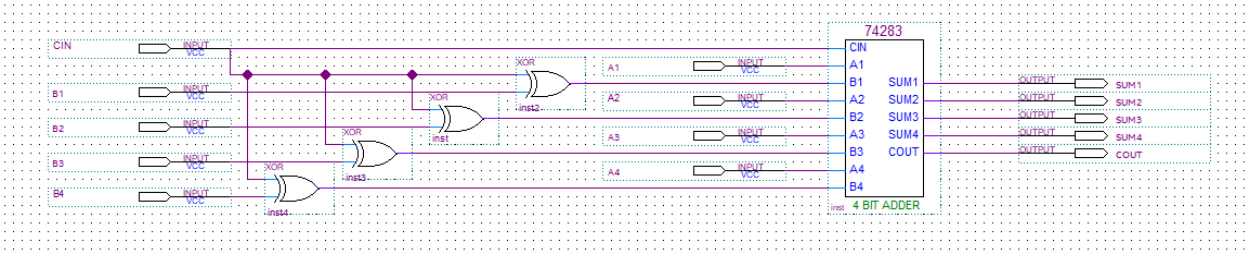


Figure 2: 4 Bit Adder/Subtracter

The 4 bit full adder/subtracter shown in Figure 2 accurately adds, subtracts the inputs. These inputs group A1, A2, A3, and A4 together as one binary number, and B1, B2, B3, and B4 together as the other binary number. One of the uses of the Carry In is to determine if the circuit is an adder or a subtracter. This is referred to as the Control. If the Control is a 0, the full adder is doing addition, and if the Carry In is a 1, the full adder is subtracting. This was accounted for in the implementation of this 4 bit full adder by using the Control as an input that would change if the adder was adding or subtracting.

Results and Analysis

When the 1 bit full adder block diagram was simulated, as shown in Figure 3, the waveforms for Sum and Cout were shown. These waveforms aligned with the Karnaugh Maps, Table 1 and Table 2. After implementing the 1 bit full adder, the outputs also aligned with the waveforms shown in Figure 3.

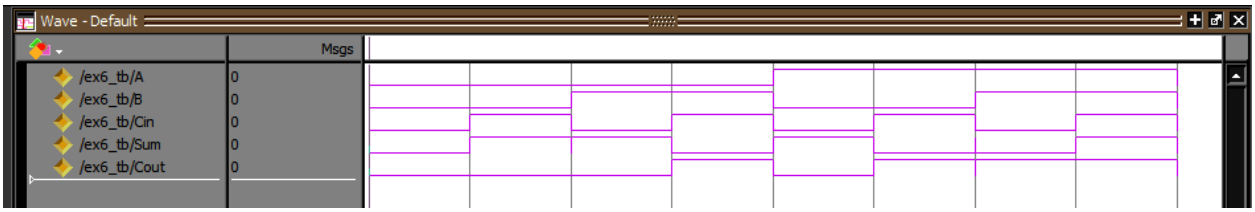


Figure 3: 1 Bit Full Adder Simulation

When the 4 bit full adder was designed and implemented, it was compared to Table 3 and Table 4. These tables were used as test values to ensure that the 4 bit full adder was properly implemented. By converting each binary value to 2's complement, the binary values were either added or subtracted. If the value returned was greater than the given range of -2^{N-1} to $2^N - 1$, then there was an overflow that was not accounted for.

Table 3: Four-bit Binary Addition

A3 A2 A1 A0	B3 B2 B1 B0	C4	F3 F2 F1 F0	A + B = F
S7 S6 S5 S4	S3 S2 S1 S0	L4	L3 L2 L1 L0	(Decimal)
1 0 1 0	0 0 1 1	0	1 1 0 1	-6 + 3 = -3
1 1 1 1	1 1 1 1	1	1 1 1 0	-1 + -1 = 0
1 1 1 1	0 1 1 0	1	0 1 1 1	-1 + 6 = 5
0 1 1 1	0 0 1 1	0	1 0 1 0	7 + 3 = -6
0 1 0 1	1 0 1 0	0	1 1 1 1	5 + -6 = -1

The difference between Table 3 and Table 4 is that Table 3 uses 4 bit binary addition, while Table 3 uses 4 bit binary subtraction. This difference is shown in Figure 2, as Cin is used as the determinant. When the Carry In, in this case referred to as the Control, is a 0, then the full adder adds. When the Control is a 1, the full adder subtracts.

Table 4: Four-bit Binary Subtraction

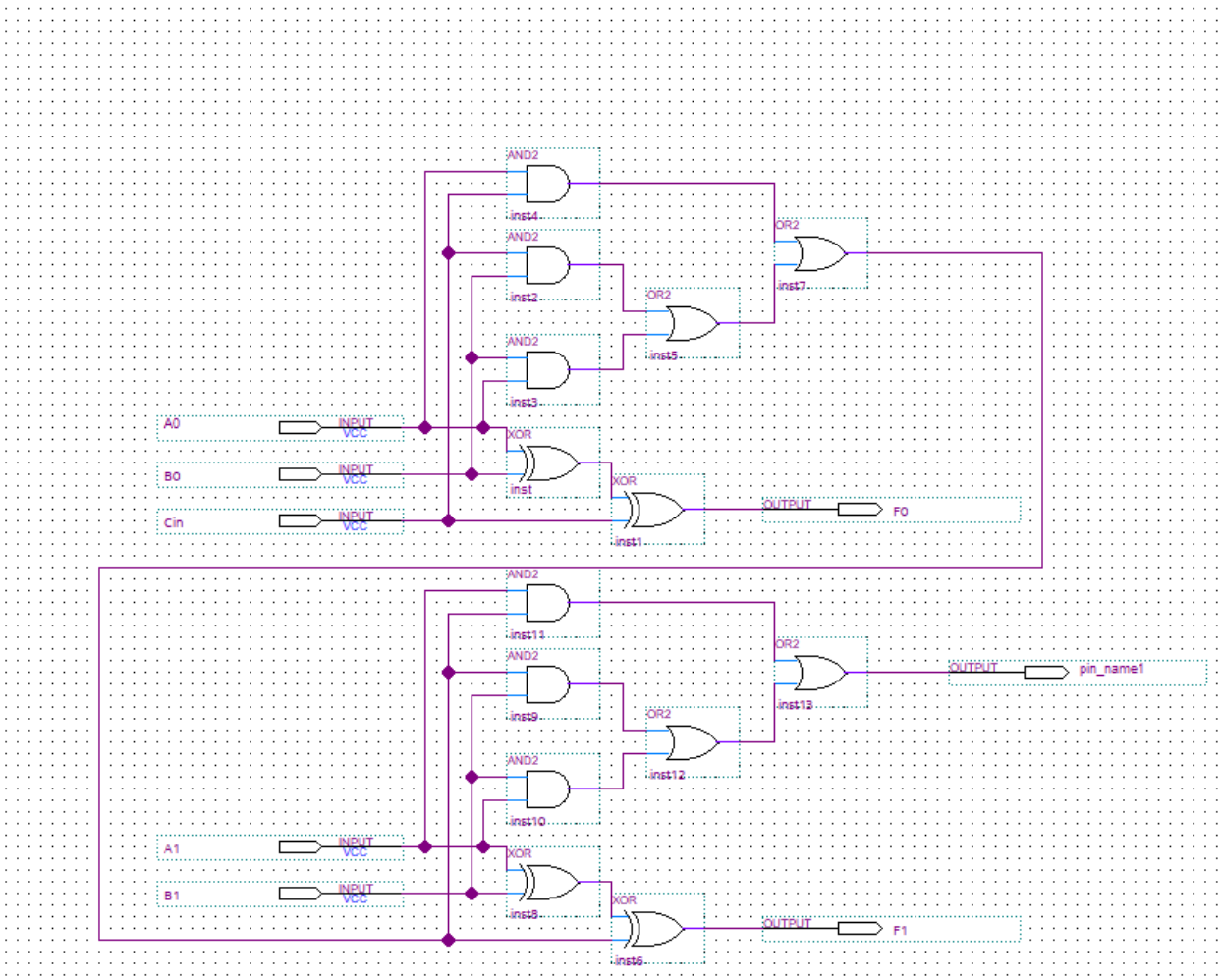
A3 A2 A1 A0	B3 B2 B1 B0	C4	F3 F2 F1 F0	A + B = F
S7 S6 S5 S4	S3 S2 S1 S0	L4	L3 L2 L1 L0	(Decimal)
1 0 1 0	0 0 1 1	1	0 1 1 1	-6 - 3 = -9
1 1 1 1	1 1 1 1	1	0 0 0 0	-1 - 1 = 0
1 1 1 1	0 1 1 0	1	1 0 0 1	-1 - 6 = -7
0 1 1 1	0 0 1 1	1	0 1 0 0	7 - 3 = 4
0 1 0 1	1 0 1 0	0	1 0 1 1	5 + 6 = 11

Conclusion

This exercise was successful and showed the proper relationship between physical addition and subtraction circuits and theoretical ones. When modelling and simulating a 1 bit full adder from a Karnaugh Map for the Sum and a Karnaugh Map for the Cout, the output was the same as when this 1 bit full adder was implemented.

Questions

1.

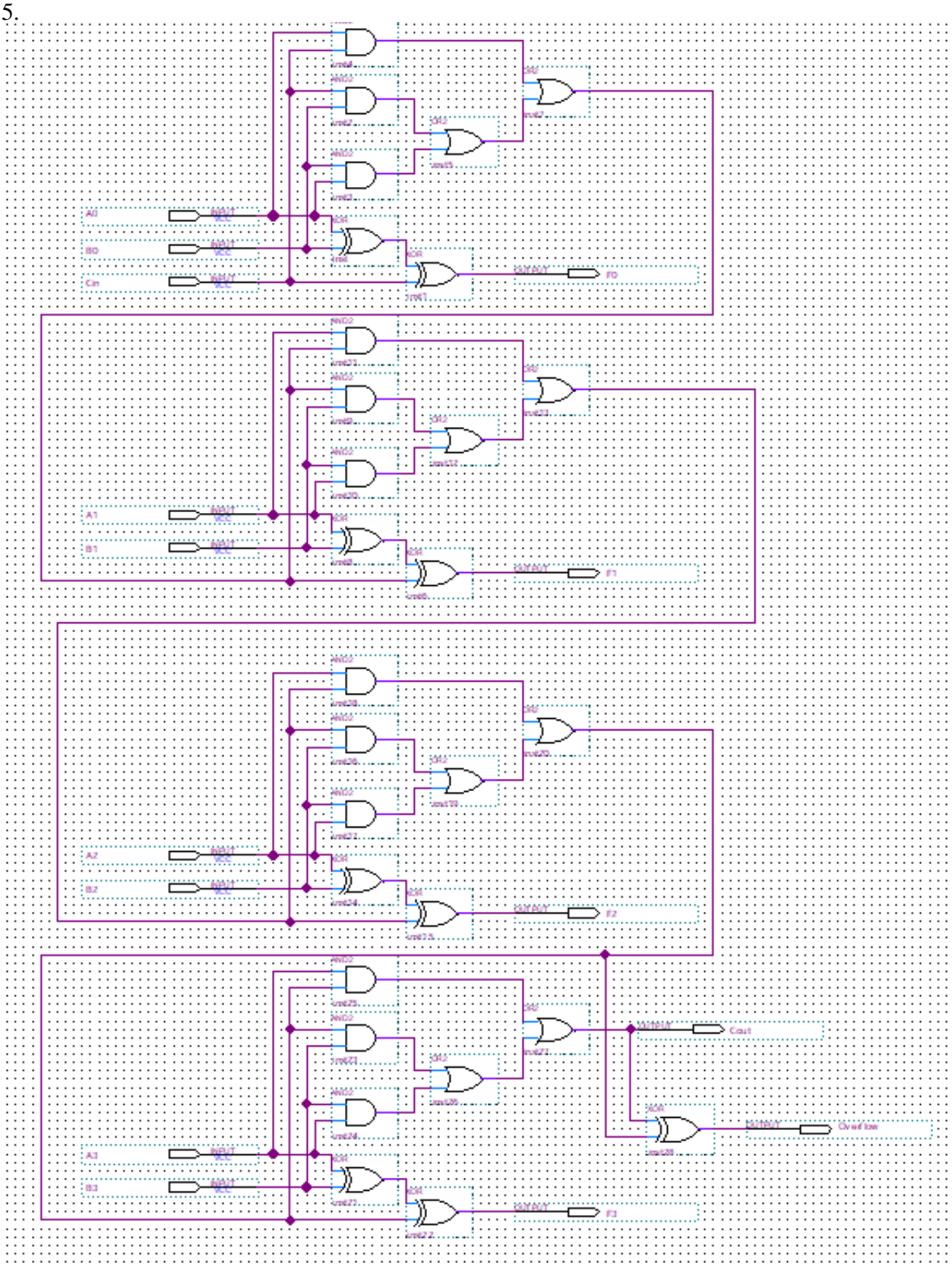


2. If the final answer is out of the bounds from -2^{N-1} to $2^N - 1$, then there will be overflow.

3. Some boolean expressions equate to using more that 4 bits.

4. Then the overflow would be accounted for as there is another output meant for the overflow.

5.



Exercise 6: Binary Addition and Subtraction Circuits

Student's Name: Oliver Vimarcs Section: 3

Prelab		Point Value	Points Earned	Comments
Part 1	K-maps	2	2	IC
	Boolean transformations	4	4	2/16
	Correct Boolean expressions	2	2	✓
	Schematic diagram	4	4	
	Simulations	4	4	
Part 2	Schematic diagram	4	4	

Demo		Point Value	Points Earned	Date
Demo	1-bit full adder	20	20	02/16. SM
	4-bit adder/-subtracter	20	20	02/16 SM

To receive any grading credit students must earn points for both the demonstration and the report.

Exercise 6: Binary Addition and Subtraction Circuits

Report		Point Value	Points Earned	Comments
Abstract		4		
Design Methodology	K-maps / Boolean transformations	3		
	1-bit FA circuit diagram	2		
	Discussion of add/subtract control	3		
	4-bit adder/-subtracter circuit diagram	2		
Results and Analysis	1-bit full adder Simulation	2		
	4-bit adder/-subtracter result tables	3		
Conclusion		4		
Questions	Q1	4		
	Q2	2		
	Q3	3		
	Q4	2		
	Q5	3		
Writing Composition		3		
Total for prelab, demo, and report		100		