Exercise 6: Binary Addition and Subtraction Circuits

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Section: 3

Prelab		Point Value	Points Earned	Comments
Part 1	K-maps	2	2	IC
	Boolean transformations	4	4	2//6
	Correct Boolean expressions	2	2	
	Schematic diagram	4	4	
	Simulations	4	Y	V
Part 2	Schematic diagram	4	4	

Demo		Point Value	Points Earned	Date
Demo	1-bit full adder	20	20	02/16. SM
Dome	4-bit adder/- subtracter	20	20	02/16 SY

To receive any grading credit students must earn points for both the demonstration and the report.

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R	Point Value	Points Earned	Comments	
Abstract		4		
Design	K-maps / Boolean trans- formations	3		
Methodology	1-bit FA circuit diagram	2		
	Discussion of add/subtract control	3 .		
Year	4-bit adder/- subtracter circuit diagram	2		
Results and Analysis	1-bit full adder Simulation	2		
	4-bit adder/- subtracter result tables	3	F 50	
Conclusion		4		The same of the sa
ce zi i c i c	Q1	4	5 724	7
	Q2	2		
Questions	Q3	3		
	Q4	2		,
	Q5	3		
Writing Comp	3		40.70	
Total for prelab,	100			