Exercise 5: Combinational Logic Circuit Design Using Karnaugh Map Simplification

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Prelab		Point Value	Points Earned	Comments
Part 1	K-maps	4	4	29 JKL
	Correct Boolean expressions	4	4	
Part 2	Schematic diagram	4	4	
	Simulations	4	4	
	EGC	4	4	

Demo		Point Value	Points Earned	Date
Demo	Test Bench	20	20	JKL
	Circuit Construction	20	20	JKL 2/9

To receive any grading credit students must earn points for both the demonstration and the report.

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Report		Point Value	Points Earned	Comments
Abstract		4		
Design Methodology	Karnaugh maps	5		
	Reduced SOP expression	5		
	Reduced POS expression	5		
	Schematic diagram	4		
Results and Analysis	SOP waveforms	2		
	POS waveforms	2		
Conclusion		5		
Question		5		
Writing Composition		3		
Total for prelab, demo, and report		100		