# CMPE-160 DSD1

## Laboratory Exercise 04

## Combinational Logic Circuit Design Using Boolean Algebra Simplification

By submitting this report, I attest that its contents are wholly my individual writing about this exercise and that they reflect the submitted code. I further acknowledge that permitted collaboration for this exercise consists only of discussions of concepts with course staff and fellow students. Other than code provided by the instructor for this exercise, all code was developed by me.

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**Abstract**

The purpose of this exercise was to simplify a Boolean algebra expression and implement this expression with a combinational logic circuit. A truth table was created with inputs C, N0 and N1, and outputs W, X, Y, and Z. Depending on the value of C, a mathematical operation was selected to get the values of W, X, Y and Z. If C was 0, the decimal value of each binary row of inputs was run through the equation $N^2$ and that output was converted to binary and became the values in the truth table for W, X, Y and Z. If C was 1, this process was repeated but instead using the equation $5N$ for outputs W, X, Y and Z. The exercise was successful and the circuit confirmed the values in the truth table.

**Design Methodology**

A truth table, shown in Table 1.1, was used to compute the inputs and the outputs of the logic circuit. When C was 0, the decimal value for the inputs was multiplied by itself using the equation $n^2$, and when C was 1, the decimal value of the inputs was multiplied by 5 using the equation $5N$.

Table 1.1: Truth table for operations $N^2$ and $5N$

| C | N1 | N0 | W | X | Y | Z |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 |

To simplify the W output, as shown in (1), De Morgan's Law is used. By using the complement rule and the absorption rule, Equation W can be simplified.

$$\begin{aligned} W &= (C'N1N0) + (CN1N0') + (CN1N0) \\ &= CN1 + N1N0 \end{aligned} \quad \text{Complement and Absorption} \tag{1}$$

As in (1), the equation to simplify (2) uses the complement rule to simplify $CN1'N0 + CN1N0$ to $CN0$.

$$\begin{aligned} X &= (C'N1N0') + (CN1'N0) + (CN1N0) \\ &= CN0 + C'N1N0' \end{aligned} \quad \text{Complement} \tag{2}$$

To simplify Y, (3), the complement rule is used to simplify $CN1N0' + CN1N0$ to $CN1$ because $N0' + N0 = 1$.

$$\begin{aligned} Y &= (CN1N0') + (CN1N0) \\ &= CN1 \end{aligned} \quad \text{Complement} \tag{3}$$

Z, (4), uses the complement rule twice as $C'N1' + C'N1 = 1$ and $CN1' + CN1 = 1$, meaning that the only term left over is $N0 + N0 = N0$ .

$$\begin{aligned} Z &= (C'N1'N0) + (C'N1N0) + (CN1'N0) + (CN1N0) \\ &= N0 \end{aligned} \quad \text{Complement} \tag{4}$$

These expressions were modeled into a schematic made in Quartus, shown in Figure 1.1. This was tested using Modelsim and aligned with the truth table shown in Table 1.1.

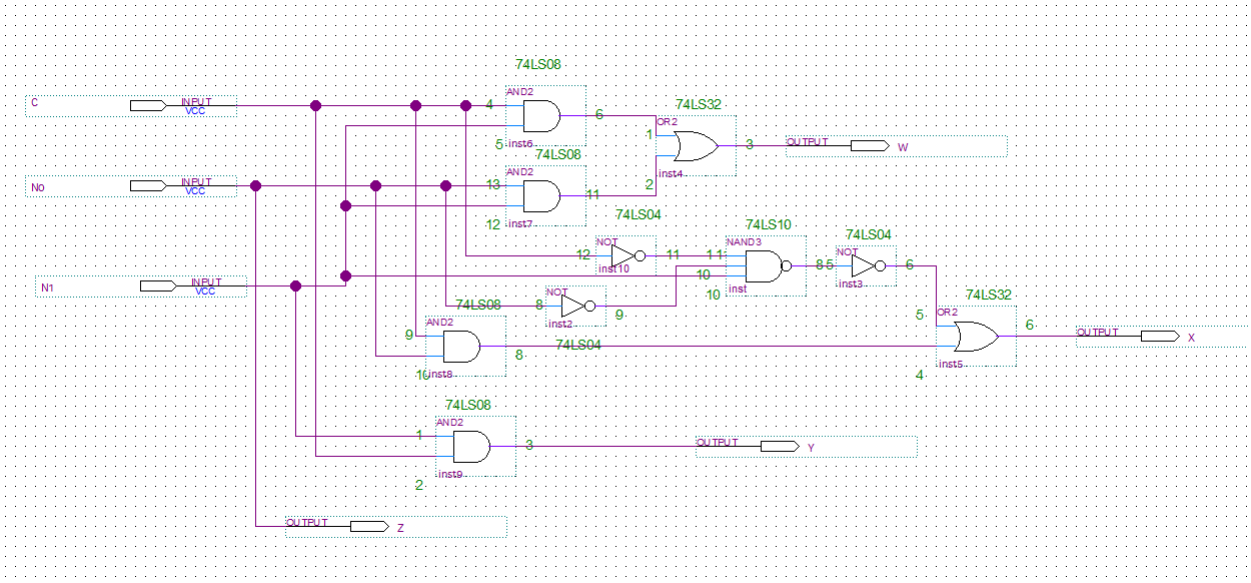


Figure 1.1: Simplified Boolean expression schematic

## Results

The circuit was tested using two-input AND gates, an inverter on a 3-input NAND gate, and 2-input OR gates. When the outputs went to 4 LEDs, the LEDs lit up when W, X, Y, or, Z was a 1. This aligned with the truth table shown in Table 1.1, the model made in Quartus, and the simulation created in Modelsim.

## Conclusion

The exercise was successful in simplifying a Boolean algebra expression and implementing it with a combinational logic circuit. The functionality of the built circuit was compared to the truth table, Table 1.1, the Quartus schematic, and the Modelsim simulation of the circuit. They all aligned and returned the same outputs for the given inputs.

## Questions

1.

a) 32 gates

b) 8 gates

2.

a) 9 chips

b) 4 chips

Exercise 4: Combinational Logic Circuit Design Using Boolean Algebra Simplification

Student's Name: Oliver Winters Section: 3

| Prelab | | Point Value | Points Earned | Comments |
|---|---|---|---|---|
| Part 1 | Table completed | 3 | 3 | 2/2 KB |
| | Expressions correct | 2 | 2 | |
| Part 2 | Correct simplified equations | 1 | 1 | 2/2 KB |
| | Steps shown | 2 | 0 | |
| | Boolean properties shown | 2 | 0 | |
| Part 3 | Correct schematic | 3 | 3 | 2/2 KB |
| | Pin and chip numbers | 1 | 1 | 2/2 KB |
| | Correct simulation | 4 | 4 | 2/2 KB |
| | Parts placement diagram | 2 | 2 | 2/2 KB |

| Demo | | Point Value | Points Earned | Date |
|---|---|---|---|---|
| Demo | Two fully functional output pins | 20 | 20 | 2/2 JSL |
| | Additional two fully functional output pins | 20 | 20 | |

To receive any grading credit students must earn points for both the demonstration and the report.

Exercise 4: Combinational Logic Circuit Design Using Boolean Algebra Simplification

| Report | | Point Value | Points Earned | Comments |
|---|---|---|---|---|
| Abstract | | 5 | | |
| Design Methodology | Truth table | 4 | | |
| | Boolean expressions | 4 | | |
| | Correct simplified equations | 1 | | |
| | Steps shown | 2 | | |
| | Boolean properties shown | 2 | | |
| | Schematic | 4 | | |
| Results and Analysis | Discussion | 5 | | |
| Conclusion | | 3 | | |
| Questions | EGC | 3 | | |
| | Chip count | 3 | | |
| Writing Composition | | 4 | | |
| Total for prelab, demo, and report | | 100 | | |