CMPE-160 DSD1

Laboratory Exercise 11

Modeling of Combinational Circuits Using Concurrent and Sequential Statements

By submitting this report, I attest that its contents are wholly my individual writing about this exercise and that they reflect the submitted code. I further acknowledge that permitted collaboration for this exercise consists only of discussions of concepts with course staff and fellow students. Other than code provided by the instructor for this exercise, all code was developed by me.

Oliver Vinneras
6 April 2022

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Abstract

The purpose of this exercise was to learn how to write structural, dataflow, and behavioral models in VHDL by modelling two 4:1 multiplexers. These models were created as architectures of the DM74LS153 chip, meaning that each architecture created a model of the two 4:1 multiplexers. All of these architectures were then simulated using the same testbench.

Design Methodology

A 4:1 multiplexer was created using 3 inverters, 4 4-input AND gates, and one 4-input OR gate. All of these were modelled as individual entity architecture pairs in VHDL to create the 4:1 multiplexer. Two 4:1 multiplexer components were used to create a DM74LS153 chip.

Results and Analysis

The DM74LS153 chip was tested using a testbench that simulated a dataflow architecture, behavioral architecture and a structural architecture of the DN74LS153 chip. Figure 1 shows the results of the first set of data values used to test the functionality of the circuit.

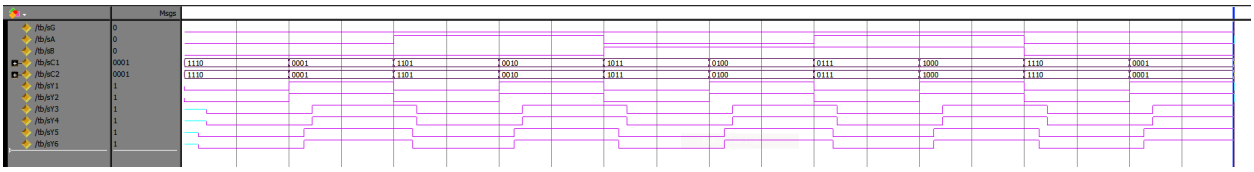


Figure 1: Test set 1

Figure 2 shows the results of the second set of test values used to further ensure that the circuit was modelled correctly.

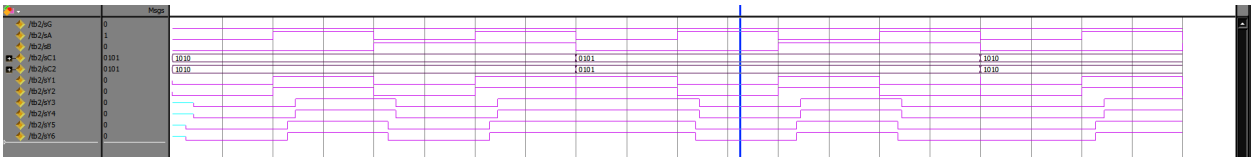


Figure 2: Test set 2

Figure 3 shows the results of the third set of values, which only changes the strobe input from 0 to 1, which disables the multiplexers and causes all outputs to be 0.

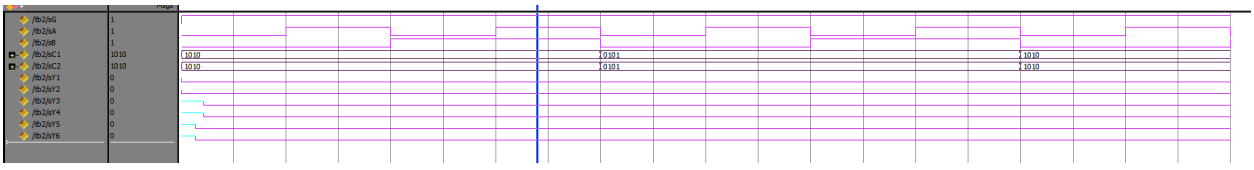


Figure 3: Test set 3

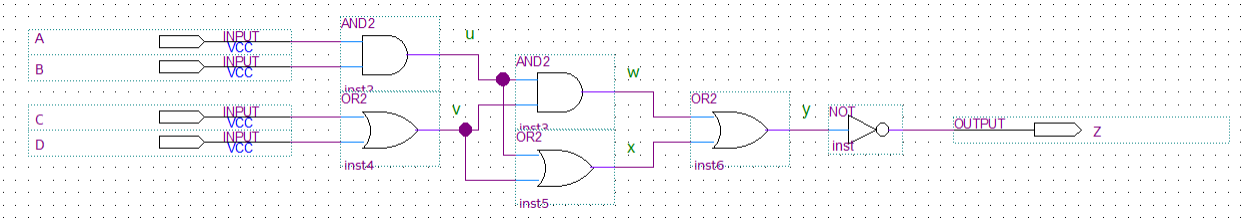
All three test cases shown in Figures 1, 2, and 3 show accurate results that the DM74LS153 is functional and modelled correctly.

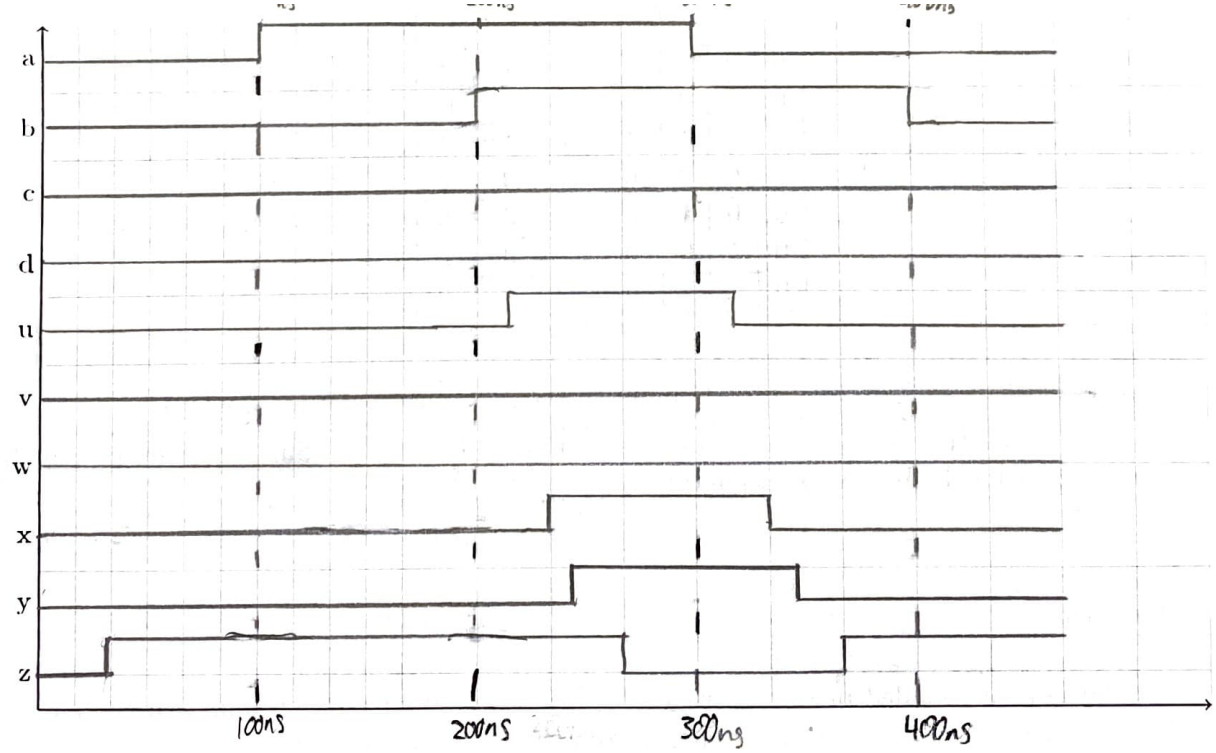
Conclusion

After modelled, the DM74LS153 chip, built using two 4:1 multiplexers, which were built using 3 inverters, 4 4-input AND gates, and a 4-input OR gate, was simulated using three different test cases that showed the correct functionality of the DM74LS153 chip.

Questions

Delta delay is the small delay when values are assigned that changes when signals dependent on other signals get their values.





Exercise 11: Modeling of Combinational Circuits Using Concurrent and Sequential Statements

Student's Name: Oliver Vinneras Section: 3

Prelab		Point Value	Points Earned	Comments
Prelab	Entity declaration	5	5	HB 03/30/2022
	Data flow architecture	5	5	
	Behavioral architecture	5	5	
	Structural architecture	5	5	

Demo		Point Value	Points Earned	Date
Demo	Test case 1	15	15	SKL 3/30
	Test case 2	15	15	3/30HB
	Test case 3	10	10	3/30HB

To receive any grading credit students must earn points for both the demonstration and the report.

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Report		Point Value	Points Earned	Comments
Abstract		3		
Design Methodology	Discussion of circuit functionality	5		
Results and Analysis	Test methodology	3		
	Simluation results	10		
Conclusion		3		
Questions		6		
Writing Composition		3		
Source code	Comments	3		
	Style	4		
Total for prelab, demo, and report		100		