CMPE-160 DSD1

Laboratory Exercise 7

Sequential Circuit Elements

By submitting this report, I attest that its contents are wholly my individual writing about this exercise and that they reflect the submitted code. I further acknowledge that permitted collaboration for this exercise consists only of discussions of concepts with course staff and fellow students. Other than code provided by the instructor for this exercise, all code was developed by me.

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Abstract

The purpose of this exercise was to design and implement basic sequential circuits. This was done by modeling and simulating a D latch with active-low enable and modeling and simulating a rising edge-triggered D flip flop. When modeled, both the D latch and the D flip flop match the expected outputs. When simulated, the D latch and the D flip flop both match their expected results and the results found when they were modeled.

Design Methodology

A table was created, shown as Table 1, to compute the Q and Qn outputs based on En and D. This table was used to compare towards the results of the model, simulation, and the built circuit.

Table 1: D latch with active-low enable

En	D	Q	Qn
0	0	0	1
0	1	1	0
1	X	Q	Qn

The D latch, shown in Figure 1, was modeled and tested using the values from Table 1. When the circuit diagram was built, the results were compared to Table 1. This ensured that a

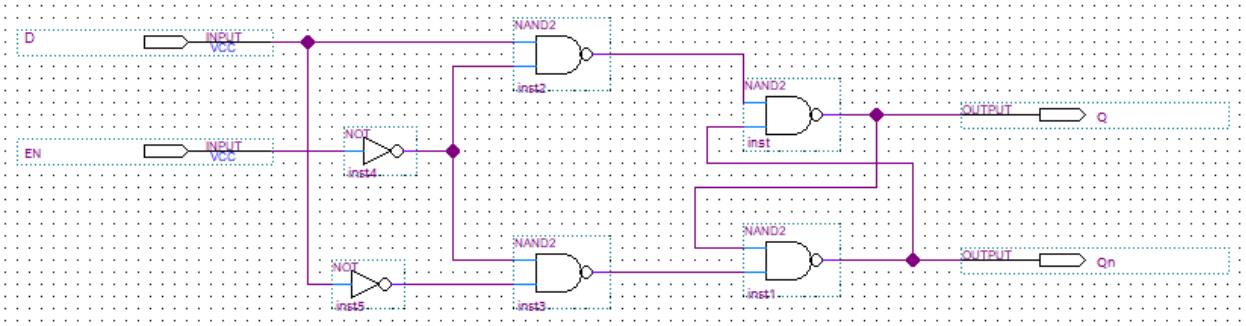


Figure 1: D latch circuit diagram

A table for the rising edge-triggered D flip flop is shown as Table 2. It shows that the outputs change on the rising edge of the clock. If the clock is not at a rising edge, the outputs will hold until the next rising edge and D value.

Table 2: Rising edge-triggered D flip flop

clk	D	Q	Qn
↑	0	0	1
↑	1	1	0
otherwise	X	Q	Qn

The implementation of Table 2 can be shown as Figure 2. A D flip flop consists of two D latches with the second enable coming from the first.

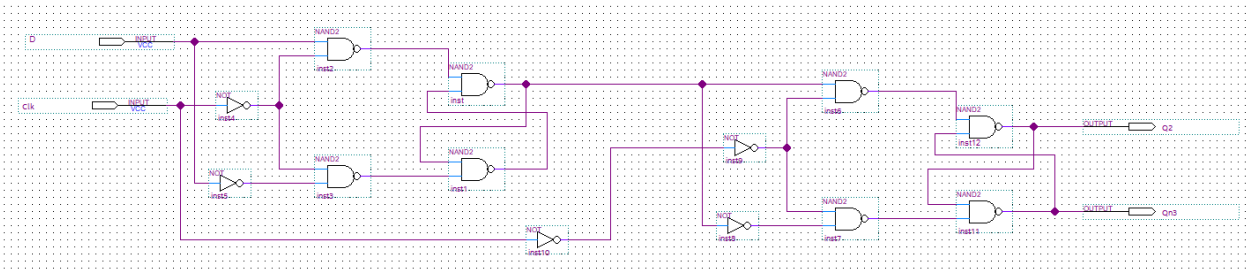


Figure 2: D flip flop circuit diagram

Results and Analysis

The D latch waveform shown in Figure 3 shows the simulation of the D latch and how the outputs are dependant on the rising edge of the enable.

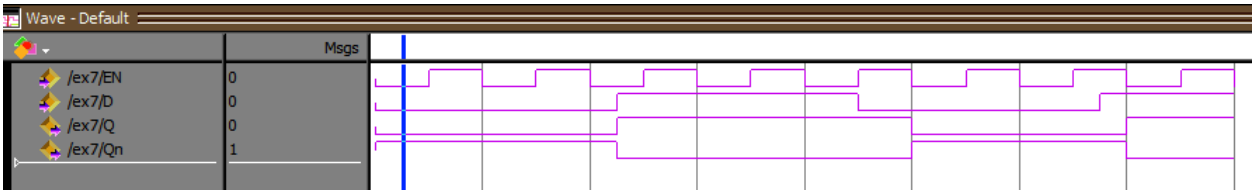


Figure 3: D latch waveform

The waveform shown in Figure 4 shows how the rising edge of the clock affects the outputs. As there is delay between the inputs, Clk and D, the changed output values are not immediately changed.

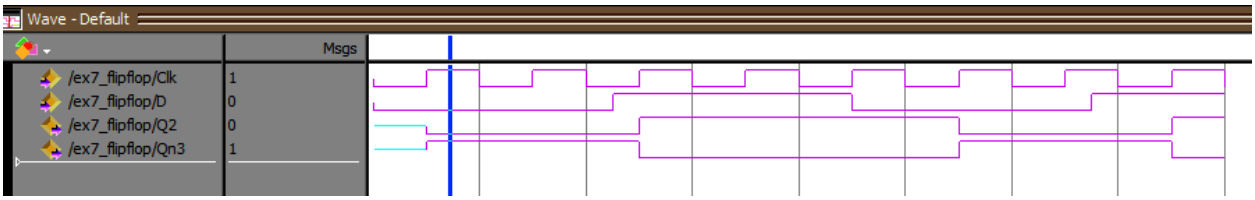


Figure 4: D flip flop waveform

The oscilloscope capture shown as Figure 5 shows the simulation of the implementation of the D flip flop, shown in Figure 2. The output is dependant on the clock used, as the output will only change on the rising edge of the clock.

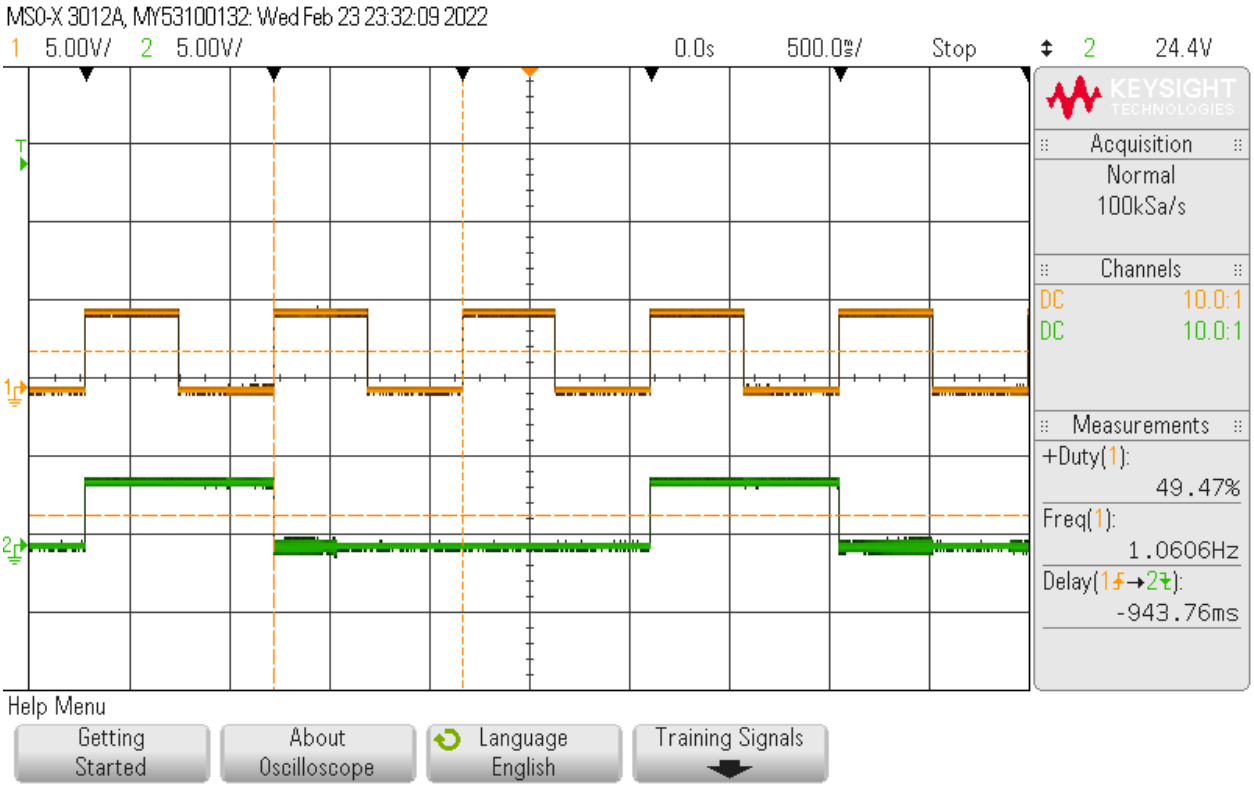


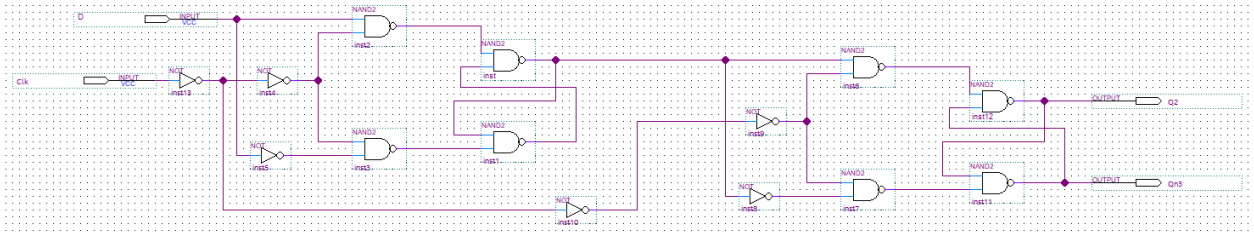
Figure 5: D flip flop oscilloscope

Conclusion

This exercise was successful as all models, implementations, and the results from the circuits built aligned with each other for both the D latch and D flip flop. This was further confirmed by the simulation waveforms of the D latch and D flip flop as they aligned to the Table 1 and Table 2.

Questions

1.



2.
a) 30 ns
b) 25 ns
c) 20 ns
d) 5 ns

Extra Credit

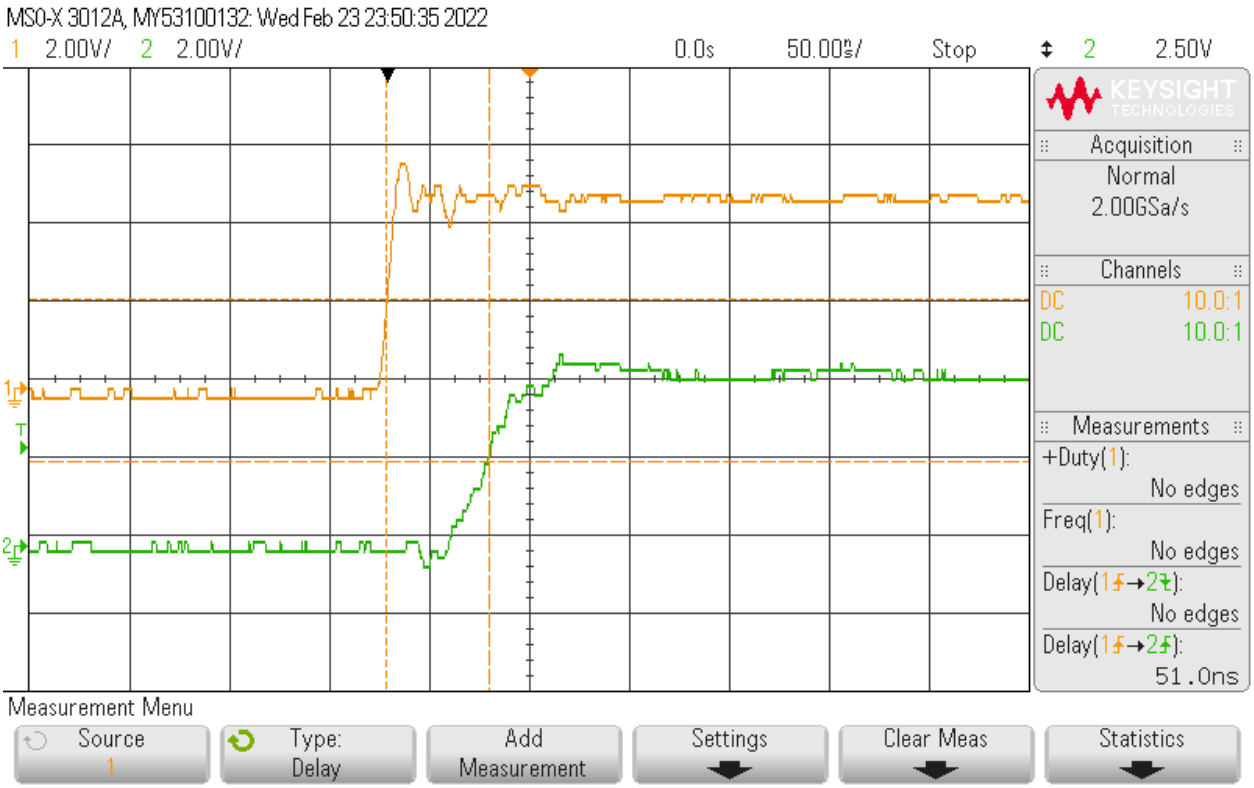


Figure 6: Clock to Q delay

The frequency is 1/51.0