CMPE-160 DSD1

Laboratory Exercise 05

Combinational Logic Circuit Design Using Karnaugh Map Simplification

By submitting this report, I attest that its contents are wholly my individual writing about this exercise and that they reflect the submitted code. I further acknowledge that permitted collaboration for this exercise consists only of discussions of concepts with course staff and fellow students. Other than code provided by the instructor for this exercise, all code was developed by me.

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Abstract

The purpose of this exercise was to use combinational logic principles to write a Sum of Products and a Products of Sums boolean expression based on a Karnaugh Map. After drawing these simplified boolean expressions, the EGC was found and the expression with a lower chip count was built to test this circuit. The Products of Sums expression was built.

Design Methodology

A Karnaugh Map, shown in Table 1, is used to find the minimum Sums of Products and Products of Sums expressions. To find the Sums of Products, each 1 in the K-Map in Table 1 is grouped together. When simplified, the Sums of Products = A'D' + BC + ABD. To find the Products of Sums expression, each 0 is grouped together to create the largest groups with 2^n values in each group. When simplified, Products of Sums = (A + C + D')(A' + C + D)(A' + B).

Table 1: Karnaugh Map for the given boolean expression

AB \ CD	00	01	11	10
00	1	0	1	1
01	1	0	1	1
11	0	1	1	1
10	0	0	0	0

Shown in Figure 1, both the POS and SOP simplified boolean expressions were modeled in Quartus. As the EGC was lower for the POS expression, it was built instead of the SOP. Either POS or SOP expressions could have been built as they would give the same results.

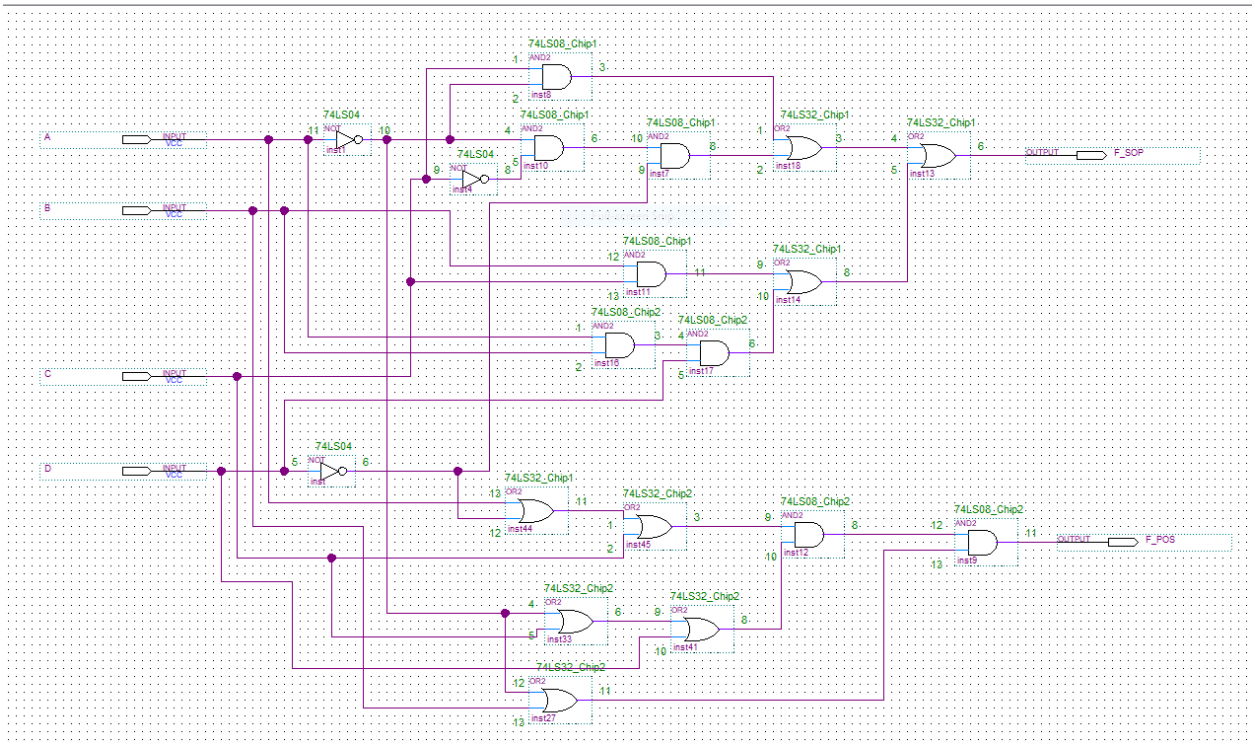

Figure 1: Simplified Boolean expression schematic

Results and Analysis

When built using Quartus, shown as Figure 1, and simulated using Modelsim, shown as Figure 2, the waveforms aligned with the Karnaugh Map shown in Table 1. When the POS simplified boolean expression was built on a circuit board and tested using an LED, the results aligned with both the Karnaugh Map, Table 1, and the Modelsim waveform, Figure 2.

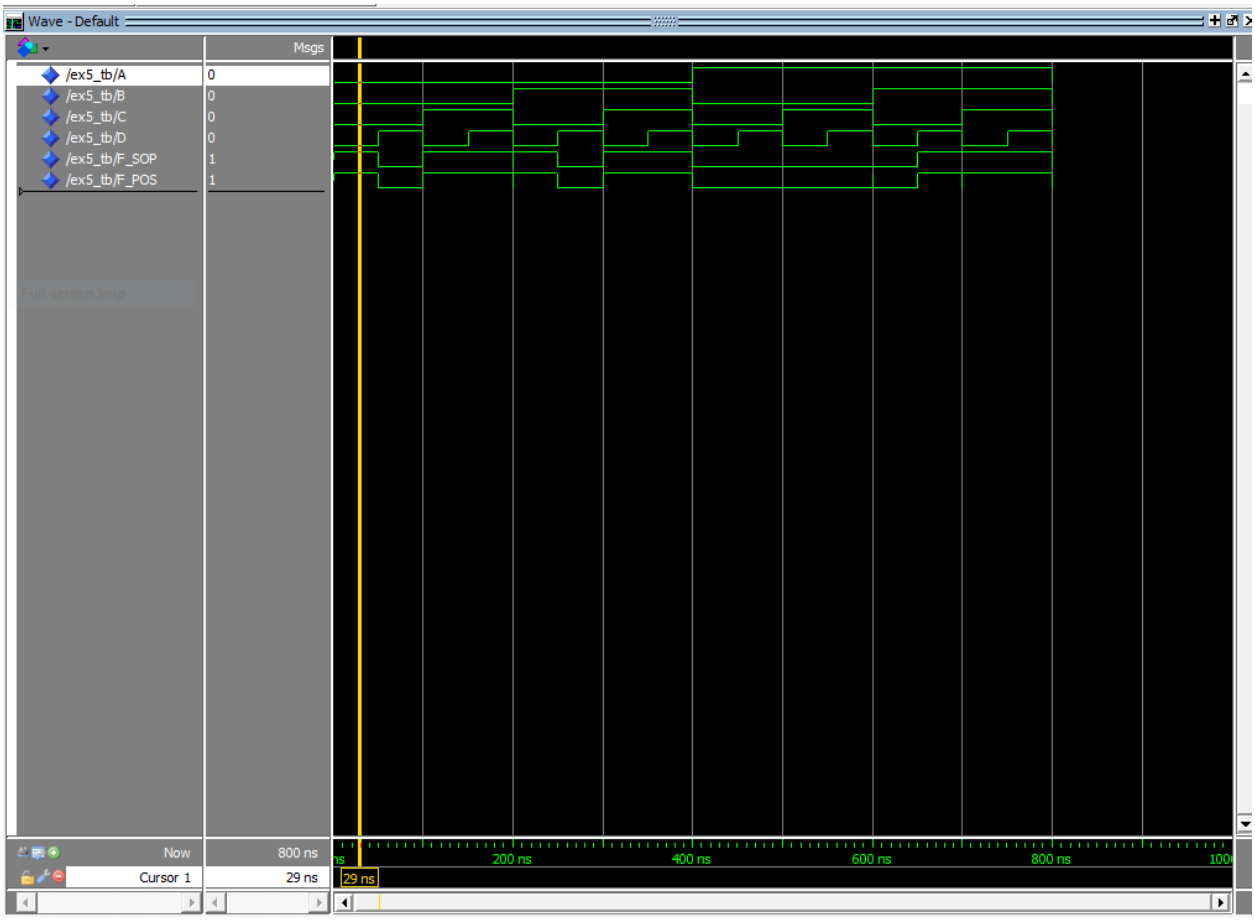

Figure 2: Waveforms of the SOP and POS Boolean expression schematic

Conclusion

Using the Karnaugh Map,Table 1, a Sums of Products and Products of Sums boolean expressions were created. When simplified, they were modeled using Quartus, Figure 1, and simulated using Modelsim, Figure 2. The results found from the Modelsim simulation aligned with the K-Map created. As the EGC of the POS expression was lower than SOP, POS was built. When tested, the POS circuit results aligned with both the Modelsim waveforms found in Figure 2 and the Karnaugh Map shown in Table 1.

Questions

Exercise 5: Combinational Logic Circuit Design Using Karnaugh Map Simplification

Student's Name: Oliver Vinneras Section: L3

Prelab		Point Value	Points Earned	Comments
Part 1	K-maps	4	4	29 JKL
	Correct Boolean expressions	4	4	
Part 2	Schematic diagram	4	4	
	Simulations	4	4	
	EGC	4	4	

Demo		Point Value	Points Earned	Date
Demo	Test Bench	20	20	JKL
	Circuit Construction	20	20	JKL 2/9

To receive any grading credit students must earn points for both the demonstration and the report.

Exercise 5: Combinational Logic Circuit Design Using Karnaugh Map Simplification

Report		Point Value	Points Earned	Comments
Abstract		4		
Design Methodology	Karnaugh maps	5		
	Reduced SOP expression	5		
	Reduced POS expression	5		
	Schematic diagram	4		
Results and Analysis	SOP waveforms	2		
	POS waveforms	2		
Conclusion		5		
Question		5		
Writing Composition		3		
Total for prelab, demo, and report		100		