CMPE-160 DSD1

Laboratory Exercise 8

Analysis and Simulation of Sequential Circuits

By submitting this report, I attest that its contents are wholly my individual writing about this exercise and that they reflect the submitted code. I further acknowledge that permitted collaboration for this exercise consists only of discussions of concepts with course staff and fellow students. Other than code provided by the instructor for this exercise, all code was developed by me.

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Abstract

The purpose of this exercise was to analyze and simulate a 4 bit register to observe how sequential circuits work. This was done by modeling and simulating both a 4 bit shift register and a 4 bit shift register using multiplexers. After analyzing both the functionality and the implementation of both of these 4 bit shift registers, the waveforms aligned with each other and produced the same results as what was found in a function table for a 4 bit shift register.

Design Methodology

A 4 bit shift register was designed and implemented by filling out a table based on a specific sequence of operations. This function table, Table 1, was used to design the 4 bit shift register used. As this 4 bit shift register had a reset active low, whenever the rising edge of the clock was triggered and the reset was at 0, the outputs, QA QB QC and QD were all set to 0.

Table 1: Function table for a reset active low 4 bit shift register

clk	rst	SL	SIN	A	B	C	D	QA	QB	QC	QD
otherwise	1	x	x	x	x	x	x	QA	QB	QC	QD
x	0	x	x	x	x	x	x	0	0	0	0
↑	1	1	x	A	B	C	D	A	B	C	D
↑	1	0	SIN	x	x	x	x	SIN	QA	QB	QC

When the SL, shift load, was 1, the input was loaded as the output. It was only possible to reach this state when reset was 1 and the clock was at a rising edge. If SL was 0, the values of QA, QB, QC, and QD were shifted to the right, with SIN being the new QA.

The Table 1 shown above was used to create a circuit diagram for the 4 bit shift register. This is shown in Figure 1. Using 4 D flip flops, a 4 bit shift register was created. This gives an output of 4 bits, each using the previous output as an input and shifting bits depending on the status of the SL.

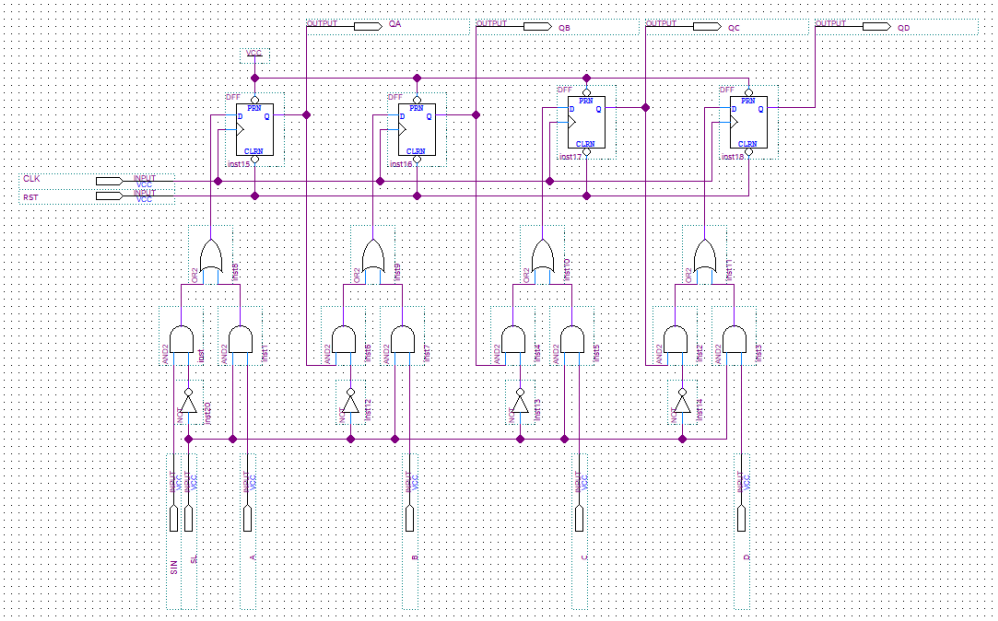

Figure 1: 4 bit shift register

The implementation of the 4 bit shift register, Figure 1, was modeled and tested depending on the values in Table 1. This is also the case for the 4 bit shift register shown in Figure 2. This shift register uses tri-state buffers as multiplexers instead of basic gates.

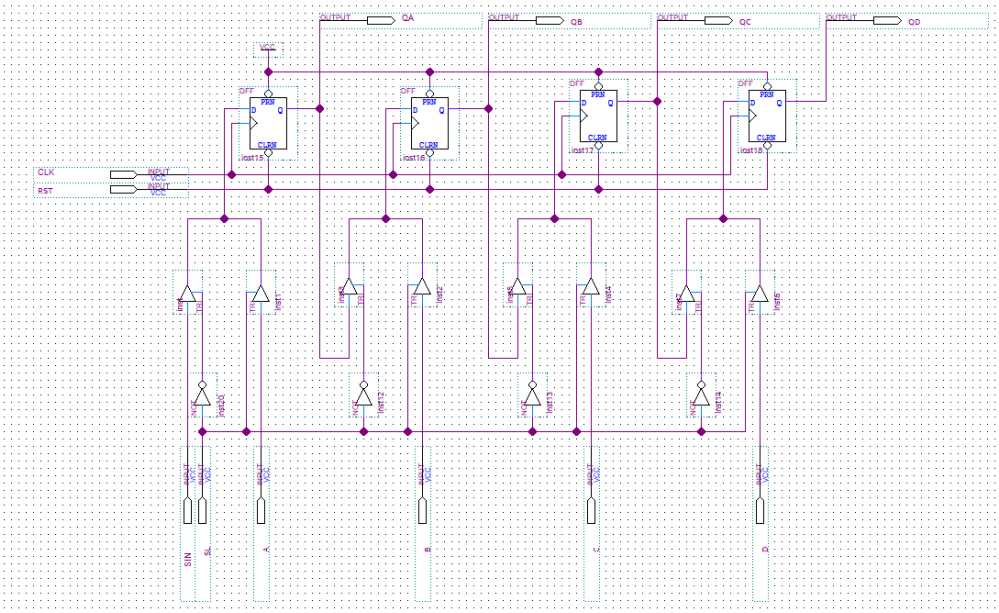

Figure 2: 4 bit shift register using multiplexers

As Figure 1 and Figure 2 had the exact same functionality, they were tested against each other and the results aligned. Using multiplexers instead of basic AOI logic gates can reduce clutter and the amount of gates used.

Results and Analysis

When both Figure 1 and Figure 2 were simulated, the results were shown in Figure 3. This simulation also aligned with Table 1 and the logic behind a 4 bit shift register.

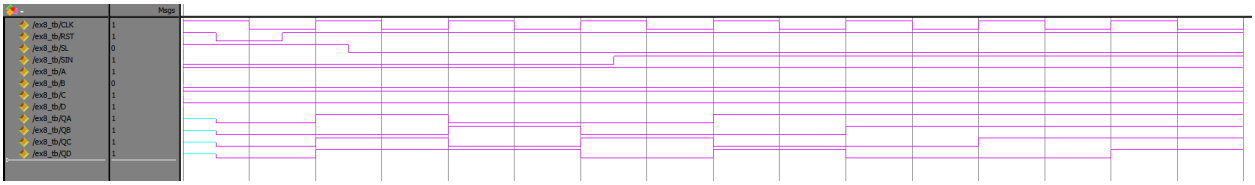

Figure 3: Simulation for the 4 bit shift register

Following the waveforms in Figure 3, they can be used to trace through any part of the implementation of the 4 bit shift register in Figure 1 and Figure 2.

$$Tmin = tco + tpd + ts$$

$$8.767\text{ns} = 6.078\text{ns} + 0\text{ns} + 2.689\text{ns}$$
$$1 / 8.767\text{ns} = 0.114 \text{ x } 10^3 = 114MHz \quad (1)$$

The timing analysis shown in Equation (1) demonstrates the minimum clock period that the circuit can operate at, $Tmin = 8.767ns$, and the maximum clock frequency to be $114MHz$. tco is the Clock to Output time, tpd is the propagation delay in this circuit, assumed to be $0ns$, and ts is the setup time.

Conclusion

This exercise was successful as a table, Table 1, was created as a function table for a 4 bit shift register and when compared to the final simulation of the modeled 4 bit shift register, all values and outputs aligned. This means that the correct relationship was found between the implementation, modeling, and simulation.

Questions

1. The binary value is divided by 2.
2. The binary value is multiplied by 2.
3. As there is a delay between when the signal from the rising edge of the clock reaches the flip flop, the signal from the input might reach the flip flop before the rising edge of the clock does.

Exercise 8: Analysis and Simulation of Sequential Circuits

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Prelab		Point Value	Points Earned	Comments
Prelab	Part 1	5	5	312 HB
	Part 2	5	5	
	Part 3	10	10	HB

Demo		Point Value	Points Earned	Date
Demo	Part 1 Simulation	15	15	03/02/2022 HB
	Part 2 Simulation	15	15	IC 3/2
	Timing Analysis	10	10	IC 3/2

To receive any grading credit students must earn points for both the demonstration and the report.

Exercise 8: Analysis and Simulation of Sequential Circuits

Report		Point Value	Points Earned	Comments
Abstract		3		
Design Methodology	Function table	5		
	Circuit diagram	5		
	Circuit diagram with multiplexors	4		
Results and Analysis	Simulation results	6		
	Timing analysis	3		
Conclusion		4		
Questions	Q1	2		
	Q2	2		
	Q3	2		
Writing Composition		4		
Total for prelab, demo, and report		100		