CMPE-160 DSD1

Laboratory Exercise 03

Electrical and Logical Characteristics of Gates

By submitting this report, I attest that its contents are wholly my individual writing about this exercise and that they reflect the submitted code. I further acknowledge that permitted collaboration for this exercise consists only of discussions of concepts with course staff and fellow students. Other than code provided by the instructor for this exercise, all code was developed by me.

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2 February 2022

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Abstract

The purpose of this laboratory exercise was to test the electrical and logical characteristics of logic gates. This was done by testing the voltage input and voltage output of a two input NAND gate, a two input OR gate, and a two input XOR gate. When 5 volts and 0.1 amps was being supplied to the circuit, the voltage was measured using a multimeter. These readings varied depending on which chip was being tested and the switch position of each input. After this, the effect of propagation delay was tested to find how the number of gates of delay affects the delay and period of a ring oscillator.

Design Methodology

The voltage of the internal connections of a logic gate can be found using a multimeter. This is shown with Figure 1.1, a 2 input AND gate. S1 and S2 are the inputs measured, and the output is L1. When a switch is put between the inputs and the AND gate, the output will change depending on what kind of gate the voltage is sent through. To measure the delay of voltage through a gate, an oscillator is used. With a given reference point, like at pin 2 in Figure 1.2, and another point used for measuring the delay found between the inverter gate, like at pin 5, the voltage delay can be found for that NOT gate.

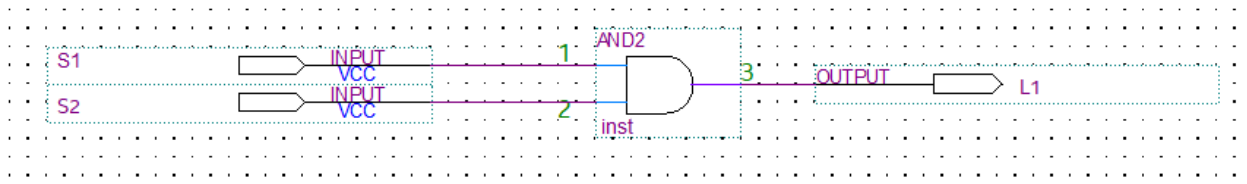


Figure 1.1: Voltage measurement circuit schematic

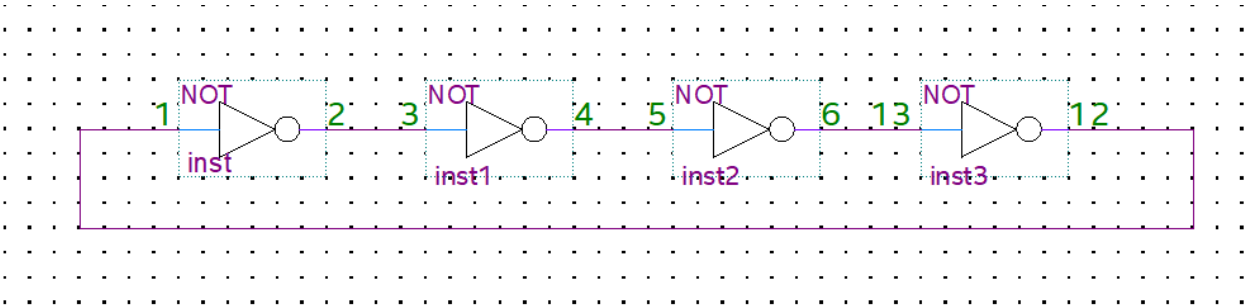


Figure 1.2: Ring oscillator circuit schematic

Results and Analysis

In this experiment, a multimeter was used to measure the voltage of logical gates. When power was given to a NAND gate, shown in Table 2.1, the voltage input and output depended on both switch positions. When both switches were closed, the LED was on. When one of the gates was open, the LED was on, and when both switches were open, the LED was off. These results align with the logic for a NAND logic gate.

Table 2.1: Measurements of a two input NAND gate circuit

Switch 1 Position	Switch 2 Position	Vin 1 (V)	Vin 2 (V)	Vout (V)	LED (on/off)
Closed	Closed	0	0	4.15	on
Closed	Open	0	5	4.15	on
Open	Closed	5	0	4.15	on
Open	Open	5	5	0	off
Logical function of gate:				NAND	
Lab kit part number for gate:				74LS00N	

When the NAND gate was switched with an OR gate, the LED behaved differently, shown in Table 2.2. When both switches were closed, the Voltage of both inputs and the output was 0, meaning the LED was off. When one switch was opened, that switch had an input of 5 volt and the LED was on. When both switches were open, their inputs were both 5 volts with an output of 4.06 volts and the LED on.

Table 2.2: Measurements of a two input OR gate circuit

Switch 1 Position	Switch 2 Position	Vin 1 (V)	Vin 2 (V)	Vout (V)	LED (on/off)
Closed	Closed	0	0	0	off
Closed	Open	0	5	4.06	on
Open	Closed	5	0	4.06	on
Open	Open	5	5	4.06	on
Logical function of gate:				OR	
Lab kit part number for gate:				74LS32	

The XOR gate behaved similar to the OR gate, but as it is exclusively OR, only when one of the switches is open and the other switch is closed will the LED be on. This is shown in Table 2.3. When both of the inputs are 0 volts, the LED is off and when both of the inputs are 5 volts the LED is off.

Table 2.3: Measurements of a two input XOR gate circuit

Switch 1 Position	Switch 2 Position	Vin 1 (V)	Vin 2 (V)	Vout (V)	LED (on/off)
Closed	Closed	0	0	0	off
Closed	Open	0	5	4.09	on
Open	Closed	5	0	4.09	on
Open	Open	5	5	0	off
Logical function of gate:				XOR	
Lab kit part number for gate:				74LS86	

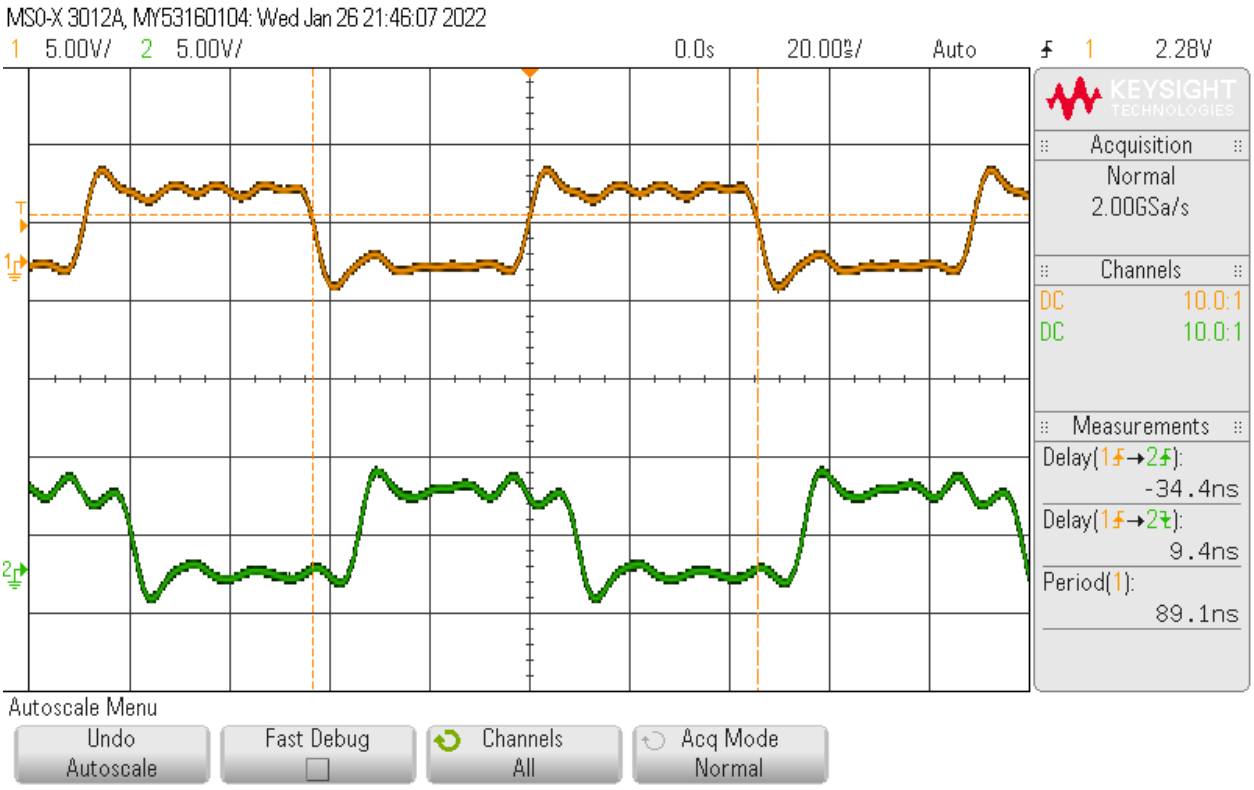


Figure 2.1: Wave readings of propagation delay

The propagation delay was studied using an oscilloscope. It measured the delay between channel 1, which was the reference point, and channel 2, which was connected to the output of an inverter gate. This was repeated to get measurements of propagation delay between 4 gates by chaining the inverters and placing channel 2 in an inverter output. These measurements were recorded in Table 2.4.

Table 2.4: Measurements of propagation delay

74LS04 (pin to pin)	Number of Gates of Delay	Propagation Delay (ns)
2 to 4 (rising to falling)	1	9 ns
2 to 6 (rising to rising)	2	20 ns
2 to 12 (rising to falling)	3	28 ns
2 to 4 (rising to rising)	4	37 ns
Period:		89 ns

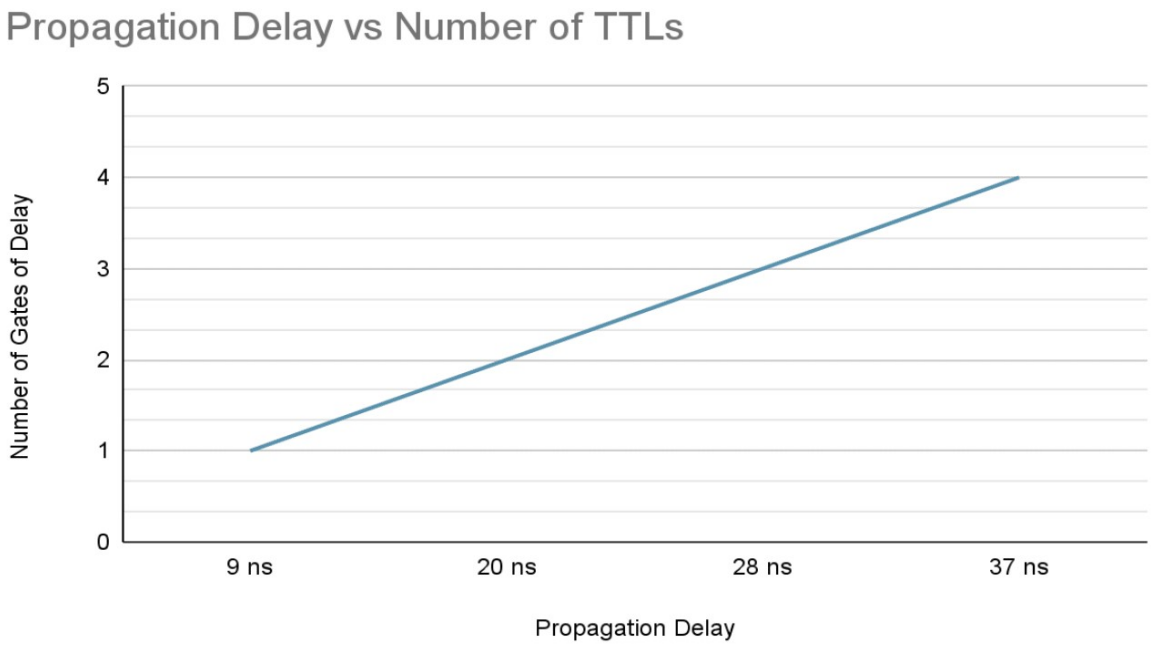


Figure 2.2: Measurements of propagation delay

The measurements of propagation delay were plotted against the number of gates and a linear relationship was found. This means that as the number of gates of delay increases, the propagation delay will also increase.

Conclusion

This exercise indicated that as voltages have gone through a switch are given to specific chips, they will act depending on the input voltages. If both switches are closed in a NAND gate, both the input voltages will be zero, the output voltage will be 5 and the LED will be on. When measuring the propagation delay in an oscilloscope, which tests and displays voltage signals as wave forms, the delay is shown. This delay is equal to how long time it takes for the voltage to pass through the given amount of gates. Each gate gives a certain amount of propagation delay, which is added together with each additional gate.

Questions

1. What are the voltage values for the 74LS27?

   (a) Minimum input voltage for logic "1"

   The minimum voltage is 2 volts.

   (b) Maximum input voltage for logic "0"

   The maximum voltage is 0.8 volts.

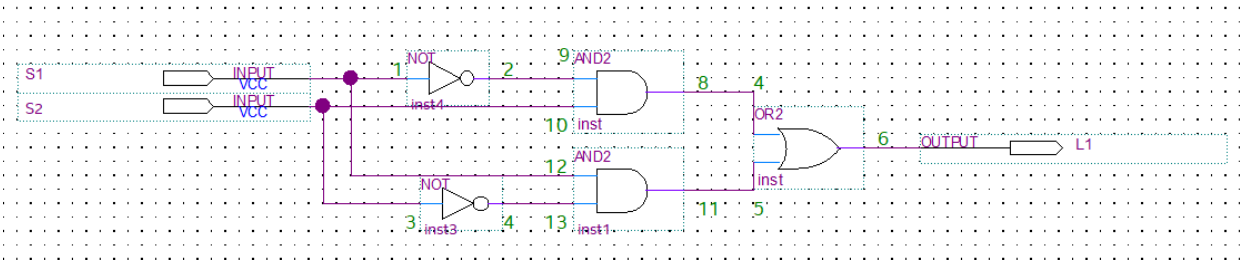
   (c) Minimum output voltage for logic "1"

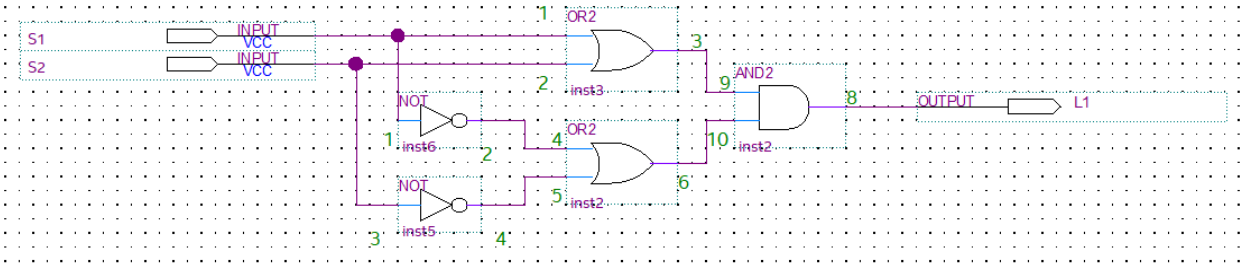
   The minimum voltage is 2.7 volts.

2. Define propagation delay, and discuss how it impacts the output from a gate. Why is it a consideration in digital designs?

   Propagation delay is the delay present in the components (gates) of a chip. Propagation delay is considered in digital designs as there is a different amount of delay based on which logic gates are used and how the configuration they are in is set up.

3. Design two different circuits that implement a 2-input XOR function using a single 74LS08 (quadruple 2-input AND gate package), a single 74LS32 (quadruple 2-input OR gate package), and a single 74LS04 (6-inverter package). Draw the circuit diagrams with the pin numbers properly labeled.


S1
S2
INPUT
VCC
INPUT
VCC
NOT
inst4
NOT
inst3
AND2
inst
AND2
inst1
OR2
inst
OUTPUT
L1


S1
S2
INPUT
VCC
INPUT
VCC
OR2
inst3
NOT
inst6
OR2
inst2
NOT
inst5
AND2
inst2
OUTPUT
L1