Class: SE **Subject: COA LAB** **Sem-III**

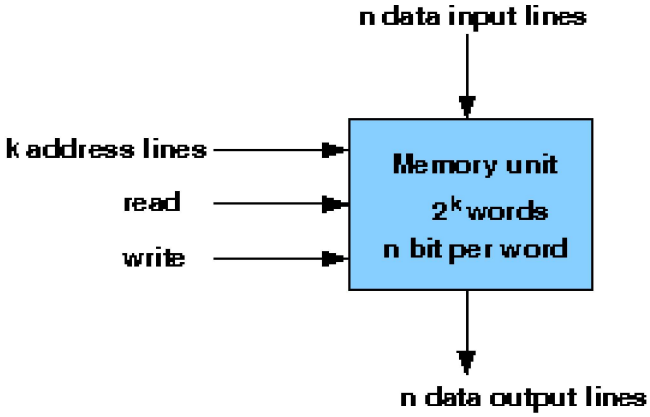
Experiment No 10

Course Outcome: CO6 **Blooms Level:L4**

Aim: Analyze the organization of memory cells in a 4×3 memory array.

Abstract: Design and analyze the structure of a 4×3 memory array to understand the organization and addressing of individual memory cells. The experiment should demonstrate how data is stored, accessed, and controlled within the array using row and column select lines, along with read/write control signals.

Theory:A memory unit is a collection of storage cells together with associated circuits needed to transform information in and out of the device. Memory cells which can be accessed for information transfer to or from any desired random location are called random access memory(RAM). The block diagram of a memory unit-



Internal Construction: The internal construction of a random-access memory of m words with n bits per word consists of m*n binary storage cells and associated decoding circuits for selecting individual words. The binary cell is the basic building block of a memory unit.

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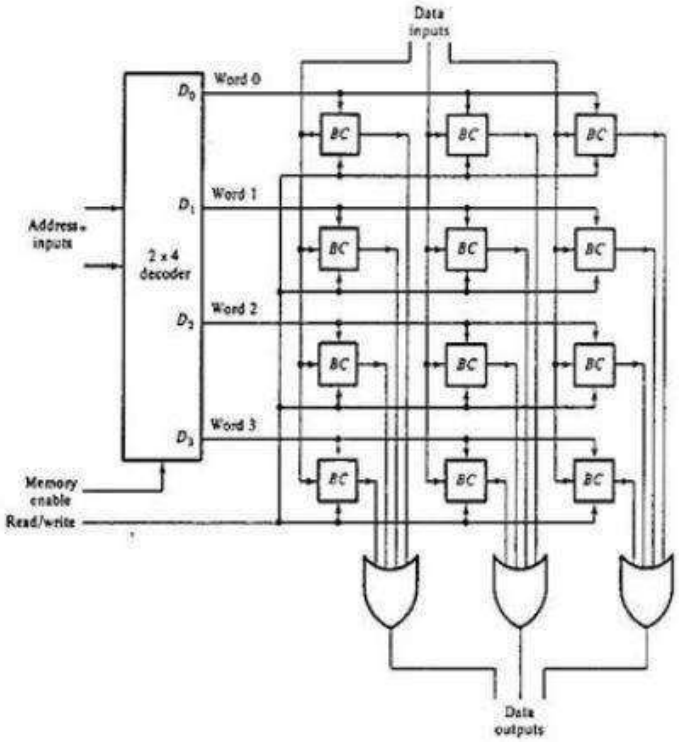
Procedure:

1. Start the simulator as directed. This simulator supports 5-valued logic.
2. To design the circuit we need 12 binary RAM cell, 9 OR gate, 7 bit switch (to give input, which will toggle its value with a double click), 3 bit display (to see the output), wires.
3. The pin configuration of a component is shown whenever the mouse is hovered on any canned component of the palette or press the 'show pinconfig' button. Pin numbering starts from 1 and from the bottom left corner (indicated with the circle) and increases anticlockwise.
4. For a binary RAM cell input is in pin-5, output is in pin-4 and select is pin-8, Read/Write is in pin-6, for read operation give 1 input to Read/Write pin. For write operation give 0 input to Read/Write pin.
5. For a 'decoder with enable', input A is in pin-6, B is in pin-5, output D0 is in pin-4, D1 is in pin-3, D2 is in pin-2, D3 is in pin-1 and Enable is in pin-8
6. Click on the 'decoder with enable' component (in the Other Components drawer in the pallet) and then click on the position of the editor window where you want to add the component (no drag and drop, simple click will serve the purpose), likewise add 12 binary RAM cell (from the Other Components drawer in the pallet), 9 OR gates (from Logic Gates drawer in the pallete), 7 bit switches (which will toggle its value with a double click), 3 bit displays (from Display and Input drawer of the pallet, if it is not seen scroll down in the drawer)
7. To connect any two components select the Connection menu of Palette, and then click on the Source terminal and click on the target terminal. According to the circuit diagram connect all the components, connect 2 bit switches to the inputs of the 'decoder with enable' (which will act as address input), 1 bit switch to the enable pin
   of the 'decoder with enable' (which will act as memory enable input), connect a bit switch to the Read/Write(R/W') line, 3 bit switches to the data inputs line, 3 bit displays to the data

output line and OR gates according to the diagram shown in the circuit diagram. After the connection is over click the selection tool in the pallete.

8. To see the circuit working, Do some read or write operation by properly setting the R/W', memory enable then give input and check the output. suppose you give, R/W'=1, memory enable=1, address input=01, data input=101, then it will be a read operation and you will not see 101 as output, it will store 101 in the word-1. now again set, R/W'=0, memory enable=1, address input=01, then it will be a write operation and you will see 101 as the content of word-1 on the output display.



Output:

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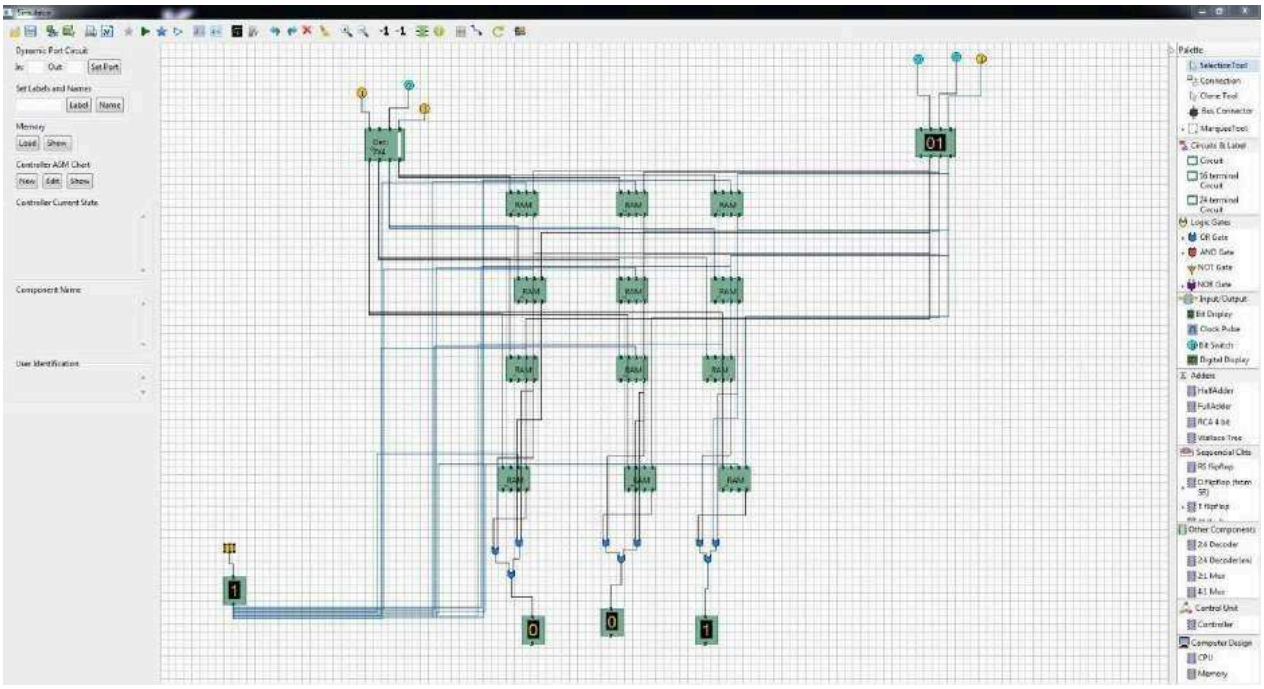

Conclusion: In this experiment, the organization of memory cells in a 4×4 memory array was analyzed to understand the structural layout and addressing mechanism of small-scale memory. The observation of how individual memory cells are accessed using row and column decoders provided insight into the internal architecture of memory arrays. This experiment reinforces the concept of memory addressing, read/write control, and data storage at the hardware level, forming a foundational understanding of how larger memory systems are constructed and managed in computer organization.

Exercise 1:

Aim: To design a 4×4 RAM memory that consists of 4 words, each word containing 4 bits, using binary RAM cells, a 2-to-4 decoder with enable, and OR gates, and to test it by giving appropriate inputs.

Abstract: The logical construction of a small RAM 4×4 is shown below. It consists of 4 words of 4 bits each and has a total of 16 binary cells. Each block labeled BC represents a binary cell with its 3 inputs and 1 output. The block diagram of a binary cell remains the same.

A memory with 4 words needs two address lines. The two address inputs go through a 2×4 decoder

to select one of the four words. The decoder is enabled with the memory enable input.

- When the memory enable is 0, all outputs of the decoder are 0 and none of the memory words are selected.
- With the memory enable at 1, one of the four words is selected, dictated by the value in the two address lines.

Once a word has been selected, the read/write input determines the operation:

- If read/write = 0, the selected word's contents are read and appear on the data output lines.
- If read/write = 1, the data input lines are written into the selected word.

The logic diagram is updated to reflect 4 bits per word, so there are 4 vertical bit lines and 4 binary cells per row, giving a total of 16 binary cells (BC1 to BC16).

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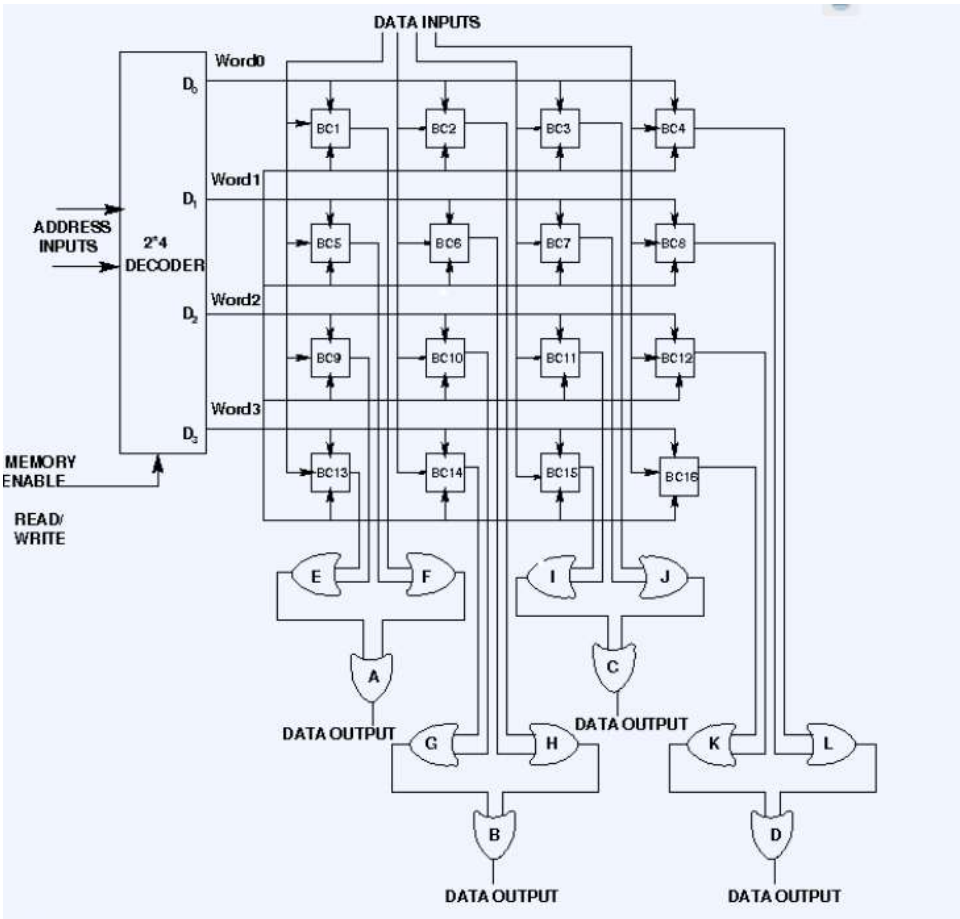

1. Do some read operation by properly setting the R/W', memory enable then give input and check the output.
2. Do some write operation by properly setting the R/W', memory enable then give input and check the output.
3. Do some read operation without setting the memory enable but properly setting the R/W' then give input and check the output.

Use Display units for checking output. Try to use a minimum number of components to build. The pin configuration of the canned components are shown when the mouse hovered over a component.