10.3" 8K
Product Specification
Rev. P0

Customer Name	:	
Product Name	:	TOP103MONO8K01A
Model Name	:	TOP103MONO8K01A
Description	:	10.3" HD (7680×4320) 8K

Proposed by			Customer's Approval
Designed	Checked	Approved	

ZHEN HUAI ZHI TECHNOLOGY CO.,LTD

Revision History

Rev.	ECN No.	Description of Change	Date	Prepared
P0	-	-.Initial issue	2021.11.30	Huangxiaoqin
P1		update timing	2021.12.31	Huangxiaoqin

Content

No.	Items	Page
1	General Description	4
2	Mechanical Specification	6
3	Absolute Maximum Ratings	6
4	Electrical Characteristics	6
5	Electro-optical Characteristics	7
6	FPC Pin Assignment	8
7	AC Characteristics	10
8	Recommended Operating Sequence	16
9	Outline Information	18
10	Reliability	19
11	Handling Precautions	20
12	Packing Specification	22

1. General Description

1-1. Introduction

WISECOCO 10.3” 8K is is a black-and-white active matrix TFT LCD module using Low Tem perature Poly-silicon TFT‘ s (Thin Film Transistors) as an active switching devices. This module has a 10.3 inch diagonally measured active area with 8K resolutions (4320 horizontal by 7680 vertical pixel array)..

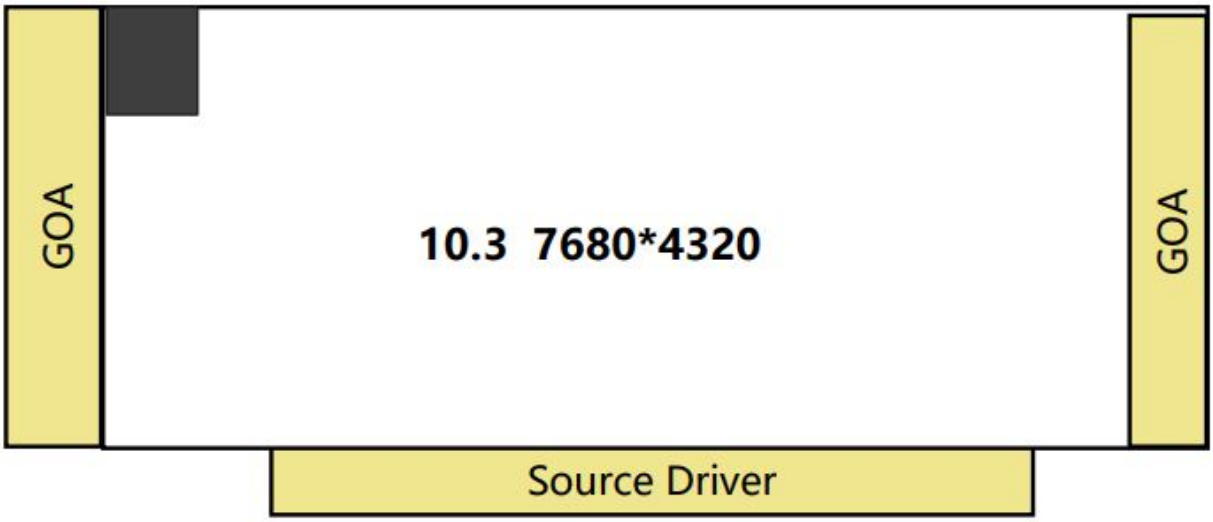


Figure 1

1-2. Driver IC Block Diagram

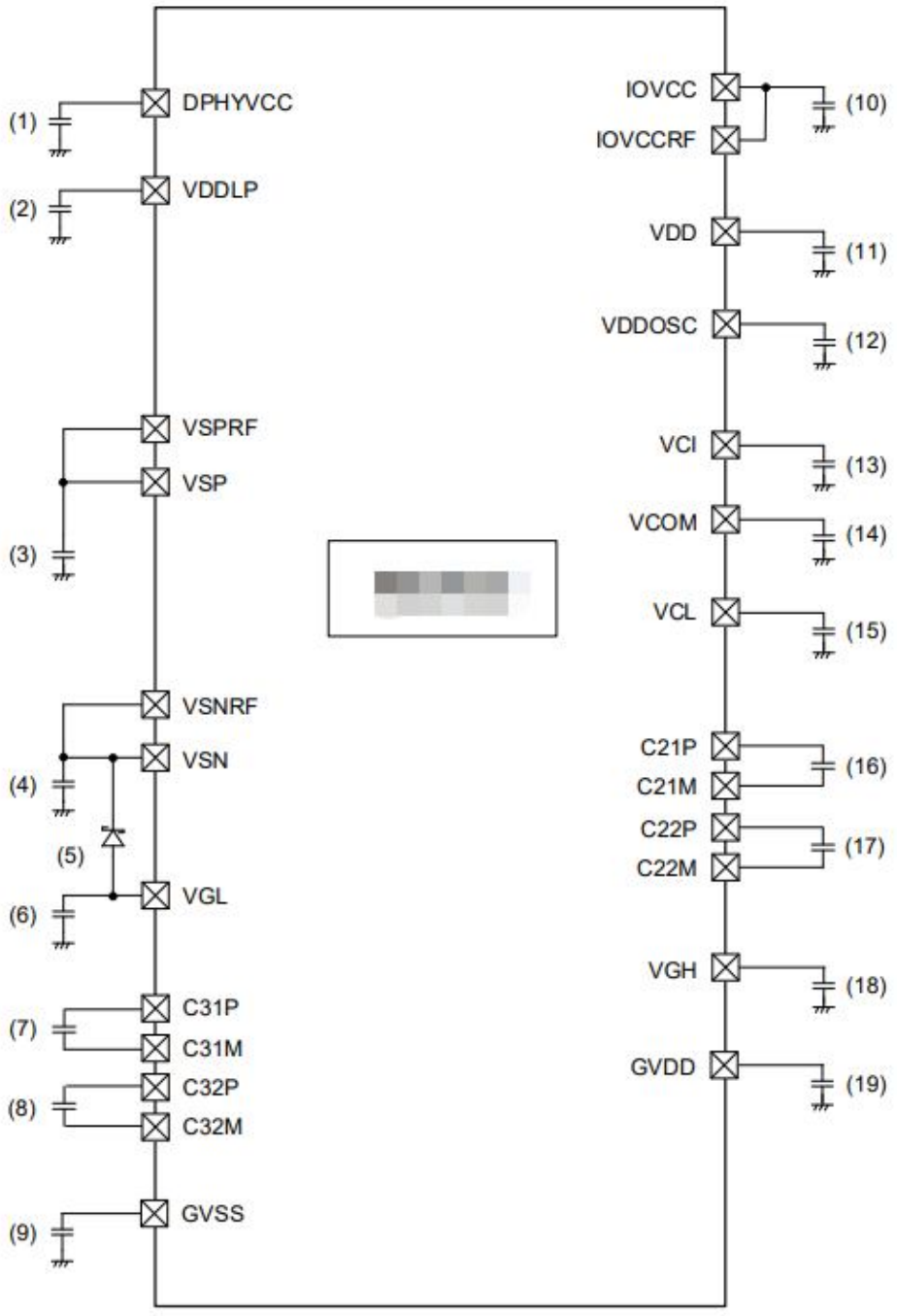


Figure 2

1-3. Features

1) Display Format : 10.3” 8K : 7680*4320
2) Interface : MIPI-DSI 8 lanes
3) Driver IC :
4) Polarizer : POL

2. Mechanical Specification

Table 1

Item	Specifications	Unit	Remark
Panel outline	232.096(W) × 138.402(H)×1.24(T)	mm	
Number of dots	7680*4320	Dots	8K
Active area	228.096(W) × 128.304(H)	mm	
Diagonal Inch	10.3	inch	
Pixel pitch	29.7(W) × 29.7(H)	um	
Pixel Arrangement	MONO		

3. Absolute Maximum Ratings

Table 2

Item	Symbol	Min.	Max.	Unit	Note
I/O Voltage	VDDIO	1.65	1.95	V	
EL Driving Voltage	ELVDD	4.50	6.30	V	
	ELVSS	-4.5	-6.3	V	
Operating temperature	Topr	-20	70	℃	
Storage temperature	Tstg	-40	80	℃	

4. Electrical Characteristics

Test Condition: Temp=25±2℃

Table 3

Item		Symbol		Condition	Min.	Typ.	Max.	Unit	Remark
ELVDD		ELVDD		-	4.5	5.5	6.30	V	
ELVSS		ELVSS		-	-4.5	-5.5	-6.30	V	Controlled by DDIC
VDDIO		VDDIO		-	1.62	1.80	1.98	V	
Current Consumption (Display)	Display on mode	IC	VCI	White pattern	-	-	-	mA	Full White
			VDDIO		-	-	-	mA	
			AVDD		-	-	-	mA	
		Panel	ELVDD		-	-	-	mA	Full White
			ELVSS		-	-	-	mA	
Frame Frequency		F_{rm}		-	-	30	-	Hz	

Notes :

1. The value is just the reference value. The customer may optimize the setting value.
2. The current of Vin is just the reference value, because it depends on the efficiency of Power IC.
3. IC Power Consumption $P_{IC}=V_{VDDIO}*I_{VDDIO}+V_{VCI}*I_{VCI}+V_{AVDD}*I_{AVDD}$
   EL Power Consumption $P_{EL}=V_{ELVDD}*I_{ELVDD}+V_{ELVSS}*I_{ELVSS}$
   Total Power Consumption $P_{total}=P_{EL}+P_{IC}$

5. Electro-optical Characteristics

The test of optical specifications shall be measured in a dark room (ambient luminance ≤1lux and temperature = 25±2°C) with the equipment of Luminance meter. We refer to θ, Ø=0º (=θ_3) as the 3 o'clock direction (the "right"), θ, Ø=90º (= θ_{12}) as the 12 o'clock direction ("upward"), θ, Ø=180º (= θ_9) as the 9 o'clock direction ("left") and θ, Ø=270º (= θ_6) as the 6 o'clock direction ("bottom"). While scanning θ and/or Ø, the center of the measuring spot on the Display surface shall stay.

Table 4

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Luminance Contrast ratio		CR	θ=0°	300:1		-	-	405nm 光 源，60℃Note2
Viewing Angle range			CR > 10	70	80	/	Deg.	Note1
				70	80	/		
				70	80	0.71		
				70	80	0.35		
transmittance			Θ = 0°	-	4	-	%	不带 APF&Haze @405nm
Cross talk			-	-	-	1.5	%	
Gamma			-	2.0	2.2	2.4	-	

Notes :1

1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the panel surface (see Figure 3).

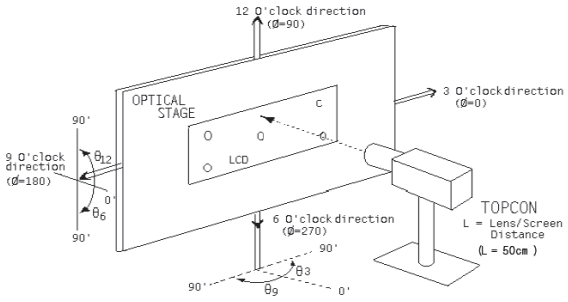


Figure 3

2. Contrast measurements shall be made at viewing angle of θ= 0º and at the center of the panel surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state. (see Figure 3) Luminance Contrast Ratio (CR) is defined mathematically.

$$\mathrm{CR} = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. The color chromaticity coordinates specified in Table 4 shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.

4. Crosstalk measurement shall be done at the center of the different pattern and the result shall be calculated as follow formula.

a. measure luminance at the center.

b. calculate cross talk as below equation:

$$\text{Crosstalk(V)} = \max\left(\left|\frac{L_{V1}-L_{V2}}{L_{V2}}\right| \times 100, \left|\frac{L_{V3}-L_{V4}}{L_{V4}}\right| \times 100\right)$$

$$\text{Crosstalk(H)} = \max\left(\left|\frac{L_{H1}-L_{H2}}{L_{H2}}\right| \times 100, \left|\frac{L_{H3}-L_{H4}}{L_{H4}}\right| \times 100\right)$$

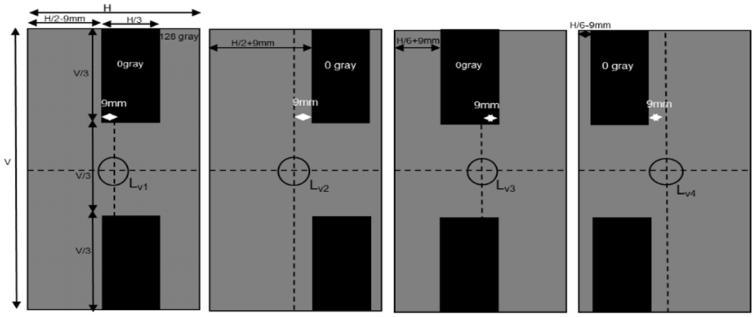


Figure 5. Vertical crosstalk measuring pattern

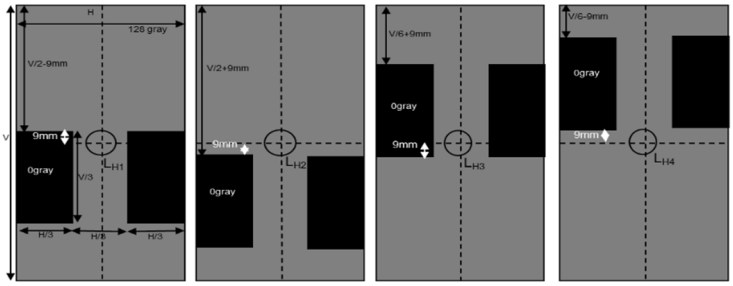


Figure 6. Horizontal crosstalk measuring pattern

6. FPC Pin Assignment

Main FPC assignment- Input/output Signal Interface.

Recommended connector: XF2M-5015-1A.

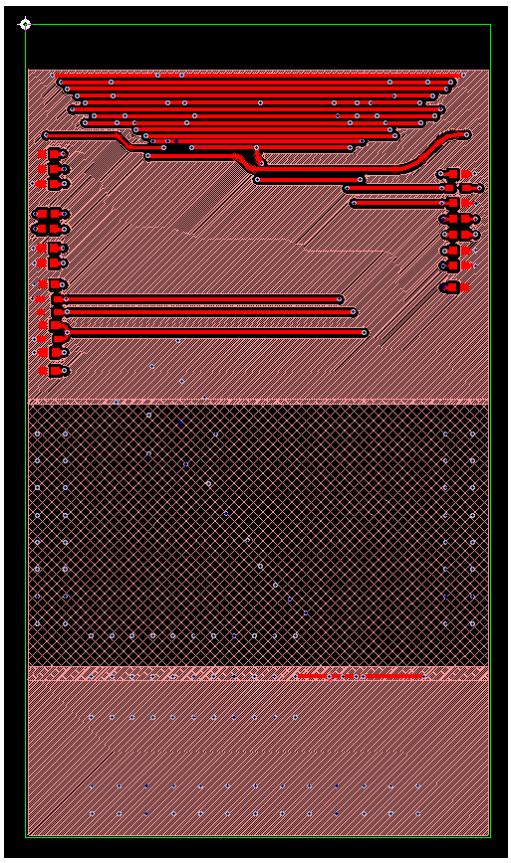
Table 5

No.	Name	Remark
1	GND	Ground
2	NC	No connection
3	NC	No connection
4	NC	No connection
5	NC	No connection
6	VSP	Positive input analog power(+5.5V)
7	NC	No connection
8	VSN	Negative input analog power(-5.5V)
9	NC	No connection
10	GND	Ground
11	GND	Ground
12	IOVCC	IO Power supply(1v8)
13	GND	Ground

14	NC	No connection
15	GND	Ground
16	NC	No connection
17	RESET	Reset signal input terminal(1v8)
18	TE	Tearing effect signal to frame memory writing
19	GND	Ground
20	GND	Ground
21	D0P_M	MASTER MIPI data Lane 0 positive-end input
22	D0N_M	MASTER MIPI data Lane 0 negative-end input
23	GND	Ground
24	D1P_M	MASTER MIPI data Lane 1 positive-end input
25	D1N_M	MASTER MIPI data Lane 1 negative-end input
26	GND	Ground
27	CLKP_M	MASTER MIPI Clock Lane positive-end input/output
28	CLKN_M	MASTER MIPI Clock Lane negative-end input/output
29	GND	Ground
30	D2P_M	MASTER MIPI data Lane 2 positive-end input
31	D2N_M	MASTER MIPI data Lane 2 negative-end input
32	GND	Ground
33	D3P_M	MASTER MIPI data Lane 3 positive-end input
34	D3N_M	MASTER MIPI data Lane 3 negative-end input
35	GND	Ground
36	D0P_S	Slave MIPI data Lane 0 positive-end input
37	D0N_S	Slave MIPI data Lane 0 negative-end input
38	GND	Ground
39	D1P_S	Slave MIPI data Lane 1 positive-end input
40	D1N_S	Slave MIPI data Lane 1 negative-end input
41	GND	Ground
42	CLKP_S	Slave MIPI Clock Lane positive-end input/output
43	CLKN_S	Slave MIPI Clock Lane negative-end input/output
44	GND	Ground
45	D2P_S	Slave MIPI data Lane 2 positive-end input
46	D2N_S	Slave MIPI data Lane 2 negative-end input
47	GND	Ground
48	D3P_S	Slave MIPI data Lane 3 positive-end input
49	D3N_S	Slave MIPI data Lane 3 negative-end input
50	GND	Ground

<Pin layout of FPC contact pads>

Front



Back

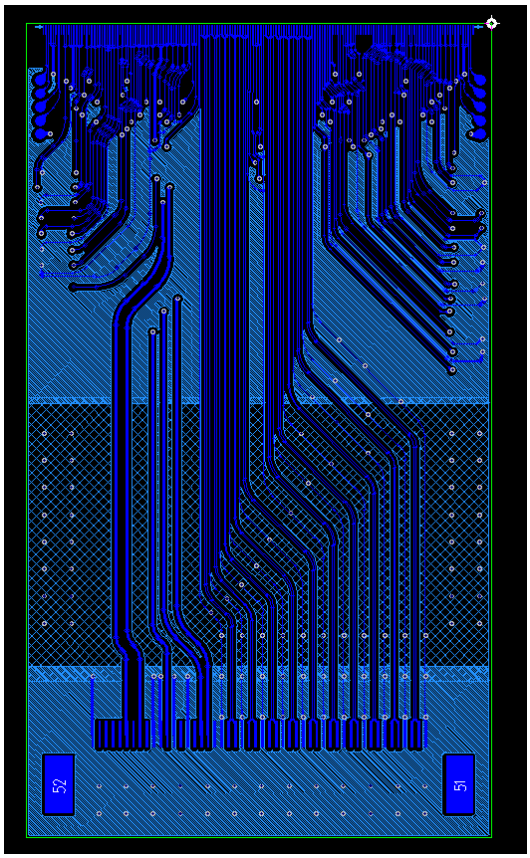


Figure 7

7. AC Characteristics（For reference only)）

7-1. MIPI DSI Characteristics

7-1-1. DC Characteristics for MIPI DSI

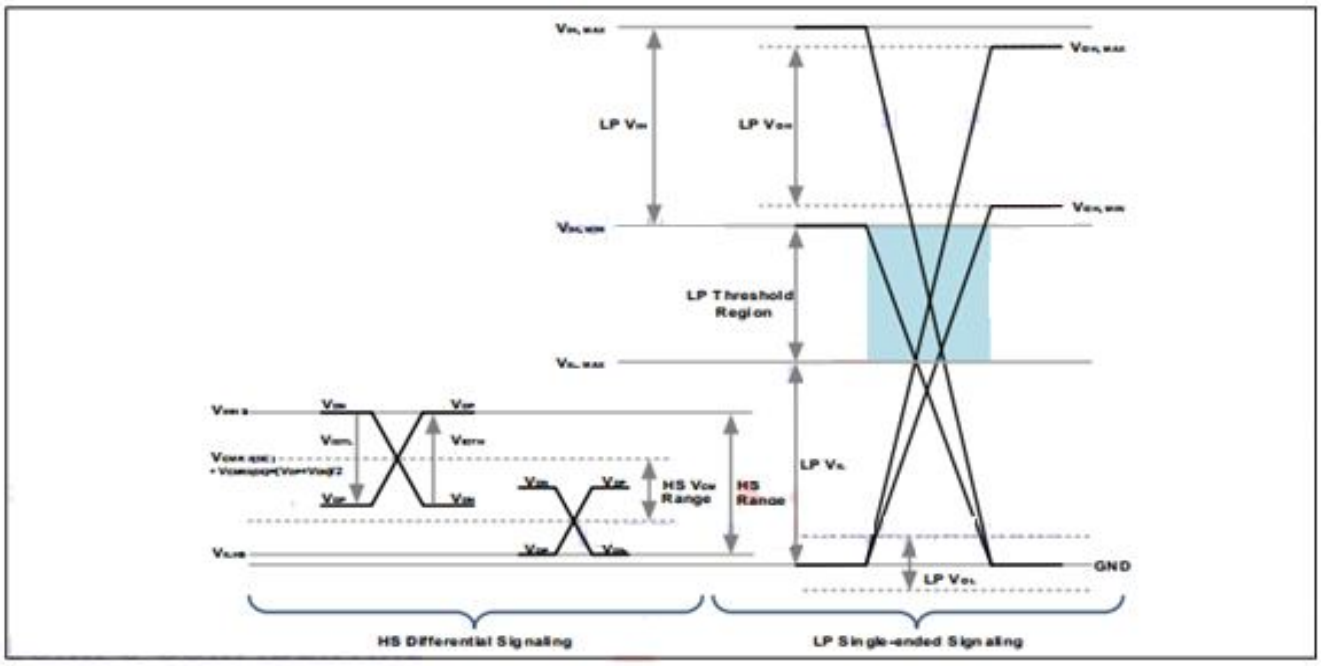


Figure 8 MIPI DSI Signaling Levels

Table 6

Signal	Symbol	Parameter	Min.	Typ.	Max.	Unit
HS_RX	V_{IDTH}	Differential input high threshold	-	-	70	mV
	V_{IDTL}	Differential input low threshold	-70	-	-	
	V_{IHHS}	Single-ended input high voltage	-	-	460	
	V_{ILHS}	Single-ended input low voltage	-40	-	-	
	$V_{TERM-EN}$	Single-ended threshold for HS termination enable	-	-	450	
	$V_{CMRX(DC)}$	Common-mode voltage HS receive mode	70	-	330	
	Z_{ID}	Differential input impedance	-	100	-	Ω
LP_RX	V_{IL}	Logic0 voltage not in ULP State	-	-	550	
	V_{IH}	Logic1 input voltage	880	-	-	mV
	V_{LEAK}	I/O leakage current	-10	-	10	uA
LP_TX	V_{OL}	The venin output low level	-50	-	50	mV
	V_{OH}	The venin output high level	1.1	1.2	1.3	V
	Z_{OLP}	Output impedance of LP transmitter	110	-	-	Ω

7-1-2. MIPI DSI High-Speed RX Clock and Data-Clock Timing

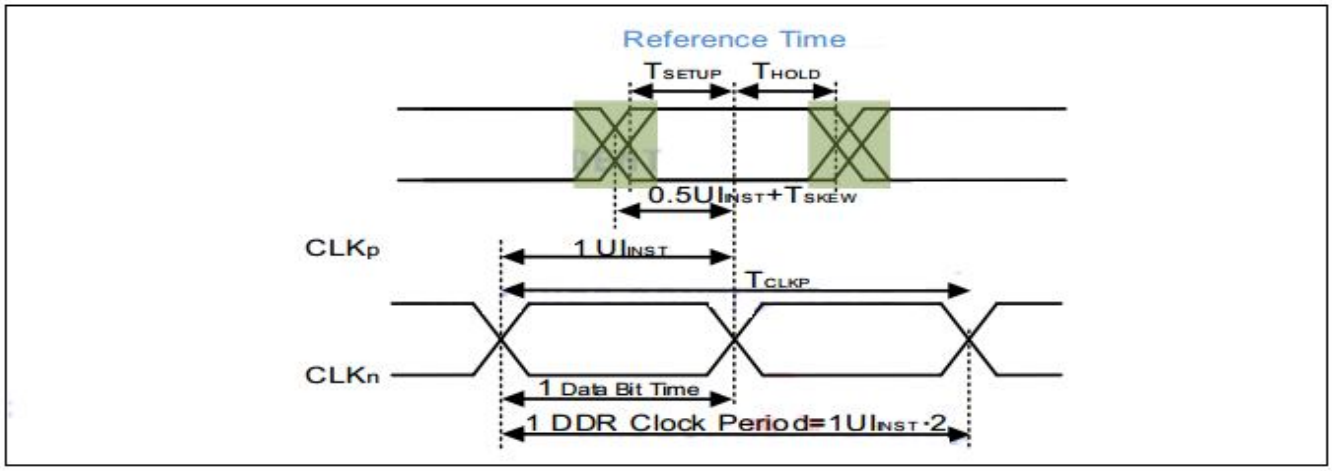


Figure 9 MIPI Data to Clock Timing Definitions

Table 7-1(Actual Value)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{DSICLK}	DISCLK Frequency	VDDI=1.65~1.95V	T.B.D.		750	MHz
T_{CLKP}	DSICLK Cycle time		1		4	Ns
T_{DSIR}	DSI Data Transfer Rate		T.B.D.		1100	Mbps
$T_{SKEW[TX]}$	Data to Clock Skew		-0.15		0.15	UI_{INST}
T_{SETUP}	Data to Clock Setup time		0.15	-	-	UI_{INST}
			0.15	-	-	ns
T_{HOLD}	Data to Clock Hold time		0.15	-	-	UI_{INST}
			0.15	-	-	ns
UI_{INST}	UI instantaneous		1		12.5	ns

Table 7-2(Design Value)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{DSICLK}	DISCLK Frequency	VDDI=1.65~3.3V	T.B.D.		750	MHz
T_{CLKP}	DSICLK Cycle time		1		4	Ns
T_{DSIR}	DSI Data Transfer Rate		T.B.D.		1000	Mbps
$T_{SKEW[TX]}$	Data to Clock Skew		-0.15		0.15	UI_{INST}
T_{SETUP}	Data to Clock Setup time		0.15	-	-	UI_{INST}
			0.15	-	-	ns
T_{HOLD}	Data to Clock Hold time		0.15	-	-	UI_{INST}
			0.15	-	-	ns
UI_{INST}	UI instantaneous		1		12.5	ns

7-1-3. Global Operation Timings

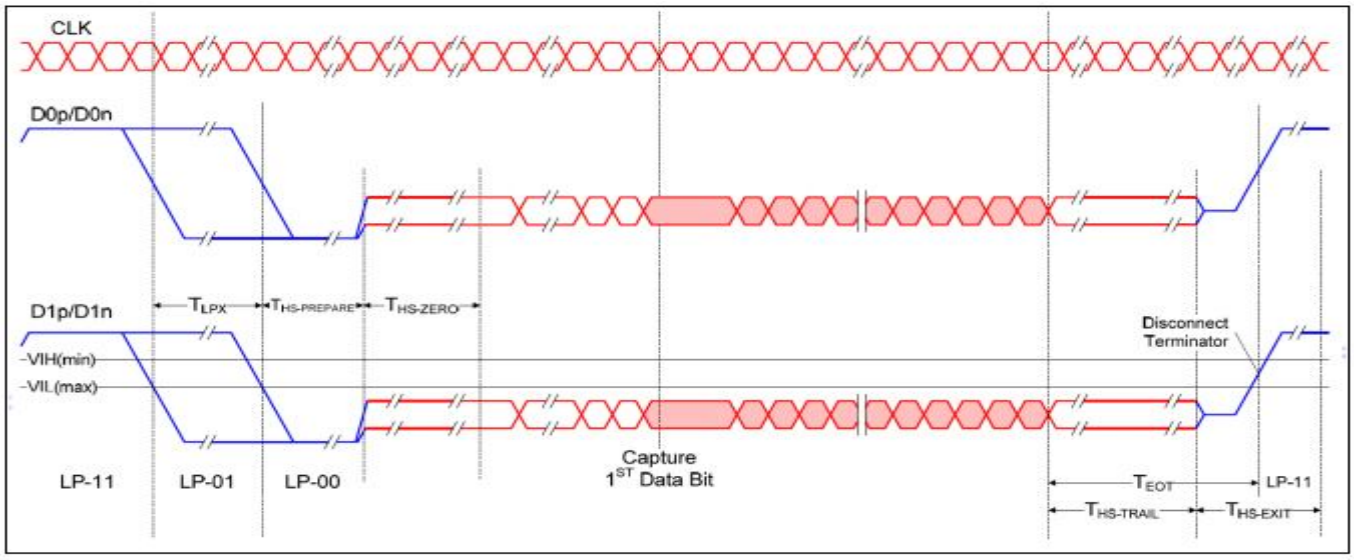


Figure 10 MIPI HS Data Transmission in Bursts

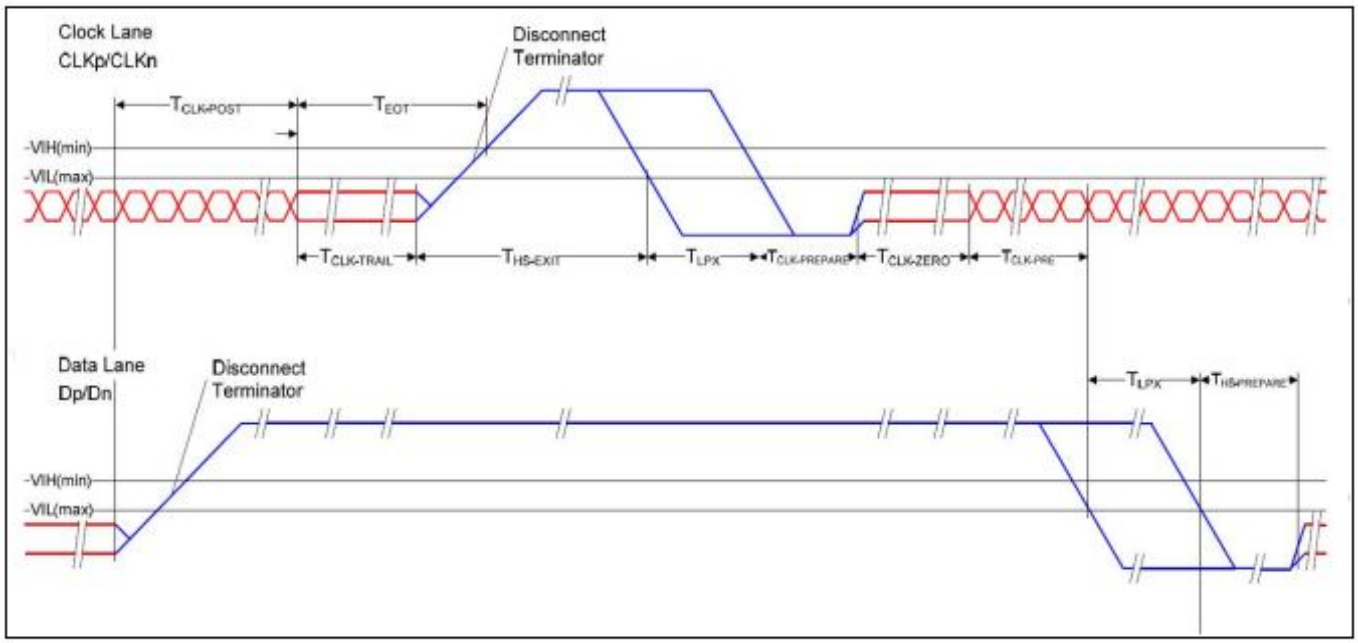


Figure11 MIPI switching the Clock Lane between Clock Transmission and LP mode

Table 8

Parameter	Description	Spec.			Unit
		Min.	Typ.	Max.	
$T_{CLK-MISS}$	Timeout for receiver to detect absence of Clock transitions and disable the Clock Lane HS-RX.			60	ns
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of $T_{HS-TRAIL}$ to beginning of $T_{CLK-TRAIL}$	60 ns +52*UI	-	-	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driver by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8	-	-	UI

$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-00 Line state starting the HS transmission.	38	-	95	ns
$T_{CLK-SETTLE}$	Time interval during which the HS receiver shall ignore any clock Lane HS transitions, starting from the beginning of $T_{CLK-PREPARE}$.	95	-	300	ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses V_{ILMAX}.	Time for Dn to reach VTERM-EN	-	38	ns
$T_{CLK-TRAL}$	Time that the transmitter drives the HS-00 state after the last payload clock bit of a HS HS transmission burst.	60	-	-	ns
$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + Time to that the transmitter drives the HS-00 state prior to starting the clock.	300	-	-	ns
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses V_{ILMAX}.	Time for Dn to reach VTERM-EN	-	35ns+4*UI	-
T_{EOT}	Transmitted time interval from the start of $T_{HS-TRAIL}$ or $T_{CLK-TRAL}$, to the start of the LP-11 state following a HS burst.	-	-	105 ns +n*12*UI	-
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following HS burst.	100	-	-	ns
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-00 Line state starting the HS transmission.	40ns+4*UI	-	85ns+6*UI	ns
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	$T_{HS-PREPARE}$ + Time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145 ns + 10*UI	-	-	ns
$T_{HS-SETTLE}$	Time interval during which the HS receiver shall ignore any Data Lane HS transitions , starting from the beginning of $T_{HSPREPARE}$	85 ns + 6*UI	-	145 ns +10*UI	ns
$T_{HS-SKIP}$	Time interval during which the HS-RX should ignore any transitions on the Data Lane, following a HS burst. The end point of the interval is defined as the beginning of the LP-11 state following the HS burst.	40	-	55 ns + 4*UI	ns
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	Max(n*8*UI, 60ns +n 4* UI)	-	-	ns
T_{INIT}	-	-	-	-	-
T_{LPX}	Transmitted length of any Low-Power state period	-	56.6	-	ns
Ratio T_{LPX}	Ratio of $T_{LPX(MARSTER)}/T_{LPS(SLAVE)}$ between Master and Slave side	2/3	-	3/2	

T_{TA-GET}	Time that the new transmitter drives the bridge state (LP-00) after accepting control during a Link Turnaround.	$5*T_{LPX}$			ns
T_{TA-GO}	Time that the new transmitter drives the bridge state (LP-00) before releasing control during a Link Turnaround.	$4*T_{LPX}$			ns
$T_{TA-SURE}$	Time that the new transmitter waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link turnaround.	T_{LPX}	-	$2*T_{LPX}$	ns
T_{WAKEUP}	Time that a transmitter drivers a Mark-1 state prior to a Stop state in order to initiate an exit from ULPS.	1			ms

7-1-4. AC Characteristics of MIPI DSI Characteristics

Table 9

Symbol	Parameter	Min.	Typ.	Max.	Unit
Thost-enable	Host output enable time	0	-	24*t-bit	ns
Thost-disable	Host output disable time, entire length of the Turnaround 1 field	0	-	24*t-bit	
Tclient-enable	Client output enable time, entire length of the Turnaround 1 field	0	-	24*t-bit	
Tclient-disable	Client output disable time, measured from the end of the last bit of the Turnaround 2 field.	0	-	24*t-bit	

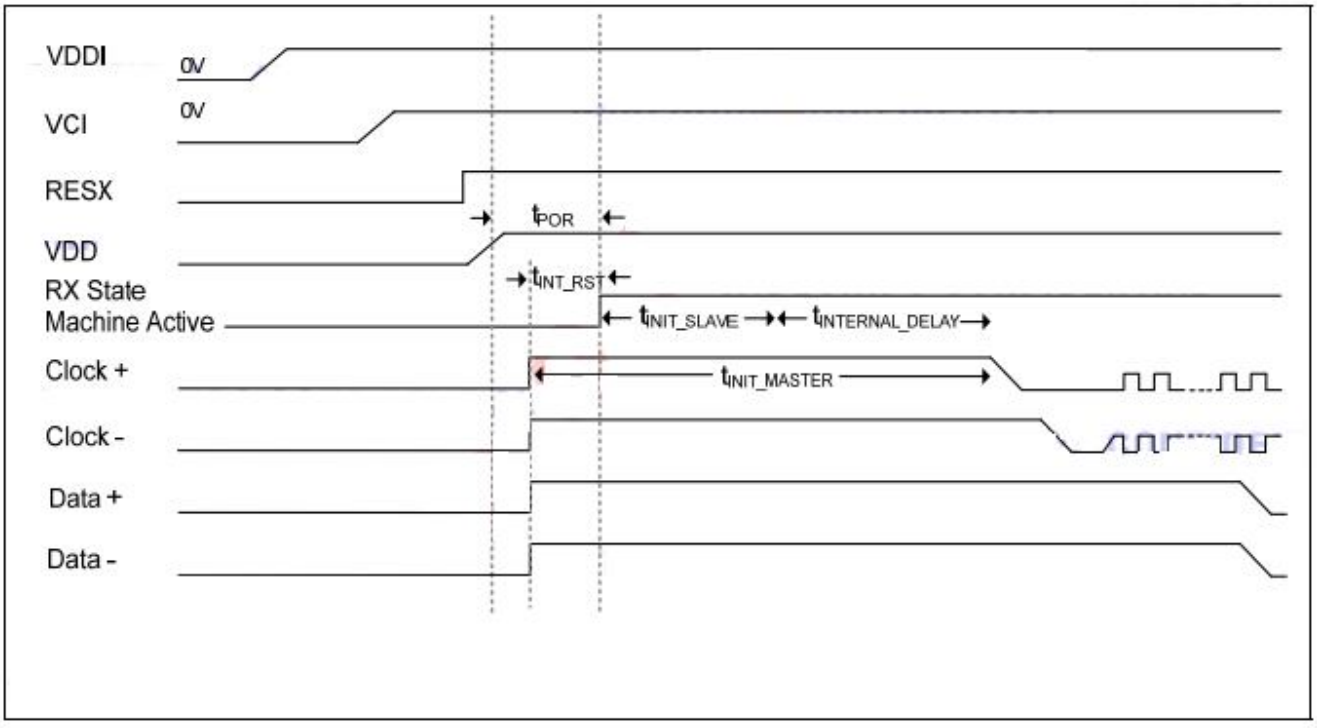


Figure 12

8. Recommended Operating Sequence

8-1. Display Power on/off Sequence

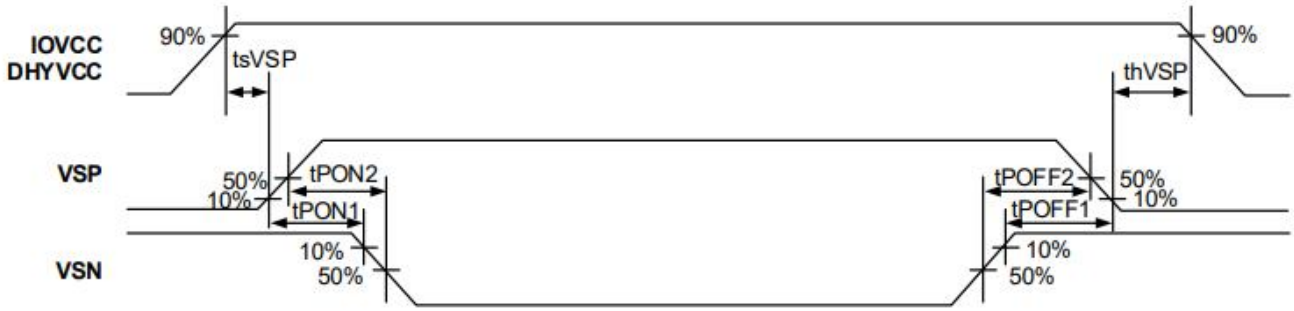


Figure 15 Power On/Off Sequence

Item	Symbol	Unit	Test Condition	Minimum	Maximum
VSP-VSN delay time (10% to 10%)	tPON1	μs	Power on	0	—
VSP-VSN delay time (50% to 50%)	tPON2	μs	Power on	0	—
System power on to VSP ON time	tsVSP	ms	Power on	1	—
VSN-VSP delay time (10% to 10%)	tPOFF1	μs	Power off	0	—
VSN-VSP delay time (50% to 50%)	tPOFF2	μs	Power off	0	—
VSP OFF to system power OFF time	thVSP	μs	Power off	0	—

Figure 15

8-1. Initial Code

Version: Rev0.
Diagonal Inch: 10.3

Table MIPI Setting

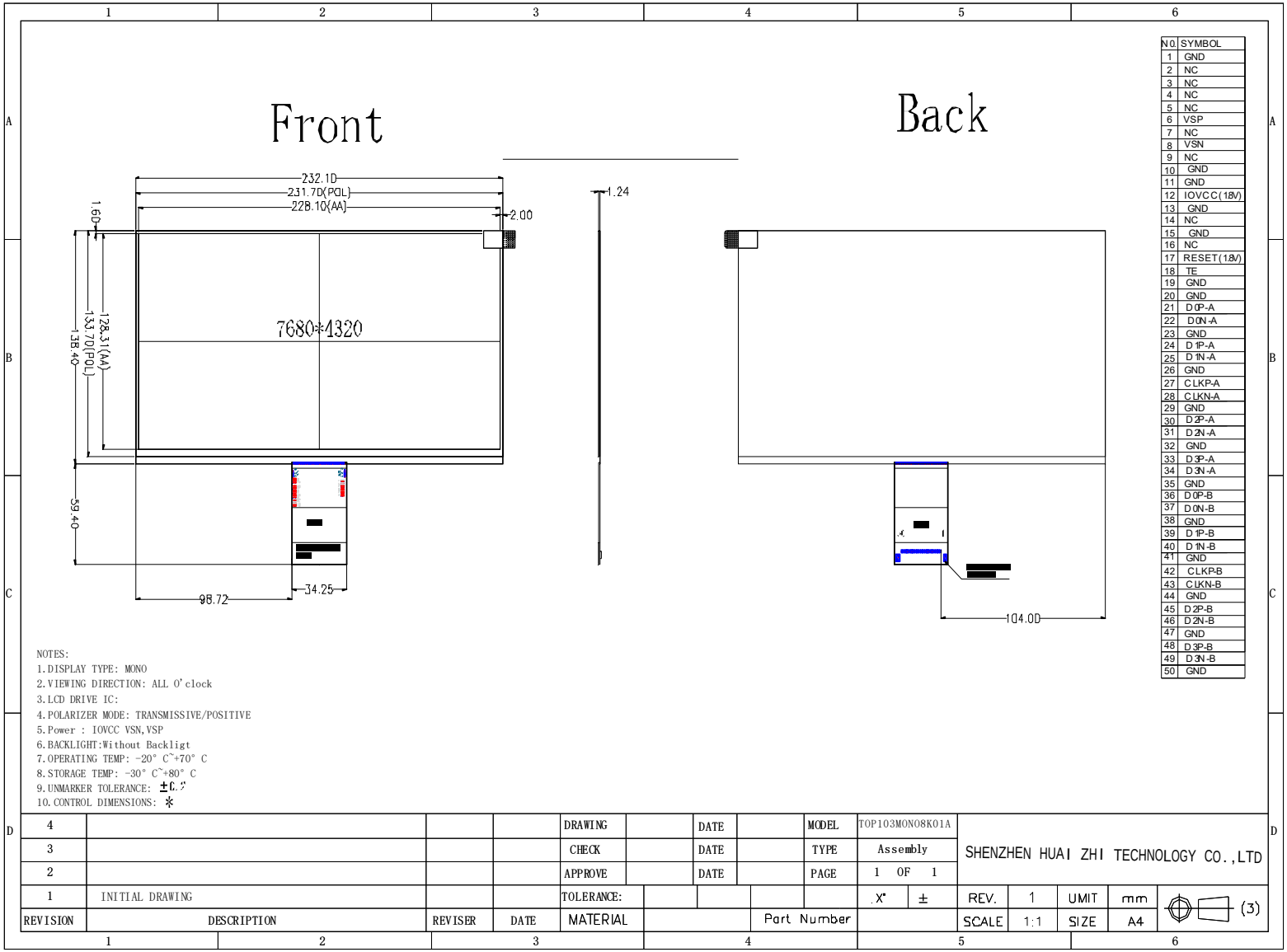
LABEL	SETTING	VALUE
(number)	Lane	8
1	x-size	2560
2	y-size	4320
3	HBP	44
4	HFP	56
5	HSW	3
6	VBP	6
7	VFP	25
8	VSW	3
9	PCLK	347.84MHZ
10	Frmae Rate	30HZ
11	GHS_Mbps	1050

Table Power Setting

Item	Voltage	Setting
input	VDDI	1.8
	ELVDD	5.5
	ELVSS	-5.5

9. Outline Information

9-1. Total Outline



NO.	SYMBOL
1	GND
2	NC
3	NC
4	NC
5	NC
6	VSP
7	NC
8	VSN
9	NC
10	GND
11	GND
12	IOVCC(1.8V)
13	GND
14	NC
15	GND
16	NC
17	RESET(1.8V)
18	TE
19	GND
20	GND
21	D0P-A
22	D0N-A
23	GND
24	D1P-A
25	D1N-A
26	GND
27	CLKP-A
28	CLKN-A
29	GND
30	D2P-A
31	D2N-A
32	GND
33	D3P-A
34	D3N-A
35	GND
36	D0P-B
37	D0N-B
38	GND
39	D1P-B
40	D1N-B
41	GND
42	CLKP-B
43	CLKN-B
44	GND
45	D2P-B
46	D2N-B
47	GND
48	D3P-B
49	D3N-B
50	GND

NOTES:
1. DISPLAY TYPE: MONO
2. VIEWING DIRECTION: ALL O'clock
3. LCD DRIVE IC:
4. POLARIZER MODE: TRANSMISSIVE/POSITIVE
5. Power : IOVCC VSN,VSP
6. BACKLIGHT:Without Backligt
7. OPERATING TEMP: -20° C~+70° C
8. STORAGE TEMP: -30° C~+80° C
9. UNMARKER TOLERANCE: ±0.3
10. CONTROL DIMENSIONS: ※

REVISION	DESCRIPTION	REVISER	DATE
4			
3			
2			
1	INITIAL DRAWING		

DRAWING		DATE		MODEL	TOP103MONO8K01A	SHENZHEN HUAI ZHI TECHNOLOGY CO.,LTD			
CHECK		DATE		TYPE	Assembly				
APPROVE		DATE		PAGE	1 OF 1				
TOLERANCE:				.X"	±	REV.	1	UMIT	mm
MATERIAL		Part Number				SCALE	1:1	SIZE	A4

(3)

10. Reliability

10-1. Environmental test

Table 16

No.	Item	Condition	Qnty	Result	Judgment Criterion
1	HTS	80℃,120hr,storage	5 ea	OK	1. No clearly visible defects or remarkable deterioration of display quality. However, any polarizer's deteriorations by the high temperature/ High humidity Storage test and the High temperature/ High humidity Operation test are permitted; 2. No function-related abnormalities; 3. Optical criteria: Color shift30°White △u'v' ≤4.8JNCD ; NTSC typ100% ; contrast ratio 100000:1 Response time <3ms ; LT95 300h Uniformity min80% ; Brightness typ350nit ;
2	LTS	-40℃,120hr,storage	5 ea	OK	
3	LTO	-20℃,24hr,operation	5 ea	OK	
4	THO	60℃/90%RH , 72hr,operation	10 ea	OK	
5	TST	-40℃~85℃, 1h/cycle , 100cycle	10 ea	OK	

11. Handling Precautions

11-1. Mounting Method

- Excessive stress or pressure on the glass of the LCD should be avoided. Care must be taken to insure that no torsional or compressive forces are applied to the LCD unit when it is mounted.
- If the customer's set presses on main parts of the LCD, the LCD may show the abnormal display. But this phenomenon does not mean the malfunction of the LCD and it should be pressed by the way of mutual agreement.
- To determine the optimum mounting angle, refer to the viewing angle range in the specification for each model.
- To mount LCD modules with the specified mounting method.

11-2. Handling & Cleaning Precautions

- Since the LCD is made of glass, DO NOT apply strong mechanical impact or static load onto it. Handling with care since shock, vibration, and careless handling may seriously affect the product. If it falls from a high place or receives a strong shock, the glass may be broken.
- The polarizers on the surface of panel are made from organic substances. Be very careful for any chemicals touch to the polarizers or it will lead the polarizers to be deteriorated.
- If the use of a chemical is unavoidable, use soft cloth with solvent（recommended below） to clean the LCD 's surface with wipe lightly.
  -IPA(iso-Propyl Alcohol),Ethyl Alcohol, Trichlorotrifluoroethane.
- Do not wipe the LCD 's surface with dry or hard materials that will damage the polarizers and others. Do not use the following solvent.
  -Water, Ketone, Aromatics
- It is recommended that the LCD be handled with soft gloves during assembly, etc. The polarizers on the LCD 's surface are vulnerable to scratch and thus to be damaged by sharp particles.
- Do not drop water or any chemicals onto the LCD 's surface.
- A protective film is supplied on the LCD and should be left in place until the LCD is required for operation.
- The ITO pad area needs special careful caution because it could be easily corroded.
- Do not contact the ITO pad area with HCFC, Soldering flux, Chlorine, Sulfur, saliva or fingerprint. To prevent the ITO corrosion, customers are recommended that the ITO area would be covered by UV or silicon. LCD should be stored in static-protective & vacuum polythene bag, please assembly it within 3 days after exposed to the air to avoid ITO corrosion.
- Do not clean the LCD with ultrasonic to avoid line open.
- Temperature of clean and bake should NOT be over 80℃.

11-3. Caution against Static Charge

- The LCD modules use C-MOS LSI drivers, so customers are recommended that any unused input

terminal would be connected to Vdd or Vss, do not input any signals before power is turn on, and ground body, work/assembly area, assembly equipments to protect against static electricity.

- Remove the protective film slowly, keeping the removing direction approximate 30-degree not vertical from panel surface, if possible, under ESD control device like ion blower, and the humidity of working room should be kept over 45%RH to reduce the risk of static charge.
- Avoid the use work clothing made of synthetic fibers. We recommend cotton clothing or other conductivity-treated fibers.
- In handling the LCD, wear non-charged material gloves. And the conducting wrist to the earth and the conducting shoes to the earth are necessary.

11-4. Caution for Operation

- It is indispensable to drive the LCD within the specified voltage limit since the higher voltage than the limit will shorten LCD 's lifetime. An electro-chemical reaction due to DC causes undesirable deterioration of the LCD so that the use of DC drive should avoid.
- Do not connect or disconnect the LCD to or from the system when power is on.
- Never use the LCD under abnormal conditions of high temperature and high humidity.
- When exposed to drastic fluctuation of temperature(hot to cold or cold to hot），the LCD may be affected. Specifically, drastic temperature fluctuation from cold to hot ,produces dew on the LCD 's surface which may affect the operation of the polarizer and the LCD.
- Response time will be extremely delayed at lower temperature than the operating temperature range and on the other hand at higher temperature LCD may turn black at temperature above its operational range. However those phenomena do not mean malfunction or out of order with the LCD.
- Do not display the fixed pattern for a long time because it may develop image sticking due to the LCD structure. If the screen is displayed with fixed pattern, use a screen saver.
- Static electricity (ESD) will damage the panel, Please make sure that operators wear static-protective glove effectively and working tables &device are effectively grounded during operation and other ESD protective method.
- LCD should be stored in required humidity due to the risk of static under low humidity, while corrode the ITO circuit under high humidity.

◆ **If WISECOCO has to change the conditions specified in the specification, previously the negotiation shall be held and decided.**

12. Packing Specification

12-1. Box Pack

TBD