ECE 154A Lab 5: Multicycle Processor

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Time spent:
Nov 23: 5 hours (4:30-9:30)
Nov 24: 7 hours (2 - 7:30 pm, 10:30 - 11:59 pm)
Nov 25: 2.5 hours (12:00-2:30 am)

Total: 14.5 hours

Table 1 (Completed Main Decoder output table)

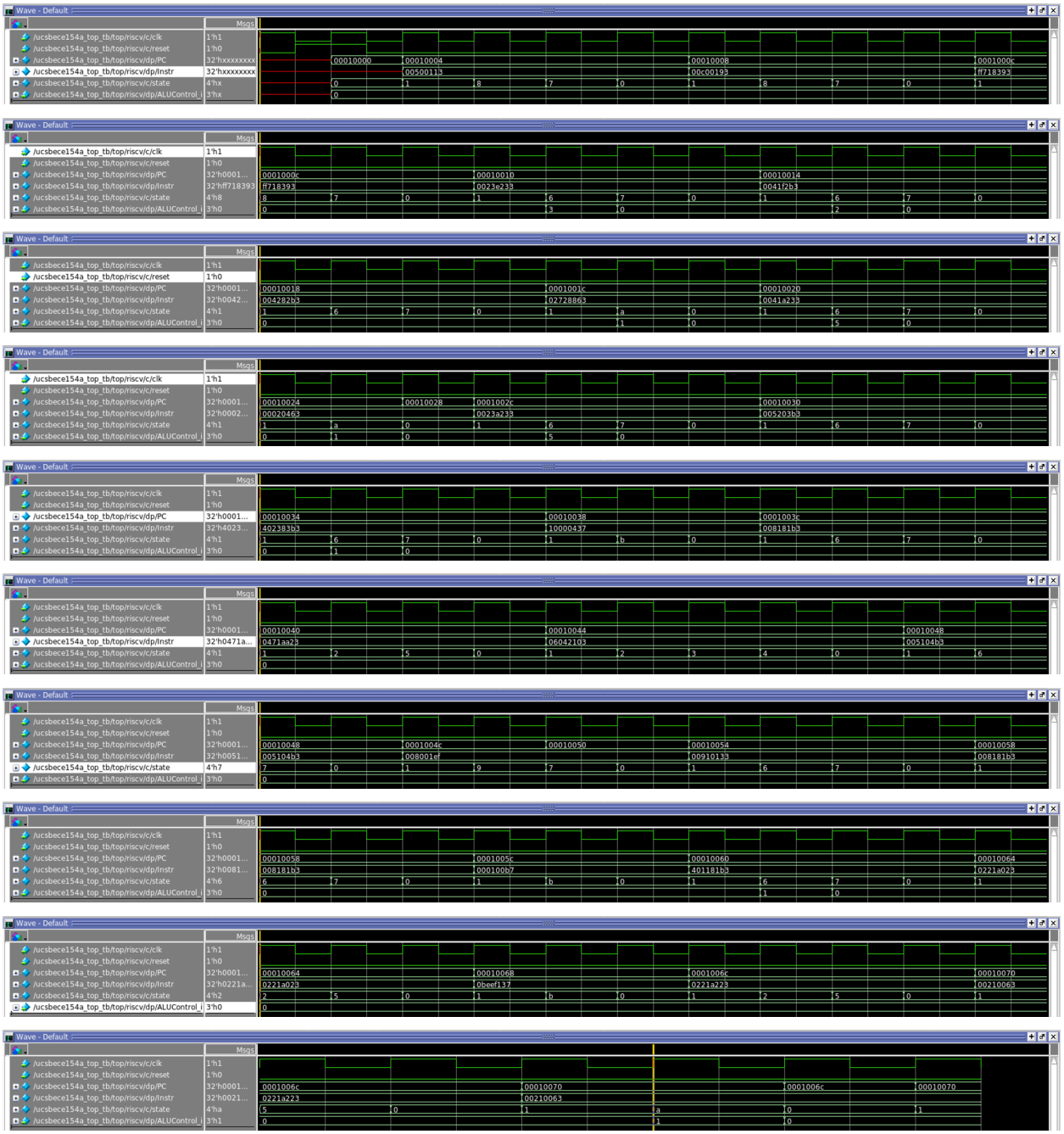
State (Name)	PCUpdate	MemWrite	IRWrite	RegWrite	ALUSrcA[1:0]	Branch	AdrSrc	ALUSrcB[1:0]	ResultSrc[1:0]	ALUOp[1:0]	ImmSrc[2:0]
0 (Fetch)	1	0	1	0	00	X	0	10	10	00	XXX
1 (Decode)	0	0	0	0	01	0	X	01	XX	00	010
2 (MemAdr)	0	0	0	0	10	0	X	01	XX	00	XXX
3 (MemRead)	0	0	0	0	XX	0	1	XX	00	XX	XXX
4 (MemWB)	0	0	0	1	XX	0	X	XX	01	XX	XXX
5 (MemWrite)	0	1	0	0	XX	0	1	XX	00	XX	XXX
6 (ExecuteR)	0	0	0	0	10	0	X	00	XX	10	XXX
7 (ALUWB)	0	0	0	1	XX	0	X	XX	00	XX	XXX
8 (ExecuteI)	0	0	0	0	10	0	X	01	XX	10	XXX
9 (JAL)	1	0	0	0	01	0	0	10	00	00	XXX
10 (BEQ)	0	0	0	0	10	1	X	00	00	01	XXX
11 (LUI)	0	0	0	1	XX	0	X	XX	11	XX	001

Table 2 (First 28 cycles)

Cycle	Reset	PC	Instr	(FSM) state	SrcA	SrcB	ALUResult	Zero
1	1	10000	xxxxxxxx	Fetch	10000	4	10004	0
2	0	10004	addi 00500113	Decode	10004	x	x	x
3	0	10004	addi 00500113	ExecuteI	0	5	5	0
4	0	10004	addi 00500113	ALUWB	x	x	x	x
5	0	10004	addi 00500113	Fetch	10004	4	10008	0
6	0	10008	addi 00C00193	Decode	10008	x	x	x
7	0	10008	addi 00C00193	ExecuteI	0	c	c	0
8	0	10008	addi 00C00193	ALUWB	x	x	x	x
9	0	10008	addi 00C00193	Fetch	10008	4	1000C	0
10	0	1000C	addi FF718393	Decode	1000C	x	x	x
11	0	1000C	addi FF718393	ExecuteI	C	FF7 (neg, so SUB)	1003	0
12	0	1000C	addi FF718393	ALUWB	x	x	x	x
13	0	1000C	addi FF718393	Fetch	1000C	4	10010	0
14	0	10010	or 0023E233	Decode	10010	x	x	x
15	0	10010	or 0023E233	ExecuteR	C	5	F	0
16	0	10010	or 0023E233	ALUWB	x	x	x	x
17	0	10010	or 0023E233	Fetch	10010	4	10014	0
18	0	10014	and 0041F2B3	Decode	10014	x	x	x
19	0	10014	and 0041F2B3	ExecuteR	C	F	C	0
20	0	10014	and 0041F2B3	ALUWB	x	x	x	x
21	0	10014	and 0041F2B3	Fetch	10014	4	10018	0
22	0	10018	add 004282B3	Decode	10018	x	x	x
23	0	10018	add 004282B3	ExecuteR	C	F	1B	0
24	0	10018	add 004282B3	ALUWB	x	x	x	x
25	0	10018	add 004282B3	Fetch	10018	4	1001c	0
26	0	1001C	beq 02728863	Decode	1001C	x	x	x
27	0	1001C	beq 02728863	BEQ	001B	1003	18 (-FE8)	0
28	0	1001C	beq 02728863	Fetch	1001C	4	10020	0

Waveforms

PART 1:



PART 2: All signals are displayed in hexadecimal and readable if you zoom.

PART 3: Yes, this matches our expectations.

Optional Feedback:

We encountered difficulties reading the instruction in for a few hours because we didn't realize we needed intermediate wires and registers for Src A and B - reminding students of this with a quick Verilog refresher before the lab would be nice.