FOWLP and Si-Interposer for High-Speed Photonic Packaging

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***Abstract*— A FOWLP and a Si-Interposer integration platform for Electronic IC (EIC) and Photonic IC (PIC) are described here. These two platforms are capable to support high-speed integration and scalable design of the next generation Optical Engine. The integration of the PIC on the FOWLP is achieved by a simple novel solution. An additional section of the Si substrate is designed at the end of the PIC to protect the optical I/Os during the FOWLP embedding process. For the Through Si-Interposer, besides providing the EIC and PIC, it include the passive alignment feature for the fibre to the PIC assembly.**

Keywords*— *FOWLP, Silicon photonics, Si Interposer, Optoelectronic integration

I. INTRODUCTION

The ever increasing demand for higher data bandwidth in the Data Centre has led to the requirement of higher speed, smaller form factors and scalable integrated Optical Engines (OE). The OE consists of various EIC and PIC to enable the optical/electrical (O/E) signal conversion. With the advancement in semiconductor device technology improvement, the packaging and integration technologies are becoming the limiting factor to realise the OE to meet the demand of the Data Centre high data bandwidth of more than 800Gbps requirement. Hence, it is important to develop a cost-effective PIC and EIC packaging platform to realise the high data rate OE. The integration and packaging technology must support the scaling of the number of the optical channel and provides high-speed electrical interconnect between the PIC and EIC of each channel of more than 100Gbps.

Advanced wafer level packaging has been successfully used in state of the art FPGA ICs, smart-phone application processors, and GPU units to provide power-performance-formfactor boosts that are not obtained by conventional packaging. A key benefit of advanced wafer level packaging is the capability to achieve heterogeneous integration whereby ICs from diverse technologies (CMOS, SiGe, SOI, PIC, III-V semiconductors etc.) can be independently optimized and tightly integrated in small formfactor packages to achieve power-performance-formfactor-cost optimization that is not otherwise possible with monolithic integration.

Data Centre OE uses ICs from diverse technologies such as CMOS/SiGe for drivers and amplifiers, III-V lasers. These ICs need to be integrated in very small formfactor system-in-package to be able to bring optical signals and convert them into electrical signals (and vice versa) to be processed by switches, FPGA or other ASICs. Thus, electronic-photonic heterogeneous integration enabled by advanced wafer level packaging is a promising technique to realize high-speed optical engines for the Data Centre.

For the best performance in term of speed, the EIC is integrated directly on top of the PIC. Currently, Silicon Photonic is the most promising technology which can provide the necessary performance and highest functionality integration. The PIC here is an active interposer, it not only consists of the photonic circuit but also provides the necessary physical area for the EIC and external routing and integration **Error! Reference source not found.**. However, this is a costly solution as the PIC will require an additional large area to support the EIC. In addition, for high-speed integration, Through Silicon Via (TSV) will be required to be used for the PIC active interposer. The fabrication of the TSV on the PIC requires many complex process steps as described in **Error! Reference source not found.**. Furthermore, the Si photonic circuit is fabricated in 200mm wafer instead of the 300mm wafer. These make the cost of this integrating solution unattractive for most of the commercial application. The alternative solution is using various complex customised multiple assembly technologies for the multi-chip module integration. However, due to the complex assembly requirement, and the limited scaling capability, this solution is not preferred.

IME is currently developing two packaging platforms based on the Fan-Out Wafer Level Packaging (FOWLP) and the Si-interposer to address the EIC and PIC integration requirement. The first solution is based on the established FOWLP technology, which has been demonstrated for Digital and RF/mmWave applications **Error! Reference source not found.** integration. The FOWLP has good RF performance and allows multi-chip heterogeneous integration is well suited for this high-performance OE application. For the Si-interposer with high resistivity substrate, it can also provide very high-speed and high

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bandwidth PIC and EIC integration. On top of this, it can provide a sub-micron alignment feature for the fibre to the PIC passive assembly.

II. PHOTONIC FOWLP

This FOWLP integration platform is for high-speed PIC and EIC integration. It is low cost and it leverages on the advanced of the FOWLP development for electronic semiconductor packaging. Currently, only the PIC with vertical coupling in FOWLP has been demonstrated **Error! Reference source not found.**, the integration of the edge PIC remains a big challenge. This is because the embedding mold compound is not transparent in the optical signal spectrum, and the optical signal cannot be coupled from the optical I/O at the edge of the PIC after molding. The optical I/O is very sensitive to contamination as the optical signal has a very short wavelength (~1.3µm to ~1.5µm), polishing and cleaning the package to revert the PIC edge I/O is very challenging and time consuming. To overcome this problem, the PIC optical I/O at the edge will be designed with an additional Silicon buffer section, as shown in **Error! Reference source not found.**. The Silicon buffet is just an additional section of the Si substrate of the PIC, extending beyond the edge optical coupling circuit. The PIC with this buffer section design is then embedded in the FOWLP process. The PIC buffer section protects the optical I/Os and will only be diced off during the singluation process to expose the PIC optical I/Os. Depending on the application requirement, the EIC can be either embedded side by side with the PIC or integrated on the top of the FOWLP PIC.

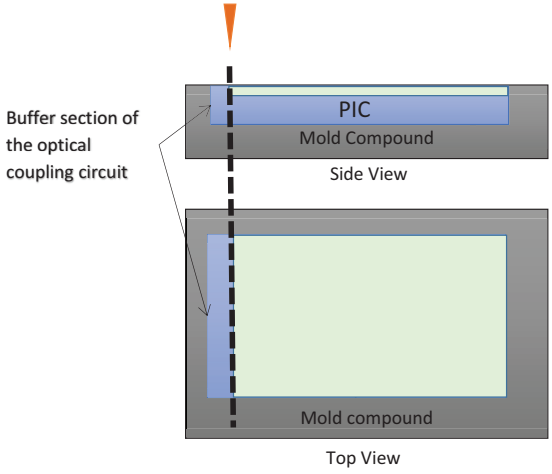


Figure 1: Schematic showing the FOWLP embedding solution of PIC with edge couple I/Os

The extended mold area of the FOWLP is used to support the electrical lateral and vertical routing connections using the Redistributing layer (RDL). The RDL can provide very fine line width connections and reduce the parasitic components with good impedance control for high-speed connections. The PIC and EIC can be integrated laterally with a gap of less than 500µm. In this way, it can achieve a very short electrical length and well match interconnect to support the high-speed and high density integration. Through Mold Via (TMV) can be designed on the FOWLP and the EIC can be stacked directly on the top of the PIC for 3D integration. Although this can help to reduce the package size, it increases the design and process complexity.

Error! Reference source not found. and **Error! Reference source not found.** show the schematic of the propose laterally integrated PIC and EIC using the FOWLP. The EIC here consists of the Driver for the photonic modulator and the Trans-Impedance Amplifier (TiA) for the Photodetector in the EIC. The FOWLP is designed for the flip-chip assembly on the substrate. Flip-chip assembly is preferred as it can provide high-speed and high bandwidth connection to the Switch IC or ASIC on the mainboard. In addition, the flip-chip assembly allows the heat sink to be designed directly on the backside of the EIC to reduce the thermal effect.

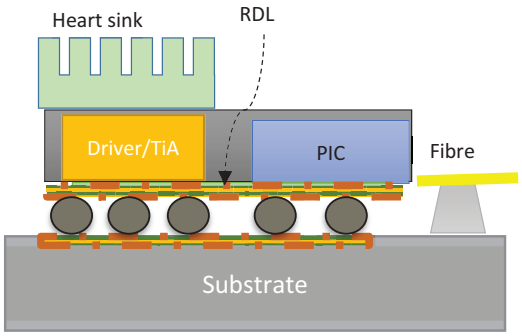


Figure 2: Schematic side view of the propose integrate PIC and EIC FOWLP flip-chip attached to substrate

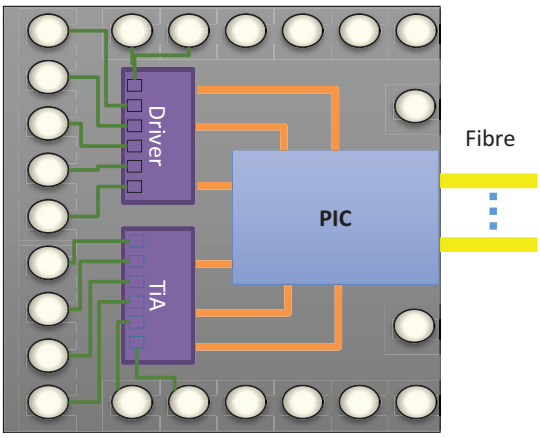


Figure 3: Schematic bottom view of the FOWLP with PIC and EIC (TiA and Driver)

For this integration design, the high-speed signal lines between the PIC and EIC, and the EIC to the external circuit are designed usually using differential transmission line. The

performance of the differentiate transmission lines of 1.0mm length is modelled using 3D EM simulator as shown in **Error! Reference source not found.**. The typical Dielectric Constant and the Loss Tangent of the mold compound is around 3.4 and 0.008, respectively. The simulated results are shown in **Error! Reference source not found.**, it has a Return Loss of more than 30dB and an Insertion Loss of less than 0.15dB up to 100GHz. The simulated results show that the FOWLP interconnect has a large bandwidth and is capable to support the high-speed digital signal in the OE. These high electrical performances are achieved mainly by short interconnect design.

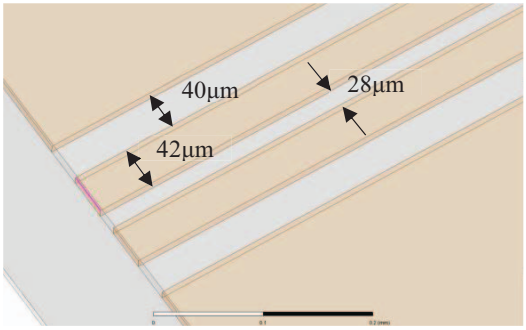


Figure 4: Simulation model of differentiate GSSG transmission line design on FOWLP.

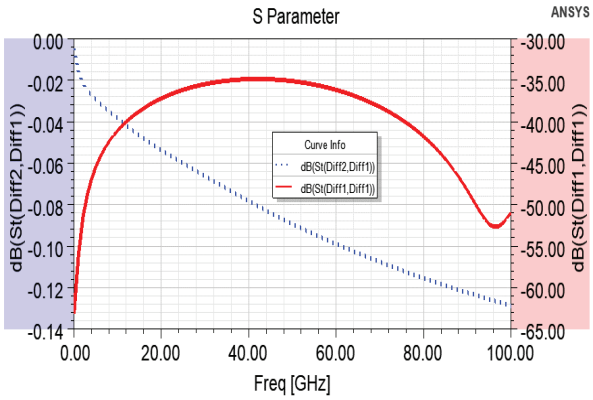
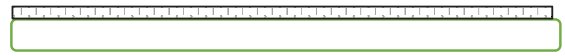


Figure 5: Simulation frequency response of the FOWLP differentiate transmission line up to 100GHz

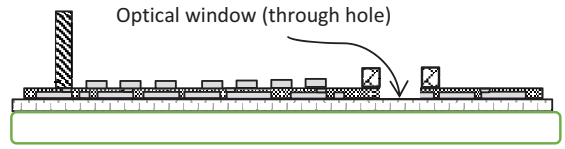
A. FOWLP Photonic Process

The key challenge of molding the PIC is to prevent contamination on the photonic I/O facets. The PIC is first singulate or diced at a distance from the photonic I/O so that a buffer area is formed. The buffer area is part of protection for the photonic I/O facet during the subsequence molding process.

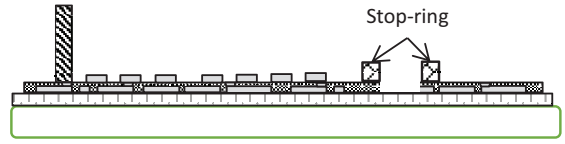
One of the possible processes for the FOWLP main process is described here. The steps are as similar as the RDL first process developed by IME**Error! Reference source not found.**. The additional process steps is to form the stop ring (dam) in **Error! Reference source not found.**. The stop ring is formed using polymer or other suitable material if necessary. It is used to prevent the underfill in the subsequent step from flowing to the optical I/O area or protected area. The singulate dicing process is designed so that the PIC buffer area and together with its surrounding mold are dice off at Step 7. The FOWLP of the EIC and PIC with optical edge coupled is formed. The integrated photonic FOWLP module can then be flip-chip assembled to the main optical board or substrate for the main integration. The process is compatible with the FOWLP process. IME is currently developing the complete process and evaluating the optical coupling performance.



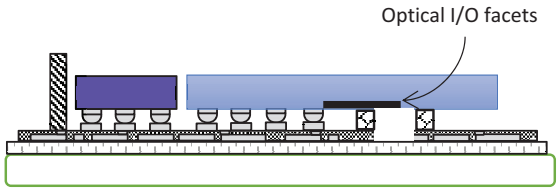
Step 1: Sacrificial layer coating on carrier



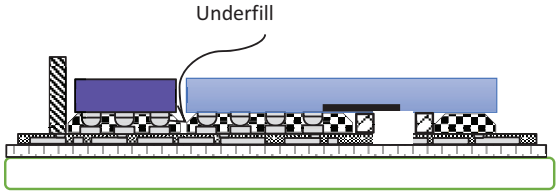
Step 2: RDL & Cu pillar TMV processing - RDL opening for Optical window



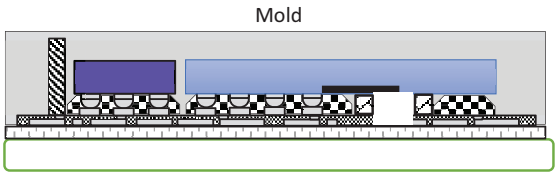
Step 3: Form stop-ring around Optical Window



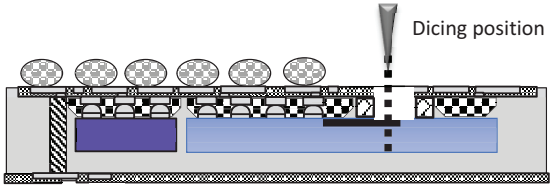
Step 4: Flip chip attached of PIC and EIC



Step 5: Apply underfill



Step 6: Wafer level compression molding



Step 7: Backside RDL, carrier removal, solder ball attachment.

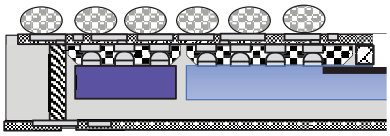


Figure 6: Propose FOWLP process flow for PIC embedding

III. PHOTONIC THROUGH SI-INTERPOSER

The other alternative integration platform for the EIC and PIC is based on the Through Si-interposer (TSI) which has also been well developed for high density electrical integration [**Error! Bookmark not defined.**]. The schematic of this overall integration design is as shown in **Error! Reference source not found.**. The TSI is used to integrate the EIC and PIC as well as to support the fibre assembly for the PIC. The main advantage of this Si-interposer is that it can provide the high alignment accuracy feature for the multi-channel optical fibre alignment and assembly. For all photonic communication circuits, the optical signal of the PIC must be eventually coupled to the optical fibre for external connection. The fibre assembly needs to achieve a high alignment accuracy in the range of less than 2 or 1μm to achieve good optical coupling efficiency.

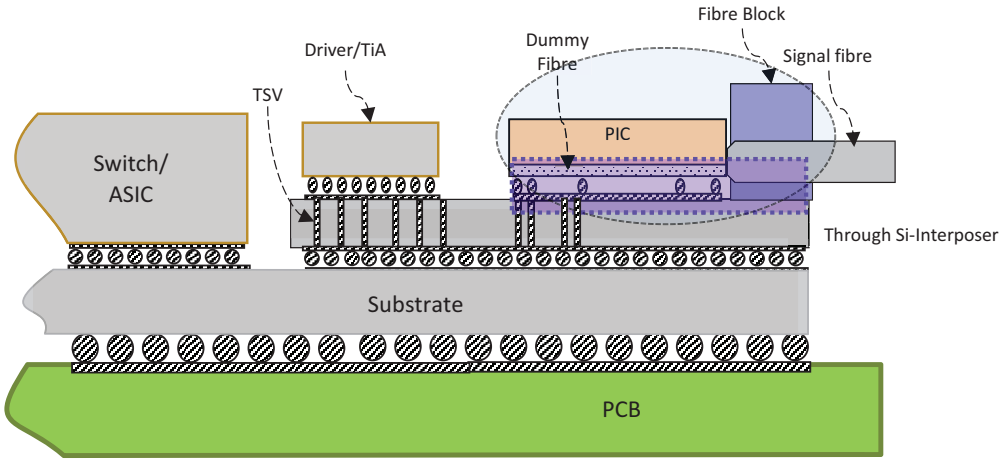


Figure 7: Proposed solution using Si Interposer to provide the fibre coupling and integration for PIC and EIC

In this fibre-to-PIC assembly propose solution, the Si-Interposer serves as a base substrate to support the PIC and a Fibre Block which hold the optical fibre array, as shown in **Error! Reference source not found.**. The alignment of the PIC and the Fibre Block is achieved by a pair of alignment or Dummy Fibre place on the deep trench or U-groove of the Si interposer. The Si-interposer is designed with a set of U-groove along its length. The U-groove is formed using a dry etch process which is compatible with the PIC and TSI.

The PIC and the Fibre Block will also have a set of matching U-groove designed along its length of the device. When the PIC and the Fibre Block are assembled faced down on the Si-interposer, with the U-groove of the PIC and the Fibre Block align on the Dummy Fibre of the Si-interposer, only the edge of the U-groove will be physically contacted the Dummy Fibre. **Error! Reference source not found.** shows the concept of using the U-groove edge to support the fiber. In this way, the optical axis of the fibre and the PIC waveguide will be self-aligned with a vertical height offset determined by the width of the deep trench and the diameter

of the Dummy Fibre. The Dummy Fibre which is a standard bare optical fibre is used as a cylindrical mechanical alignment and support features due to its inherent high precision diameter and yet low cost. The standard optical bare fibre has a very precise diameter of 125µm diameter (Ø) ±0.7µm. For this fibre to the PIC alignment solution, it relies only on the edges of the U-groove which are used to support the alignment fibre. The depth and profile of the U-groove are not critical as it does not have any physical contact with the U-groove. As epoxy will be applied in the U-groove to assemble the alignment fibre, the depth of the U-groove just has to be deep enough to support the epoxy volume without pushing up the fibre or affect the fibre position. More detail on the Si-interposer design can be found in [**Error! Bookmark not defined.**].

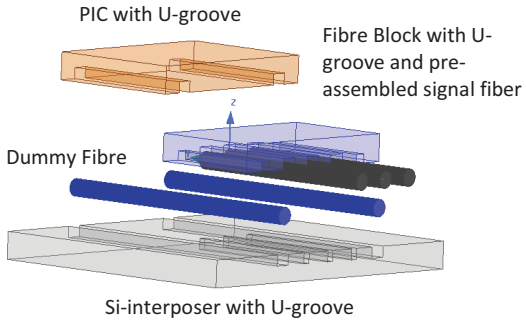


Figure 8: Side View of the Si Electrical Optical Interposer

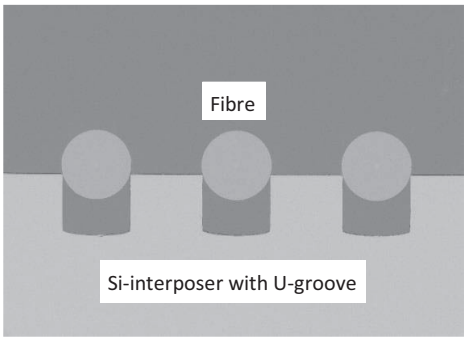


Figure 9: Cross-section of the test vehicle assembly showing the U-groove edge supporting the fiber

It is noted that the coupling efficiency also depends on the performance of the optical coupler of the PIC. An optical coupler is usually used to mitigate the coupling loss due to the large mode size mismatch between the fibre and the optical waveguide. Besides having low coupling loss, the optical coupler should have a large misalignment tolerance to relax the alignment accuracy requirement. For these reasons, the suspended coupler designed is the preferred design over the typical inverse tapered coupler. The reported suspended coupler **Error! Reference source not found.** has a 1dB excess loss of more than 2µm in the cross-section misalignment, and more than 40µm along the fibre direction. The performance of the suspended coupler well matches the requirement of this Si-interposer integration platform.

Both the PIC and the EIC are flip-chip assembled on the Si-interposer. Usually, the front side electrical connection of the interposer is formed using BEOL, which support the bare die assembly using micro solder bump. Typically, up to 3 BEOL can be formed on the top side of the Si-interposer to support the front side routing. The minimum BEOL line width is around 0.8µm, this is more than sufficient to support all the electrical routing between the PIC and the EIC. The electrical connection on the backside of the interposer is formed using RDL, which has a much larger line width resolution. As most likely the top side BEOL has provided all the electrical routing, the backside RDL is used mainly to support the solder bump for the assembly of the Si-interposer to the substrate or PCB. The electrical connection between the BEOL and the RDL is using the TSV. The TSV helps to overcome the bandwidth limiting inductance of the wire bond and increases the I/O density of the interconnect. For high-speed electrical connection, high resistivity Si wafer is required to reduce the electrical loss.

For the TSI integration, the length of the TSV has to be much greater than the U-groove depth. The Dummy Fibre is designed to be supported by the edge of the U-groove, hence the depth of the U-groove needs to be deep enough so that it can accommodate the epoxy without overflow or push up the Dummy Fibre. Based on the preliminary design, the depth of the U-groove needs to be more than 50µm, but to prevent the Si-interposer breakage during handling, it is recommended to increase the height of the Si-interposer to about 200µm.

The EM simulated response of a differential GSSG TSV with a height of 200µm is as shown in **Error! Reference source not found.** below. The typical aspect ratio of the TSV is 1:10, hence for a 200µm height TSV the diameter will be around 20µm. The pitch of the TSV is set to 100µm, and a high resistivity wafer of 700Ω.cm is used. As shown in **Error! Reference source not found.**, the simulated ideal Insertion Loss is less than 0.5dB and the Return Loss is more than 10dB up to 100GHz. Again, the simulated result shows that the TSI can support the high-speed high density EIC and PIC integration for the Date Centre OE.

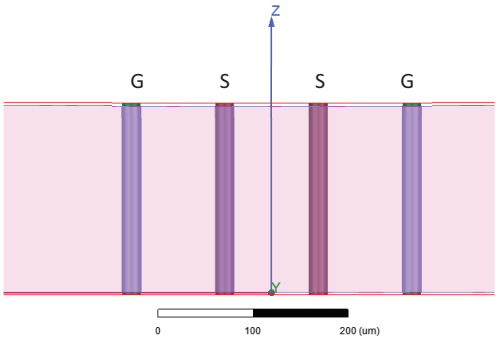


Figure 10: GSSG TSV model

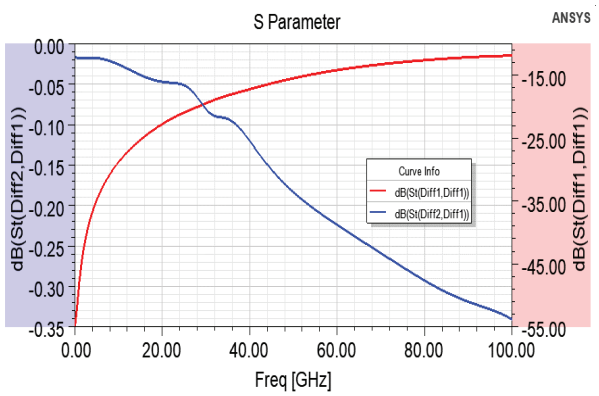


Figure 11: Simulated frequency response of the Differentiate TSV

IV. CONCLUSION

Two EIC and PIC integration platforms are proposed here. The FOWLP and the TSI platforms allow the PIC and the EIC to be integrated close together with high density routing. This helps to improve the electrical performance and reduce the form factor, which are required to meet the current and future OE for the Data Centre. For the FOWLP platform, the main solution to enable the embedding of the edge coupled PIC has been illustrated. An extra section of the Silicon substrate is designed on the PIC to protect the optical I/O. This additional section of Silicon substrate is diced off after the FOWLP process to expose the PIC optical I/Os. This design is simple and is compatible with the current FOWLP process. This will enable the high-speed photonic circuit to be integrated using the cost effective FOWLP.

For the Through Si-interposer integration platform, besides providing the high-speed PIC and EIC integration, it provides the alignment feature for the fibre to the PIC assembly. Together with the PIC optical coupler, the fibre can be aligned using passive alignment, which is one of the main photonic packaging challenges.

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REFERENCES

[1] Gilles Denoyer;Chris Cole;Antonio Santipo;Riccardo Russo;Curtis Robinson;Lionel Li;Yuxin Zhou;Jianxiao "Alan" Chen;Bryan Park;Frédéric Boeuf;Sébastien Crémer;Nathalie Vulliet, "Hybrid Silicon Photonic Circuits and Transceiver for 50 Gb/s NRZ Transmission Over Single-Mode Fiber", Journal of Lightwave Technology, Year: 2015 | Volume: 33, Issue: 6

[2] Yan Yang ; Mingbin Yu ; Qing Fang ; Junfeng Song ; Xiaoguang Tu ; Patrick Guo-Qiang Lo ; Rusli, , "3D Silicon Photonics Packaging Based on TSV Interposer for High Density On-Board Optics Module ", 2016 IEEE 66th Electronic Components and Technology Conference (ECTC)

[3] "FOWLP Design for Digital and RF Circuits", Teck Guan Lim;David Soon Wee Ho;Eva Wai Leong Ching;Zihao Chen;Surya Bhattacharya 2019 IEEE 69th Electronic Components and Technology Conference (ECTC)

[4] Hiroshi Uemura;Kaori Warabi;Kazuya Ohira;Yoichiro Kurita;Haruhiko Yoshida;Hideto Furuyama;Yoshiaki Sugizaki;Hideki Shibata, "Backside Optical I/O Module for Si Photonics Integrated with Electrical ICs Using Fan-Out Wafer Level Packaging Technology", 2018 IEEE 68th Electronic Components and Technology Conference (ECTC)

[5] "Development of High Density Fan Out Wafer Level Package (HD FOWLP) with Multi-layer Fine Pitch RDL for Mobile Applications", Vempati Srinivasa Rao;Chai Tai Chong;David Ho;Ding Mian Zhi;Chong Ser Choong;Lim P.S. Sharon;Daniel Ismael;Ye Yong Liang, 2016 IEEE 66th Electronic Components and Technology Conference (ECTC)
"Silicon Optical Electrical Interposer - Fiber to the Chip", Lim Teck Guan;Li Hong Yu;Jong Ming Chinq;Eva Wai Leong Ching;Chong Ser Choong;Lim Soon Thor;Thomas Y. L Ang;Ong Jun Rong, 2019 IEEE 21st Electronics Packaging Technology Conference (EPTC)

[6] Jayasanker Jayabalan;Vivek Chidambaram;Sharon Lim Pei Siang;Wang Xiangyu;Jong Ming Chinq;Surya Bhattacharya, "Active Through-Silicon Interposer Based 2.5D IC Design, Fabrication, Assembly and Test", 2019 IEEE 69th Electronic Components and Technology Conference (ECTC)

[7] Jia Lianxi;Liow Tsung-Yang;Li Chao;Luo Xianshu;Tu Xiaoguang;Huang Ying;Zhou Haifeng;Yu Mingbin;Patrick Lo, "High efficient suspended coupler based on IME's MPW platform with 193nm lithography", 2017 Optical Fibre Communications Conference and Exhibition (OFC)