Heterogeneously integrated silicon-conductive oxide MOSCAP microring modulator array

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Abstract: In pursuit of energy-efficient optical interconnect, silicon microring modulator (Si-MRM) has emerged as a pivotal device offering an ultra-compact footprint and capability of on-chip wavelength division multiplexing (WDM). This paper presents a 1 × 4 metal-oxide-semiconductor capacitor (MOSCAP) Si-MRM array gated by high-mobility titanium-doped indium oxide (ITiO), which was fabricated by combining Intel's high-volume manufacturing process and the transparent conductive oxide (TCO) patterning with the university facility. The 1 × 4 Si-MRM array exhibits a high electro-optic (E-O) efficiency with V_{π}·L of 0.12 V·cm and achieves a modulation rate of (3×25 + 1×15) Gb/s with a measured bandwidth of 14 GHz. Additionally, it can perform on-chip WDM modulation at four equally spaced wavelengths without using thermal heaters. The process compatibility between silicon photonics and TCO materials is verified by such industry-university co-fabrication for the MOSCAP Si-MRM array and demonstrated enhanced performance from heterogeneous integration.

1. Introduction

With the exponentially growing data traffic, the quest for energy-efficient and scalable on-chip optical communication systems has become more imperative [1,2]. Silicon photonics plays a pivotal role in optical interconnects and optical computing by offering high bandwidth and large-scale integration on a matured platform that is compatible with CMOS industry [3]. On-chip wavelength division multiplexing (WDM) allows simultaneous modulation and detection at multiple wavelengths through a single physical channel, which can significantly improve the bandwidth density of silicon photonics [4,5]. As the ideal device for on-chip WDM, silicon microring modulator (Si-MRM) offers ultra-compact footprint, low energy consumption, and wavelength multiplexing/demultiplexing simply by changing the radius of the ring [6]. By coupling multiple Si-MRMs with slightly different radii to a single bus waveguide [7], it will enable electro-optic (E-O) modulation at various wavelengths concurrently, thereby maximizing the bandwidth density of photonic integrated circuits (PICs). Several on-chip WDM systems using Si-MRM array based on reversed PN junctions have demonstrated large-scale integration with aggregated bandwidth by leveraging the top-quality fabrication capability offered by silicon photonics foundries [8–17]. However, the E-O efficiency of Si-MRMs by commercial foundries is limited by the relatively weak plasma dispersion of silicon and the low capacitance density of reversed PN junctions as discussed in Ref. [18]. To address such intrinsic weakness, silicon photonic devices driven by the metal-oxide-semiconductor capacitor (MOSCAP) incorporating a thin insulator layer, such as hafnium oxide (HfO_2), provide improved E-O efficiency [19,20]. Moreover, MOSCAP devices allow heterogeneous

integration with other semiconductors such as III-V compounds, transparent conductive oxides (TCOs), and graphene, which offers larger refractive index modulation [21–23]. Previous work on MRMs utilizing MOSCAP gated by various materials have demonstrated enhanced E-O modulation performance [24–28]. However, these reports only covered individual Si-MRM device, which do not answer uncertainties of scalability to large-scale integration considering the challenge of process compatibility of heterogenous integration.

In this article, we demonstrate a 1 × 4 MOSCAP-driven Si-MRM array heterogeneously integrated with high-mobility titanium-doped indium oxide (ITiO), which can perform on-chip WDM modulation. The ITiO-gated MOSCAP Si-MRM performs non-return-to-zero (NRZ) modulation with open eye diagrams up to 30 Gb/s. Additionally, it showcases an enhanced E-O efficiency $V_\pi \cdot L$ of 0.12 V·cm, surpassing traditional Si-MRMs using PN junctions where $V_\pi \cdot L$ often exceeds 0.5 V·cm [12,29]. Our previous work has shown that a MOSCAP-driven Si-MRM with a gate bias can obtain high E-O efficiency, enabling substantial wavelength tuning, which can effectively compensate temperature variations and fabrication errors [30,31]. In this work, we introduce a moderate gate bias to fine-tune the resonant spectra of Si-MRMs with minimal power consumption. This approach demonstrates the feasibility of tailored modulation performance while maintaining equally spaced working wavelengths for possible integration with comb lasers. Ultimately, the 1 × 4 Si-MRM array achieves a throughput of (3 × 25 + 1×15) Gb/s with a maximum E-O bandwidth of 14 GHz. The MOSCAP Si-MRM array was fabricated using Intel's high-volume manufacturing process and the TCO layer was patterned with the university fabrication facility. This work demonstrates a heterogeneous integration of MOSCAP Si-MRM array for on-chip WDM, marking a significant milestone of the development of MOSCAP modulators towards large-scale PICs.

2. Design and fabrication

2.1 Device design

The ITiO-gated Si-MRM array is illustrated in Fig. 1(a) with four ring resonators, of which the radii vary from 6.00 μm, 6.02 μm, 6.04 μm, to 6.06 μm to operate at four equally spaced wavelengths. Fig. 1 (b) shows the cross-sectional view of the active region of the Si-MRM, which comprises of an ITiO/HfO_2/Si MOSCAP with ITiO as the gate and HfO_2 as the insulator. The silicon ring waveguide acts as the bottom substrate of the MOSCAP, featuring a 300 nm thick silicon rib waveguide with a 100 nm slab thickness. The waveguide width of the microring is designed to be 300 nm to optimize E-O efficiency [31]. In contrast to our prior work [31], the doping profile of silicon in this work is properly designed to reduce the series resistance, thereby enhancing the modulation speed. The entire Si-MRM incorporates a background Si p-doping (1×10^{17} cm^{-3}). The top of the ring waveguide, including part of the silicon slab, features Si p+ doping (3×10^{18} cm^{-3}). Additionally, the metal contact region is doped with Si p++ (1×10^{20} cm^{-3}) and is approximately 600 nm away from the ring waveguide.

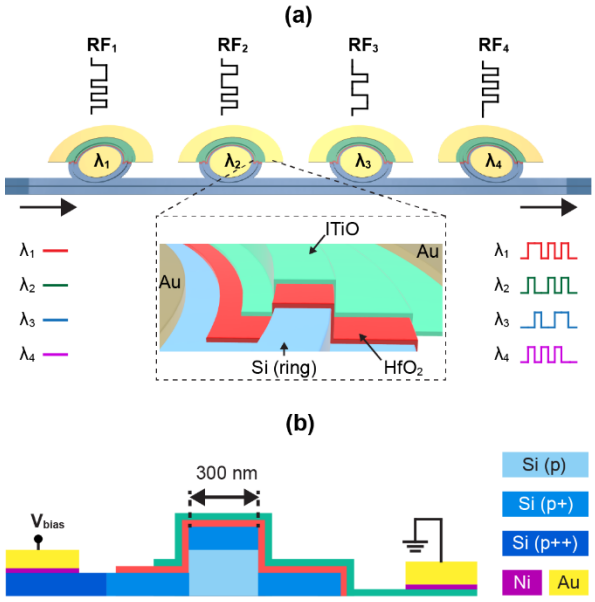

Fig. 1. (a) Schematic of the 1×4 ITiO-gated MOSCAP Si-MRM array for on-chip WDM modulation. Inset: close-up view of the Si-MRM featuring an ITiO/HfO_2/Si MOSCAP structure. (b) Cross-sectional view of the active region of the ITiO-gated MOSCAP Si-MRM.

2.2 Device fabrication

The 1 × 4 ITiO-gated MOSCAP Si-MRM array was co-fabricated utilizing Intel's HVM silicon photonics fab alongside the TCO patterning techniques that we developed. The fabrication procedures are illustrated in Fig. 2.

(a) The silicon microring array, with radii of 6.00 μm, 6.02 μm, 6.04 μm, and 6.06 μm, respectively, was fabricated on a Silicon-on-Insulator (SOI) wafer using Intel's 300 mm HVM silicon photonics process, involving Si p, p+, and p++ doping. A SiO_2 top cladding was deposited to safeguard the underlying silicon microring array.

(b) To integrate MOSCAP onto the doped silicon waveguide layer with TCO gates, the top SiO_2 cladding surrounding the active regions of the microrings underwent patterning via photolithography, followed by reactive ion etching (RIE) with Ar/CHF_3 gas mixture. This process exposed parts of the microrings while ensuring that both the bus waveguide and the coupling regions between the bus waveguide and microrings are covered by the SiO_2 cladding.

(c) A 10 nm HfO_2 insulator layer was uniformly deposited across the entire SOI substrate using atomic layer deposition (ALD), utilizing Tetrakis (ethylmethylamino) hafnium (TEMA-Hf) as the precursor and H_2O as the oxygen source at 300 °C.

(d) Subsequently, a 14 nm ITiO layer was RF-sputtered onto the HfO_2 layer at a high substrate heating temperature of 500 °C, covering the entire wafer.

(e) To ensure the ITiO layer is only present at the active regions, a two-step patterning process was employed. Firstly, electron beam lithography (EBL) precisely defined the desired ITiO pattern within the active regions, followed by RIE etching of ITiO with HBr gas. Secondly, photolithography was utilized to shield the active regions, facilitating selective removal of the residual ITiO layer using wet etching (ITO etchant). These sequential processes guaranteed that the ITiO layer was selectively deposited only over the active regions of the microrings.

(f) Next, the HfO_2 layer in the silicon contact regions was patterned using EBL and removed by RIE with Ar/CHF_3 gas mixture.

(g) Finally, metal contacts were formed by thermal evaporation of Ni/Au metals, forming Ohmic contacts with both ITiO gates and the silicon bottom substrates.

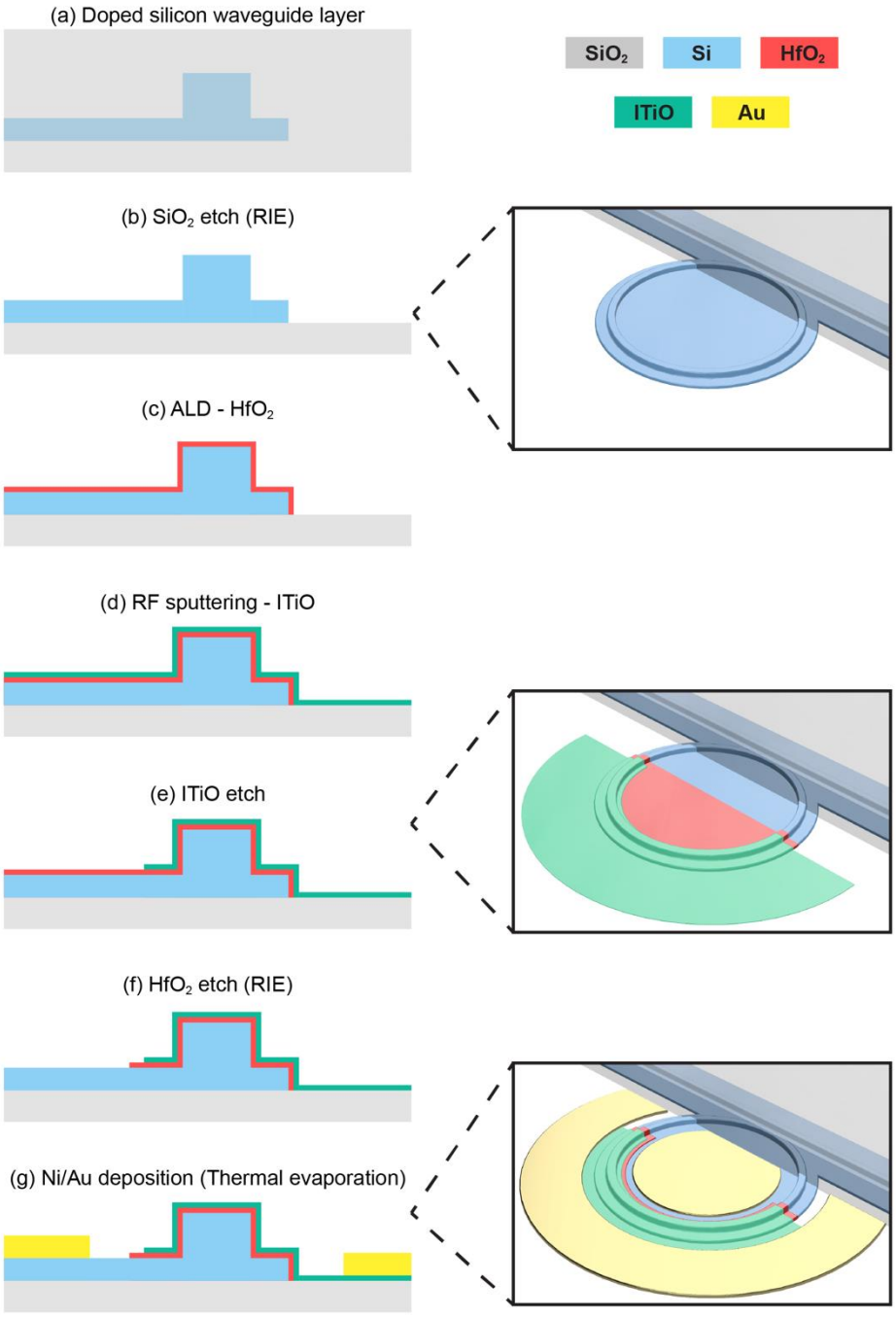

Fig. 2. Illustration of the co-fabrication process flow for the ITiO-gated MOSCAP Si-MRM array. Note: The depiction shows HfO_2 exclusively in the active region, whereas it is actually applied throughout the entire substrate.

Fig. 3 showcases the co-fabricated 1 × 4 ITiO-gated MOSCAP Si-MRM array. In Fig. 3(a), there are four cascaded passive silicon microring resonators coupled to a bus waveguide with two grating couplers. Fig. 3(b) displays the completed Si-MRM array after undergoing the comprehensive TCO patterning process. Additionally, the inset image of Fig. 3(b) offers detailed perspectives of the active region, illustrating the ITiO coverage to the silicon microring waveguide to form the ITiO/HfO_2/Si MOSCAP structure. Fig. 3(c) presents the measured transmission spectra for on-chip WDM modulation. Due to slight variations in the radius of each silicon microring, four resonant wavelengths are fitted within a free spectral range (FSR) of 11.6 nm. Additionally, the inset image of Fig 3(c), which was captured by an infrared camera, highlights the light confinement observed in one of the Si-MRMs at its respective resonant wavelength.

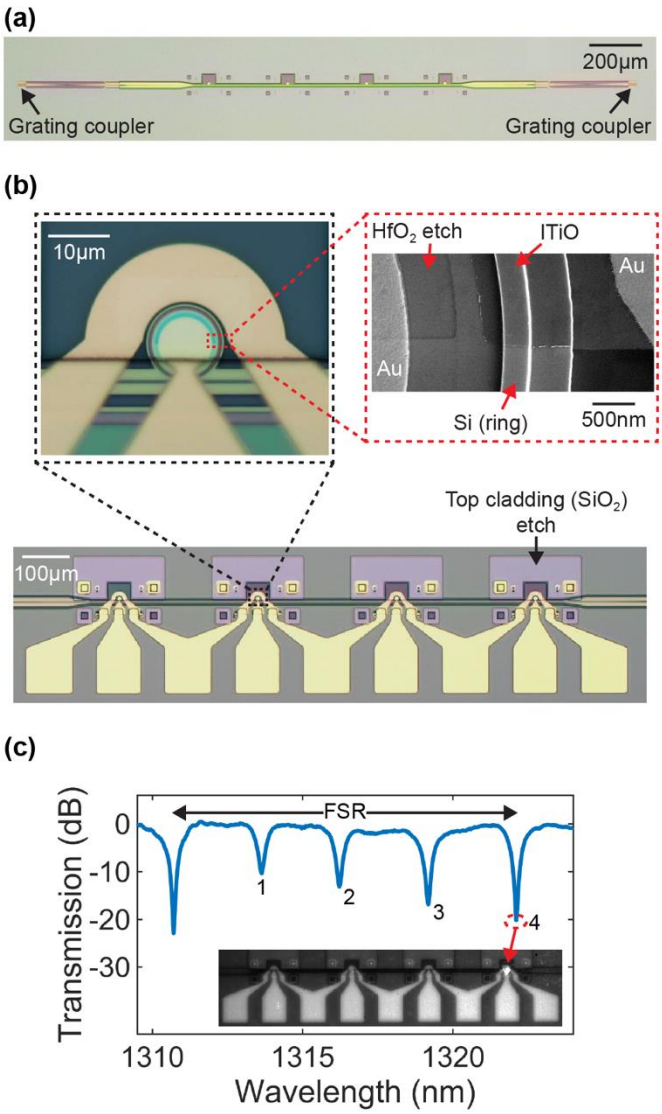

Fig. 3 (a) Optical microscope image of the 1 × 4 silicon microring resonator array fabricated by Intel. (b) Optical microscope image of the co-fabricated Si-MRM array. Inset: close-up view of the ITiO-gated MOSCAP Si-MRM and the Scanning Electron Microscope (SEM)

image illustrating the active region formed by the ITiO/HfO_2/Si MOSCAP structure. (c) Measured transmission spectrum, revealing an FSR of 11.6 nm. Inset: the 1×4 ITiO-gated MOSCAP Si-MRM captured under an infrared camera, showing light confinement within a Si-MRM at its resonant wavelength.

3. Device characterization

3.1 DC characterization

Each ITiO-gated MOSCAP Si-MRM in the array was individually characterized. In Fig. 4(a), the normalized transmission spectra of these Si-MRMs are presented under various gate biases. The increment in bias voltages induces a reduction in the effective index of the waveguide, consequently causing a blue shift of the microring resonance. The MOSCAP Si-MRM array showcases E-O efficiency ranging from 80 pm/V to 105 pm/V, with an average $V_\pi \cdot L$ of 0.12 V·cm. However, it exhibits relatively low Q-factors from 2100 to 2600. Since the radii are approximately 6 µm, these microrings are more sensitive to sidewall roughness [32]. The SiO_2 cladding etch during fabrication (as shown in procedure (b) in Fig 2) may have introduced additional roughness to the silicon microring waveguide. Therefore, the Q-factors of these microrings are lower than our previous work, where a larger radius of 8 µm was utilized [27].

Furthermore, Fig. 4(b) illustrates the E-O transfer curve at different working wavelengths for each channel, represented by different colors. The observed non-linearity of the E-O transfer curve is attributed to the Lorentz shape of the microring transmission. The E-O efficiency and Q-factor play crucial roles in determining the extinction ratio (ER) of the modulation. The E-O efficiency influences the shift in the transmission spectrum, while the Q-factor affects the sharpness of the transmission spectrum. For example, with an insertion loss (IL) of 3 dB, both channel 1(CH1) and channel 2 (CH2) attain an ER above 6 dB with a 2 V_{pp} voltage swing. In contrast, CH3 and CH4, which have relatively lower Q-factors and E-O efficiencies, achieve an ER of less than 6 dB under the same IL and voltage swing. To ensure efficient E-O modulation across every channel within the modulator array, a V_{pp} of 3V is chosen for all channels. This choice is intended to achieve optimal and practical modulation performance, adhering to the criteria of an IL below 3 dB and an ER above 6 dB [33].

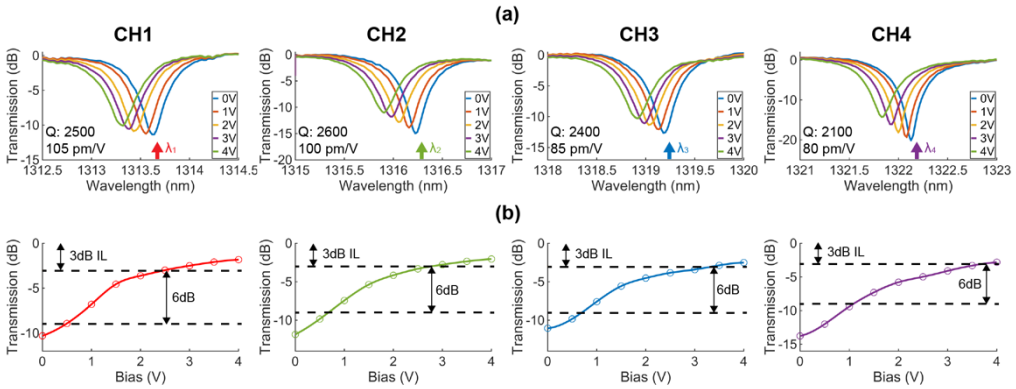

Fig. 4 (a) Normalized transmission spectra of each ITiO-gated MOSCAP Si-MRM under various gate biases. (b) E-O transfer curve at different working wavelengths for each channel, indicated with different colors, illustrating the necessary voltage swing for modulation with IL < 3 dB and ER > 6 dB.

3.2 High-speed characterization

The optical input was generated from a tunable laser and coupled into and out of the modulator array using vertical grating couplers. The RF signals were transmitted to the devices through a 50-Ω terminated probe. The E-O frequency response (S_{21}) of the fabricated ITiO-gated MOSCAP Si-MRM was measured using a vector network analyzer (VNA), revealing a 3dB bandwidth of 14 GHz, as shown in Fig. 5(a). For the characterization of data transmission, each ITiO-gated MOSCAP Si-MRM was driven by NRZ pseudorandom binary sequence (PRBS) signals generated by an arbitrary waveform generator (AWG) sequentially. The signal traversed a path including a RF amplifier (the AWG output is limit to 2V), a bias tee, and a 50-Ω terminated probe before reaching the respective device. Subsequently, the modulated optical signals were amplified by an optical fiber amplifier before being detected by a digital communication analyzer (DCA). As an illustrative example, in the characterization of CH2, the tunable laser set the optical input wavelength to 1316.29 nm, while CH2 was driven by 3 V_{pp} (0 V ~ 3 V) NRZ PRBS signals. Fig. 5(b) shows the resulting optical eye diagrams of CH2 at various data rates, with the eye diagram remaining open up to a data rate of 30 Gb/s.

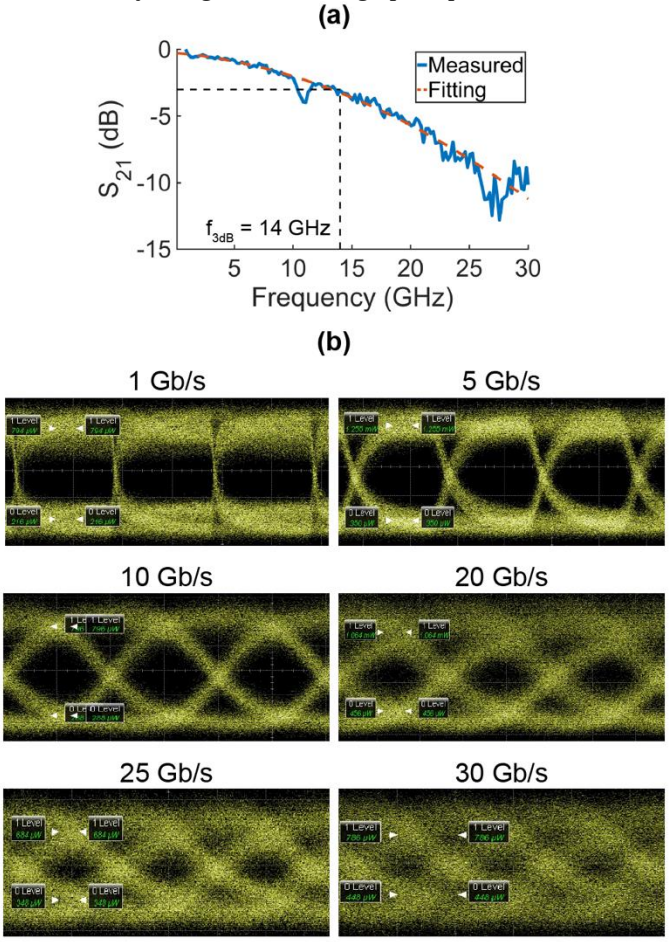

Fig. 5: (a) Measured EO response (S_{21}) showing an EO bandwidth of 14 GHz (blue solid curve). The orange dashed curve represents the fitting of the response. (b) Measured NRZ modulation eye diagrams of the ITiO-gated MOSCAP Si-MRM (CH2) under a driving voltage of 3 V_{pp} at 1316.29 nm, showcasing different data rates: 1 Gb/s (ER: 5.6 dB), 5 Gb/s (ER: 5.5 dB), 10 Gb/s (ER: 4.4 dB), 20 Gb/s (ER: 3.6 dB), 25 Gb/s (ER: 2.9 dB), 30 Gb/s (ER: 2.4 dB).

To prove the working condition with equal wavelength spacing that may be compatible with comb lasers [34], we intentionally set the optical input wavelengths at 1313.34 nm, 1316.29 nm, 1319.24 nm, and 1322.19 nm, respectively. This allowed us to thoroughly characterize each channel within the modulator array for on-chip WDM application. Fig. 6(a) shows the measured leakage current of the ITiO-gated MOSCAP Si-MRM. Within 8 V, such a device exhibited a low leakage current of less than 100 pA. However, beyond 8 V, the leakage dramatically increased, approaching breakdown, which is detrimental to device operation. Upon characterizing each channel with a 3 V_{pp} voltage swing (ranging from 0 V to 3 V) at varying wavelengths, CH2 exhibited the anticipated modulation performance at 1316.29 nm with the IL less than 3 dB and the ER exceeding 6 dB, as shown in Fig. 6(b). Conversely, under identical driving conditions, CH3 and CH4 exhibited unexpected IL values greater than 3 dB, as illustrated in Fig. 6(c). To address this issue, additional gate biases were introduced to shift the spectra, resulting in an approximate 40 pm shift for CH3 and 80 pm shifts for CH4. Subsequently, applying the gate bias effectively reduced the IL to below 3 dB while maintaining an ER greater than 6 dB. However, CH1 displayed significant resonant spectra offset, leading to modulation on the opposite side of the resonant spectra compared to other channels at the CH1 working wavelength (1313.34 nm), as shown in Fig. 6(b). While tuning with a high gate bias (around 5 V ~ 6 V) might address this issue, it would bring the device close to the breakdown voltage post-tuning. Therefore, CH1 was characterized without any gate bias tuning. Despite lacking gate bias tuning and exhibiting modulation on the opposite side of the resonant spectra compared to other channels, CH1 achieved an IL of less than 3 dB and an ER exceeding 6 dB at 1313.34 nm. Fig. 6(d) illustrates the modulation of the four channels with a 3 V_{pp} driving voltage at different working wavelengths after gate bias tuning. Three channels demonstrated clear open-eye diagrams up to a data rate of 25 Gb/s. However, despite similar expectations, CH4's open-eye diagram extended only up to 15 Gb/s. This deviation may stem from potential shortcomings in the fabrication quality of CH4. Moreover, through an optimized fabrication process, each ITiO-gated MOSCAP Si-MRM holds the potential to enhance the Q-factor and reduce the driving voltage to sub-volt levels as individual MRM [27].

The leakage current primarily determines the static power consumption associated with gate bias tuning. At low gate biases, the leakage current for the ITiO-gated MOSCAP Si-MRM is approximately 25 pA, as illustrated in Fig. 6 (a). Utilizing this leakage current alongside the E-O efficiency, we estimate a gate bias tuning power consumption of approximately 312 pW/nm. This estimation shows that achieving a total resonant wavelength shift of 120 pm in this MOSCAP Si-MRM array would require approximately 37 pW. In contrast, employing conventional thermal tuning to adjust the resonant spectra, typically operating with the power consumption of 3.1 mW/nm [35], would cost approximately 0.37 mW for the same resonant wavelength shift. Therefore, gate bias tuning offers an exceptionally efficient approach for sustaining the desired working wavelength and achieving anticipated modulation performance in on-chip WDM systems.

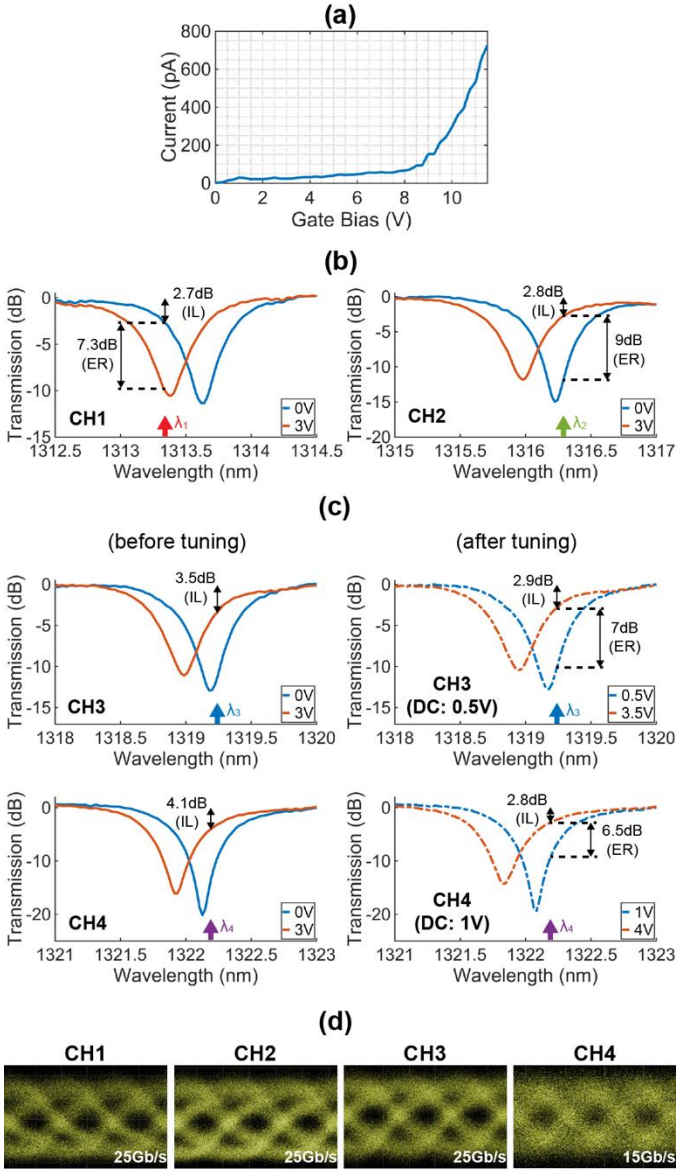

Fig. 6 (a) Measured current-voltage curve, depicting the leakage current and near breakdown voltage of the ITiO/HfO_2/Si MOSCAP. (b) Transmission spectra of CH1 and CH2, illustrating the IL and ER with a voltage swing range of 0 V to 3 V at selected working wavelengths (1313.34 nm for CH1, 1316.29 nm for CH2). (c) Transmission spectra of CH3 and CH4, showcasing the additional gate biases, shift the spectra to achieve the desired modulation performance (IL < 3 dB, ER > 6 dB) at selected working wavelengths (1319.24 nm for CH3, 1322.19 nm for CH4). (d) Measured NRZ modulation eye diagrams of each channel at selected working wavelengths after gate bias tuning.

4. Conclusion

In conclusion, this work demonstrated a 1×4 ITiO-gated MOSCAP Si-MRM array. Our experimental results highlighted a remarkable E-O efficiency $V_\pi \cdot L$ of 0.12 V·cm, showcasing the feasibility of achieving tailored modulation performance while preserving equally spaced

working wavelengths. By employing the gate bias technique to fine-tune the resonant spectra of Si-MRMs, we have achieved data rates of (3 × 25 + 1×15) Gb/s, with potential capability of reaching 4 × 25 Gb/s at a sub-volt 0.8 V_{pp}. The adoption of gate bias tuning offers significant advantages in power efficiency over traditional thermal tuning methods, particularly crucial in the realm of large-scale on-chip WDM optical interconnects.

Furthermore, this work demonstrated a co-fabrication approach by combining Intel's HVM silicon photonics process with university fabrication facility for TCO patterning, creating heterogeneously integrated silicon PIC driven by high mobility ITiO, which will enable high bandwidth density Si-PICs with better energy efficiency for future optical communication and computation systems. Although there is still significant room for optimization of the co-fabrication approach, successful demonstration of the 1 × 4 ITiO-gated Si-MRM array with capability of on-chip WDM modulation accomplished a milestone to MOSCAP-driven Si-PICs.

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Disclosures.

The authors declare no conflicts of interest.

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