8-λ × 50 Gbps/λ Heterogeneously Integrated Si-Ph DWDM Transmitter

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***Abstract*— We demonstrate a 3-D heterogeneously integrated dense wavelength-division multiplexing (DWDM) silicon-photonic transmitter simultaneously modulating eight 200-GHz spaced wavelengths at 50 Gbps/λ each, to deliver an aggregate per-fiber bandwidth of 400 Gbps. All necessary *O*-band optical components are fully integrated on the photonic integrated circuit (PIC), including an eight-wavelength laser array, a broadband semiconductor optical amplifier (SOA), and eight microring modulators (MRMs). Eight 50-Gbps non-return-to-zero (NRZ) modulator drivers, capable of delivering 2-V_{pp} modulation voltage, are integrated in a 28-nm CMOS electronic IC (EIC). The EIC also includes a thermal control unit (TCU) to align the eight MRMs to the eight laser wavelengths by appropriately tuning integrated MRM heaters. The measured energy efficiency at 50 Gb/s of the high-speed electronics, including serializer overhead, is 1.17 pJ/bit.**

***Index Terms*— CMOS, co-packaged optics, microring modulator (MRM), non-return-to-zero (NRZ), *O*-band, optical transmitter, silicon photonics, wavelength-division multiplexing (WDM).**

I. Introduction

As APPLICATIONS running in datacenters have evolved, the requirements for compute, memory, storage, and interconnect within the data center have also changed. Artificial intelligence (AI), machine learning (ML), and other high-performance computing (HPC) workloads use significantly more data per compute operation than many traditional workloads and often parallelize computation across multiple nodes. This shift—and the continued scale-out driven by increasing size and complexity of AI/ML models—has led to rethinking the way we architect datacenter systems [1], [2], [3], [4], [5]. Two key bottlenecks in existing systems are latency between compute nodes connected through hierarchical network switches and limited available per-node memory [Fig. 1(a)]. One way to improve latency is to flatten the network hierarchy by reducing or eliminating network switches [Fig. 1(b)] [2], [5]. In this way, nodes can communicate directly with each other, with a low-latency standard such as UCIe or CXL [6], [7].

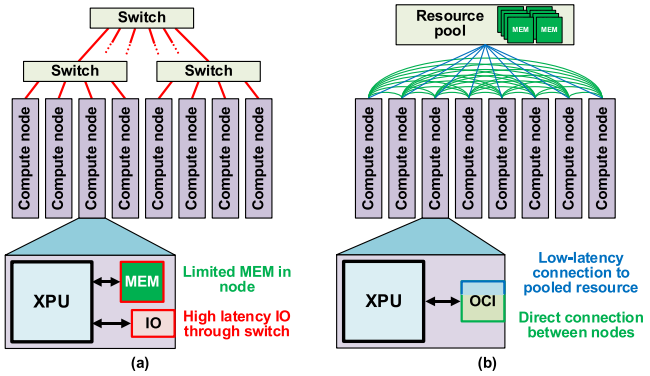

Fig. 1. (a) Typical datacenter network with hierarchical switches and (b) flattened network topology with pooled resources, enabled by OCI.

Improving per-node resource availability and overall resource utilization can be addressed by pooling the available compute, memory, and storage resources. This sharing, combined with a low-latency flexible interconnect fabric, enables optimal configuration and utilization based on specific workload demands. However, both network flattening and resource disaggregation require a high-bandwidth, low-latency, energy-efficient interconnect solution, which can also deliver the increased reach for AI/ML/HPC scale-out.

Silicon-photonic (Si-Ph) interconnect, with its reach capability (hundreds of meters over single-mode fiber), and high-bandwidth density—enabled by dense wavelength-division multiplexing (DWDM) and small fiber pitch—can enable this vision for computing that is optimized for emerging HPC workloads [2], [8]. By allowing independent modulation of many closely spaced optical wavelengths on a single fiber, DWDM provides a more energy-efficient path to scaling bandwidth density compared to all-electrical links that rely

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on increasing baud rate and/or package pin count. However, leveraging this increased bandwidth density requires transitioning from the traditional pluggable optical module form factor to optical compute interconnect (OCI), where Si-Ph transceivers [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24] are co-packaged with compute die and fiber is coupled to the package, ideally with a detachable optical cable [2]. This eliminates the bandwidth density limitation of pluggable form factor while also eliminating the need for high-speed copper-based SerDes interface between the package and the pluggable module (and the consequent power overhead).

One promising approach to realize the in-package Si-Ph transceiver necessary for OCI is a heterogeneous 3-D-integrated chiplet consisting of: 1) a silicon-photonic IC (PIC), which includes all critical DWDM optical components (multi-λ laser, optical modulators, and optical amplifier); and 2) a CMOS electronic IC (EIC) with the necessary high-speed and control electronics. Heterogeneously integrating EIC and PIC allows the EIC energy efficiency and performance to improve with CMOS process scaling while enabling photonic component enhancements over time on a stable PIC process technology. Recently, we have demonstrated key TX and RX components of such a link [25], [26]. This article expands on [25] by detailing how the system-level link loss budget informs optical TX (OTX) design specifications (Section II), providing more details of TX datapath and MRM thermal control (Section III), and 50-GBaud DWDM measurements demonstrating an aggregate data rate of 400 Gbps (Section IV).

II. O-Band Silicon-Photonic Components

Fig. 2 shows the architecture of an eight-wavelength DWDM intensity-modulated direct-detection (IMDD) optical link. An integrated multi-wavelength laser (MWL) generates eight optical carriers that are subsequently combined to feed a bank of eight cascaded microring modulators (MRMs). The MRM resonant wavelength can be electrically modulated, resulting in a consequent change in its insertion loss (IL) and thus optical intensity modulation, as shown in Fig. 2 [27]. The resonant nature of MRM enables DWDM though a simple cascading of appropriately tuned devices (without the need for explicit optical multiplexers), a key benefit of MRMs over Mach–Zehnder modulators (MZMs) [28], [29] for DWDM systems. A broadband semiconductor optical amplifier (SOA) can compensate for optical path losses to meet RX sensitivity requirements. Cascaded microring resonators (MRRs) on the RX side implement an optical demultiplexer (DEMUX), enabling separation of modulated signals on each optical carrier. At the drop port of each MRR, an integrated germanium photodiode (Ge-PD) converts the demultiplexed optical signal to a photocurrent, which is then amplified by a trans-impedance amplifier (TIA) in the EIC.

The eight TX and RX MRRs are fabricated with slightly different radii stepped by 8 nm (around a nominal radius of 6 μm). This staggers their resonances by ~200 GHz (1.15 nm) over a span that falls within the nominal ring FSR (full spectral range) of 11.3 nm. Each ring's resonance can be tuned thermally through a dedicated heater integrated in the PIC [30], [32], [33], [34], [35]. The bandwidth of this thermo-optic effect is much lower (~30 kHz) compared to the electro-optic effect used for MRM intensity modulation (~tens of gigahertz). In this prototype, we leverage the thermal tuning mechanism to maintain laser-MRM alignment (detuning) through an always-on (background) closed-loop thermal control unit (TCU) for each channel (as elaborated in Section IV).

The PIC in this work was fabricated in Intel's 300-mm hybrid silicon-photonics platform. The III–V gain medium necessary for the MWL and SOA is wafer-bonded to the rest of the silicon PIC. Next, we present a typical optical link (OTRX) loss budget, describe key O-band optical components in the PIC, and explain how these inform the specifications of the MRM driver.

A. OTRX Link Budget

The performance metrics of interest for the OTX are the optical modulation amplitude (OMA) and extinction ratio (ER) delivered with an SNR adequate for ensuring a target link bit error rate (BER) of $<10^{-12}$.

For non-return-to-zero (NRZ) transmission, OMA is the difference in optical power between "1" and "0" levels. As ER is defined to be the ratio of the power of the two levels, the following relationship exists between average optical power (P_{avg}), OMA, and ER:

$$\text{OMA} = 2P_{\text{avg}}\frac{(\text{ER}-1)}{(\text{ER}+1)}. \tag{1}$$

To determine the optical power required from the MWL source, we assume that each per-wavelength optical receiver (ORX) has −10-dBm sensitivity at 50 Gbps for a target BER of 10^{-12} [36]. Allocating 3 dB for ORX path loss (from ring DEMUX, taps, waveguide loss, and so on), we need −7-dBm/λ OMA at the ORX input. To achieve this desired ORX OMA with a reasonable P_{avg}, we target an ER >4 dB for the link [37]. Note that link ER is unchanged by optical path losses in the link, while OMA experiences the same degradation as P_{avg} [see (1)]. An ER of 4 dB and OMA sensitivity of −7 dBm/λ correspond to P_{avg} of −6.3 dBm/λ at the ORX or 2.7 dBm over eight wavelengths.

We assume that fiber coupling losses at the OTX and ORX interfaces add up to 4 dB, and an additional 3-dB loss is budgeted for losses in transmission from optical connectors in the fiber. We further allocate 6-dB IL for MRM (discussed further in Section II-B) and 1 dB for other OTX path losses. This implies that we need a laser power of 7.7 dBm/λ to close the link. While this power can be sourced by our ON-chip laser ([38], see Section II-C), it would lead to sub-optimal overall energy efficiency if the MWL were dedicated to a single 8-λ fiber. Sharing the MWL across several fibers (through broadband optical splitters) can enable MWL operation closer to peak efficiency. To make up for the consequent power loss through splitting, we use an on-chip integrated SOA [39] to boost the OMA by ~4 dB so that only 3.7 dBm/λ is needed from the laser for an 8-λ DWDM link. Section II-C discusses the laser performance and its ability to source the desired power.

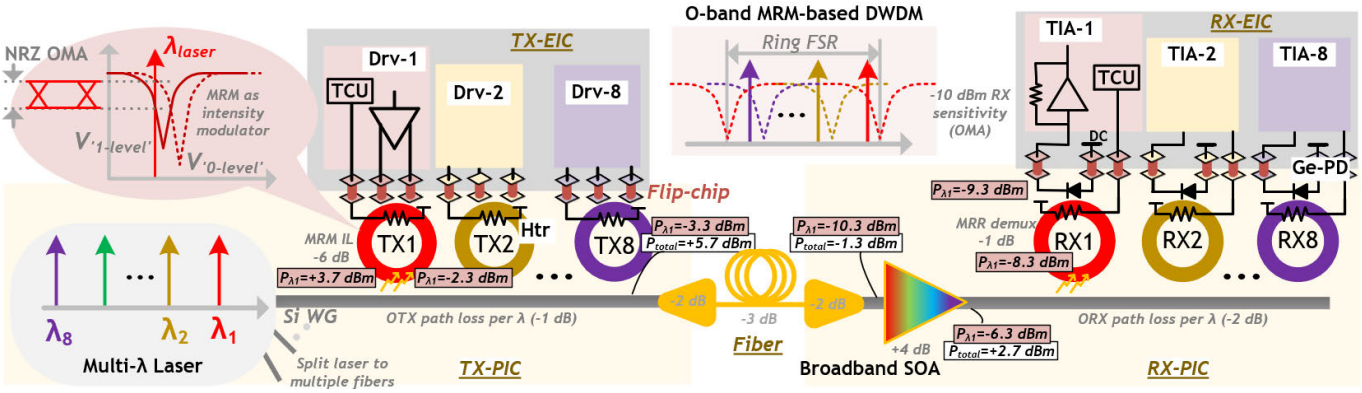

Fig. 2. Optical link-budget and resulting performance specifications on optical transmitter (OTX) for 8-λ DWDM.

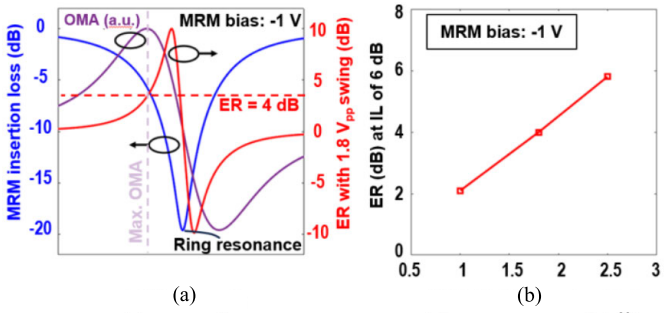

Fig. 3. (a) ER and OMA for a driver swing of 1.8 V_{pp} for different MRM ILs and a fixed reverse bias of 1 V. (b) ER available at 6-dB IL for different driver swings with a fixed reverse bias of 1 V.

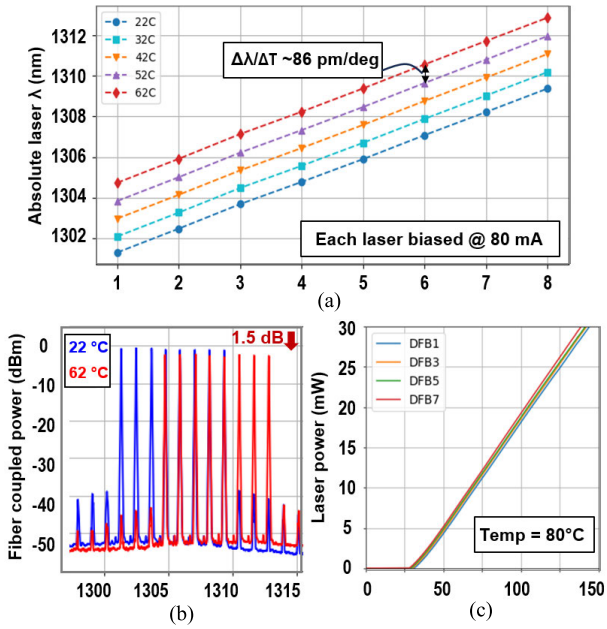

Fig. 4. MWL (a) relative spacing and (b) output power across temperature, and (c) output power versus bias current at 80 °C.

B. MRM Performance

The MRMs in the TX-PIC in Fig. 2 have a nominal radius of 6 μm and a quality factor of 4300 [40]. As described above, each MRM has a dedicated on-chip heater to tune this resonance across process and temperature variations and align it to the desired laser wavelength. MRM modulation bandwidth improves with higher reverse bias but at the cost of modulation efficiency. We choose a reverse bias of 1 V that is sufficient to deliver an E-to-O modulation bandwidth >50 GHz. This accommodates the bandwidth limitation of the EIC driver to support 50-Gbps/λ NRZ transmission. The OMA (normalized to incident laser power) and ER for a fixed electrical driver swing of 1.8 V are shown in Fig. 3(a) when the ring is biased at 1 V. An ER of 4 dB can be achieved if the MRM resonance is detuned from the incident λ_{laser} such that the IL is 6 dB, which is close to the IL for the maximal OMA condition.

Fig. 3(b) shows the ER achievable at 6-dB IL for a fixed reverse bias of 1 V for different modulation voltage swings. This indicates that >1.8 V_{pp} swing is necessary to meet the 4-dB minimum ER spec. We cover the implementation details of the electrical 50-Gbps NRZ MRM driver with 1.8-V_{pp} swing and 1-V reverse bias in 28-nm CMOS in Section III.

C. Integrated Multi-Wavelength Single-Epi DFB Laser Array

We have recently demonstrated an *O*-band MWL comprised of eight distributed-feedback (DFB) lasers with a channel spacing of ~200 GHz, integrated in a silicon-photonics platform [38]. This narrow wavelength spacing is possible by leveraging the lithography capabilities available for CMOS IC fabrication to create a high-resolution grating for the DFB laser.

Unlike coarse-WDM with larger wavelength spacing (e.g., FR4 optics), a single III–V epitaxial structure is sufficient to fabricate all eight narrowly spaced DWDM lasers, greatly simplifying the fabrication process. At 200-GHz spacing, all eight channels can be accommodated in the available 11.5-nm FSR without the need for interleaver/de-interleaver stages.

A key consideration with integrated lasers is their performance under thermal stress. Fig. 4 shows measured variation in the integrated MWL performance with temperature. All DFB lasers in the array respond similar to a temperature sweep, and the relative wavelength spacing remains constant to within 20 GHz. The absolute laser wavelength of each channel varies with temperature, as shown in Fig. 4(a). MRMs

that are near the laser also respond similar to temperature variation, though with a slightly lower thermal coefficient. This first-order thermal tracking between MWL and MRMs reduces the range of required MRM thermal tuning (and its power overhead) [8]. The continuous tracking provided by the TCU helps close any remaining gap between the ring resonance and the laser-λ to maintain constant detuning for robust link operation.

When the temperature increases from 22 °C to 62 °C, the absolute power reduces by 1.5 dB; however, the power difference between wavelengths remains less than 0.5 dB. Using an integrated laser source also eliminates an additional input fiber to the OTX and the associated coupling loss. Given the high power levels that can be generated from this laser (e.g., 13 dBm/λ at 100 mA and 80 °C), the power can be shared across eight 8-λ DWDM links using an 8 × 8 MUX/splitter [8]. The resulting absolute power after splitting can still meet the link budget discussed in Section II-A at 80 °C.

D. Semiconductor Optical Amplifier

The SOA is a broadband optical amplifier with a 3-dB bandwidth sufficient to accommodate all 8-λ channels. The SOA placement is chosen to: 1) prevent back-reflections into the integrated laser; 2) reduce the laser power incident on the MRMs to minimize ring self-heating [32]; and 3) ensure input power levels that allow SOA operation in the linear regime.

In this configuration, preserving linearity over the modulation depth is an important consideration in determining the SOA gain. Higher gain will reduce the laser power needed but compromise linearity due to gain saturation. Kumar et al. [39] reported the measured gain performance of our SOA for varying input power, and 4-dB optical power gain can be achieved with good linearity for the total SOA input power of −1.3 dBm.

Another consideration in choosing SOA gain is its noise contribution. The integrated laser has very low relative intensity noise [41], and thus, the SOA noise due to amplified spontaneous emission (ASE) is the major optical noise contributor for this OTX. The SOA output noise power spectral density (S_{ASE}) is given as

$$S_{\mathrm{ASE}}(\nu) = n_{\mathrm{sp}} \cdot (G-1) \cdot h\nu \tag{2}$$

and it increases with amplifier gain G. Here, n_{sp} is the spontaneous emission factor and $h\nu$ is the photon energy. More importantly, the SOA noise is enhanced due to beating with the total power at the receiver photodiode [42]. The receiver photocurrent ($i_{\mathrm{RX-PD}}$) can be expressed as

$$i_{\mathrm{RX-PD}} = \|E\|^2 \tag{3}$$

where E is the total incident electric field and $E = \sqrt{G}E_{\mathrm{in}}.e^{j\omega t} + E_{ASE}.e^{j\varphi(t)}$. E_{in} and E_{ASE} are the electric fields associated with the optical signal and SOA noise incident on the Ge-PD, respectively. Expanding this yields the following expression for the variance of the effective RX noise current generated due to ASE noise:

$$\sigma^2_{i,\mathrm{RX-PD}} = \underbrace{2.(R.GP_{\mathrm{in}}.L^{-1}).(R.S_{\mathrm{ASE}}.\Delta f.L^{-1})}_{\text{noise from beating term only}} \tag{4}$$

where R is the PD responsivity (0.85 A/W), P_{in} is the signal power into the SOA (−1.3 dBm), L is the loss from the SOA to the PD (3 dB), and Δf is the RX frontend bandwidth (∼25 GHz for 50 GBaud NRZ). With an SOA noise figure of 8 dB (n_{sp} ∼3.2) [39], [42] and gain (G) of 4 dB, the noise current from the SOA is 1.2 μA_{rms}. With 85-μA_{pp} signal current generated at the PD when operating at −10-dBm sensitivity limit, this magnitude of noise does not pose a significant limitation for achieving a BER of 10^{-12} for NRZ transmission [43].

III. 28-nm CMOS EIC TX Implementation

The electrical transmitter for each wavelength is designed in 28-nm CMOS to meet the swing requirements that can drive the MRM with an NRZ OMA sufficient for 10^{-12} BER signaling. In this section, we discuss the implementation of the high-speed data path and clocking (Figs. 5–7) followed by circuits for the MRM TCU (Fig. 8). On the data path, an operational and reliability concern with the ac-coupled level shifters used to drive the output stage will be discussed, and a reset circuit to address this concern is described.

A. High-Speed Signal Path and Clocking

As shown in Fig. 5, a single-ended signal path drives the anode of the MRM. The cathode is held at a constant voltage to provide the desired junction reverse bias, as well as to provide a method for measuring low-frequency MRM photocurrent, used for ring thermal tuning, discussed in Section III-B. To achieve the desired swing of 1.8 V at the MRM junction, a stacked driver operating from a 2-V supply is used. AC-coupled latches drive the high- and low-side pMOS and nMOS devices in the stacked driver with appropriately level-shifted inputs while ensuring reliability and minimizing jitter. A 4:1 serializer driven by four-phase quarter-rate clocking and data from the in-channel pattern generator provides serialized data to the full-rate data path.

A global half-rate differential clock is distributed to the eight transmitter channels. In each channel, the half-rate clock is divided (post duty-cycle correction (DCC) at half-rate) to generate four-phase quarter-rate clocks. This is followed by quarter-rate DCC and buffering to drive the 4:1 serializer. Duty-cycle and quadrature-error detection (DCD/QED) is performed near the serializer inputs to ensure optimal serializer clocking.

The 4:1 serializer [32] generates 25% duty-cycle clock pulses from the quarter-rate 50% duty-cycle clocks. The quarter-rate pulse is then multiplied with the quarter-rate data to generate full-rate high and low data pulses depending on the data value. The pulses drive the inputs of tri-state inverters that are combined to generate the full-rate data stream. A digitally tunable active inductor with three equally weighted segments is used at the output of the serializer to provide bandwidth extension. As discussed in [44], this

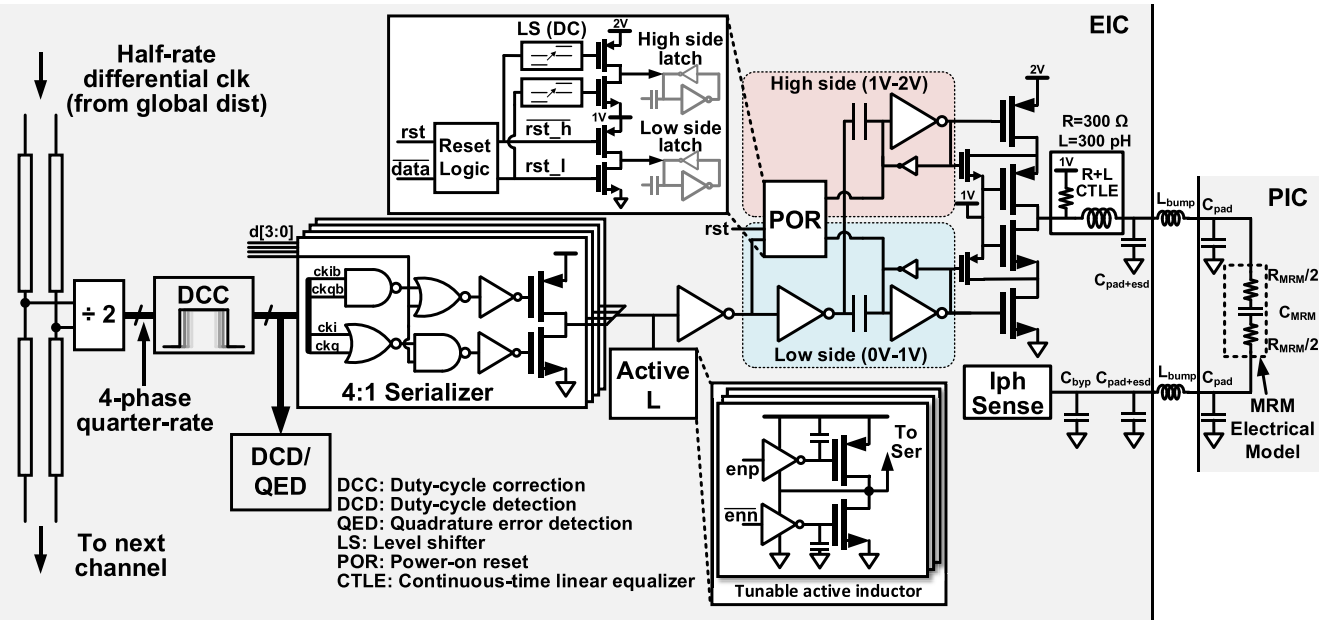

Fig. 5. Circuit implementation of stacked-driver-based 50-Gbps electrical transmitter in 28-nm CMOS.

serializer architecture provides higher speed operation than designs with transmission-gate-based multiplexer, and it is lower power than cascaded 2:1 multiplexers.

An ac-coupled latch has shown to be an effective approach to generating level-shifted high-speed data for high-swing, stacked, voltage-mode drivers. Unlike an ac-coupled level shifter with dc bias provided through a resistor [31], which introduces a low-frequency cutoff in the data path, a latch guarantees that state is maintained for data patterns with long strings of the same symbol [16], [28], [30]. However, careful design is required to ensure the latch operates reliably and maintains signal integrity. To understand the reliability concerns with an ac-coupled latch, we begin by assuming that the inverters in the latch are sized to nominally have equal nMOS and pMOS ON-resistance. Random mismatch and process variation will inevitably introduce differences in the devices. With this variation, we cannot guarantee the state of the latches in the level shifter at start-up. If either or both latch inputs after the coupling capacitors do not match the state of the data before the coupling capacitor, this can lead to improper operation of the latch and driver.

An example of the impact of such a variation at start-up on reliability is shown in Fig. 6(a). In this example, the latch input starts in a logic "1" state and the data to the input of the ac-coupling capacitor is a logic "0." When a clock waveform is sent, beginning with a 0→1 transition, initially, the latch input exceeds the supply voltage of the latch. In some cases, with repeated switching, the latch eventually settles into the desired operating region. However, in many cases, the latch input continues to exceed the supply after settling leading to reliability concerns. In these undesirable cases, the latch output also does not toggle logic state with the input and the driver does not function as desired, one example of which is shown in Fig. 6(b). Similar functionality issues to these induced by random mismatch exist for process corner variation.

To address this issue, a reset circuit is included before both latches to sense the state of the signal before the coupling capacitor and force the latch state. The tri-state inverter that performs the reset is sized just large enough to overpower the small latch feedback inverter. The high-side ac-coupled latch and the timing diagram illustrating the reset with the input data in logic "0" state and latch input starting in logic "1" state are shown in Fig. 7. The tri-state inverter on the high-voltage domain is driven by low-frequency dc-coupled level shifters (implemented with thick-gate transistors) that shift the outputs of the reset logic block.

Latch device sizing is also important to achieve the best performance. The latch device in the forward signal path is sized with the proper fan-out to drive the TX output stage. Ideally, the feedback inverter mimics a large feedback resistor for dc biasing but also provides positive feedback to maintain the proper logic state in the forward-path inverter for data content below the cutoff of the ac-coupling network. Rather than adding a large explicit resistor, the size of the feedback inverter is minimized [Fig. 6(a)]. Not only does this increase the device ON-resistance, lowering the ac coupler cutoff frequency, but it also reduces the drive strength of the feedback inverter, minimizing competition with the inverter before the ac-coupling cap.

The output driver is a stacked voltage-mode driver operating from a 2-V supply. The driver is sized to drive the capacitive load (MRM junction capacitance and parasitic capacitance of ESD diodes and pads) at greater than 50 Gbps. Passive bandwidth extension improves the eye quality at 50 Gbps and is implemented with a shunt-R, series-L output network [31].

B. Per-Channel MRM TCU

As discussed in Section II, continuous closed-loop thermal control of the ring resonators is needed to maintain constant

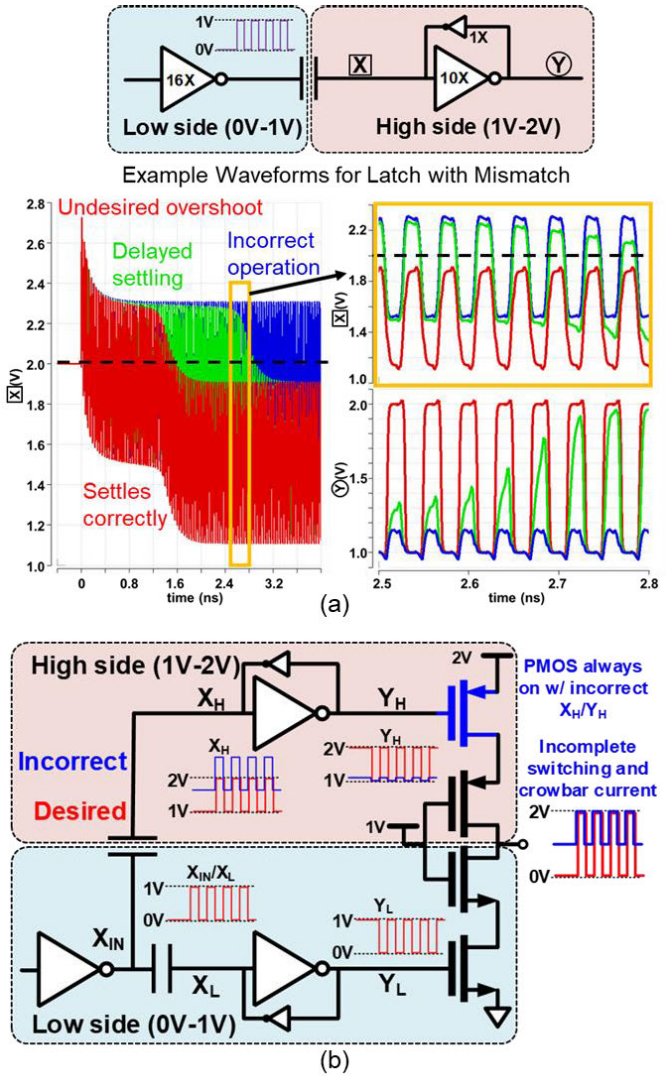

Fig. 6. (a) Single ac-coupled latch with simulated waveforms of mismatch leading to improper operation. (b) AC-coupled latches used in high-swing driver, where the improper operation of (a) leads to incorrect driver output.

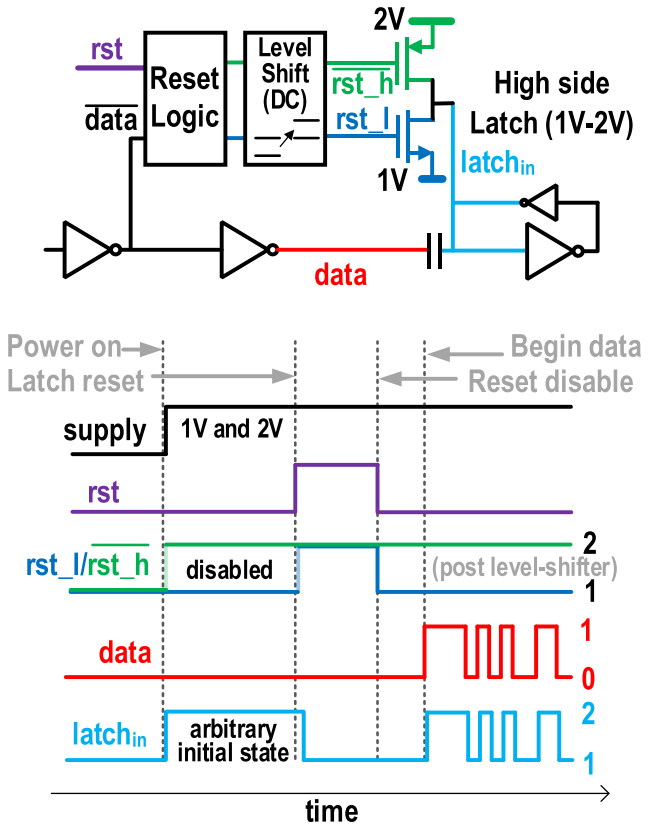

Fig. 7. AC-coupled latch with reset logic for ensuring proper logic state at start-up and timing diagram with input data in logic "0" state and latch input in logic "1" state at start-up.

detuning from the desired λ_{laser} in the presence of static process and dynamic temperature variation. We also described the resistive heater-based thermal tuning mechanism available for each MRM controlled by a dedicated TCU. Fig. 8 shows the circuit implementation of the TCU.

As in our previous work [31], we employ the photocurrent (i_{PH}) generated by the reverse-biased MRM p-n junction to estimate the IL. Each IL on the stable red-bias [32] region ($\lambda_{\text{MRM resonance}} > \lambda_{\text{laser}}$) corresponds to a unique i_{PH}. By sensing this photocurrent and tuning the ring heater to achieve the desired i_{PH} value (that maps to the target IL), we can maintain a constant IL during OTX operation.

The single-ended NRZ driver for the MRM modulates its anode, and its cathode is biased at ~2 V to establish ~1-V reverse bias. Using a thick-gate pMOS mirror to bias the cathode (from a 2.4-V supply) allows us to sense the MRM i_{PH} without any additional pads in the hybrid-integrated OTX. Two large capacitances (tens of picofarad) are included in the sensor: 1) at the MRM cathode to provide a low impedance path for modulated data and 2) a bypass cap C_{X} in the pMOS mirror to mitigate any crosstalk from other TX channels. Compared to [31], the low impedance of the cathode bias network removes the need for a large resistor to sense photocurrent, enabling a reduced cathode bias supply voltage. The photocurrent is converted to a voltage using a switched-capacitor integrator. A current scaler ensures that the sensed i_{PH} is within the dynamic range of the integrating stage. An offset current digital-to-analog converter (DAC) is also included before the integrator to subtract out MRM dark current and mismatch in the input mirror and scaler. The output of the integrating stage is digitized using a 7-b successive-approximation register (SAR) analog-to-digital converter (ADC) for processing by the digital backend. The switched-capacitor integrating amplifier is periodically reset to calibrate and subtract any temperature-dependent offset from the opamp and the SAR ADC. The clock phases for various operating phases of the integrating stage and sampling switch are shown in Fig. 8. At the end of the reset phase, the offset is digitized and stored to be subtracted from the value digitized at the end of the integrating stage. The 7-b ADC output is averaged and compared to the desired i_{PH} value. This implementation assumes a dc-balanced data input, and that the bandwidth of the TCU loop (<1 kHz) is lower than the data cutoff. The error is accumulated in a 32-b counter (loop filter) and its 14 MSBs are reduced to a 4-b pulsewidth modulated signal using a sigma-delta modulator and power DAC (PDAC). As shown previously in [31], the output current is shaped by

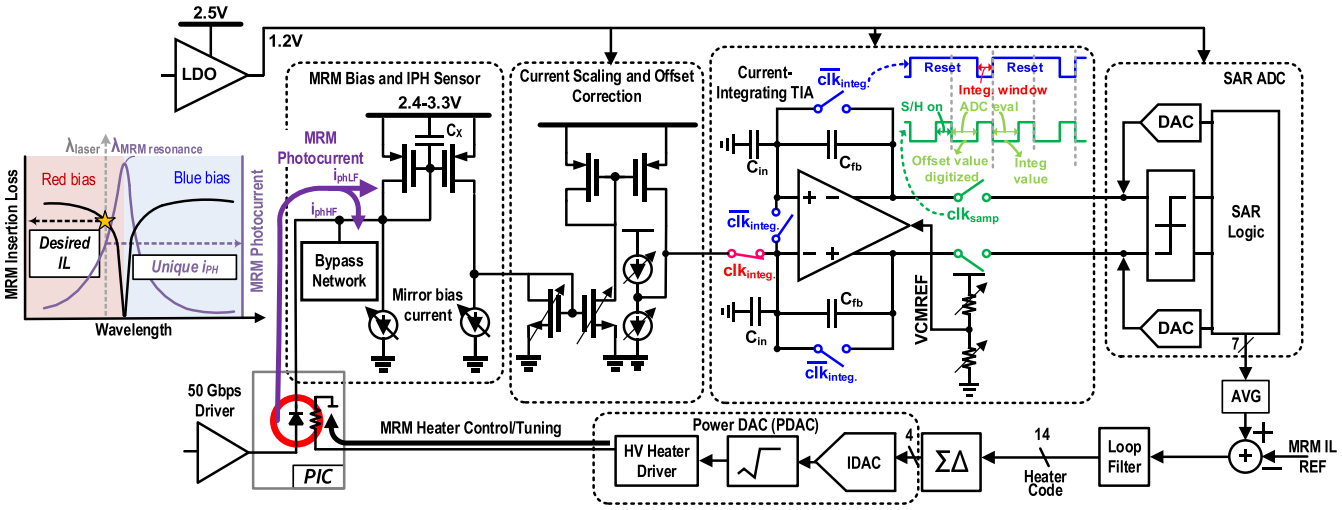

Fig. 8. Circuit implementation of CMOS-based TCU to maintain constant detuning between MRM resonance and λ_{laser}.

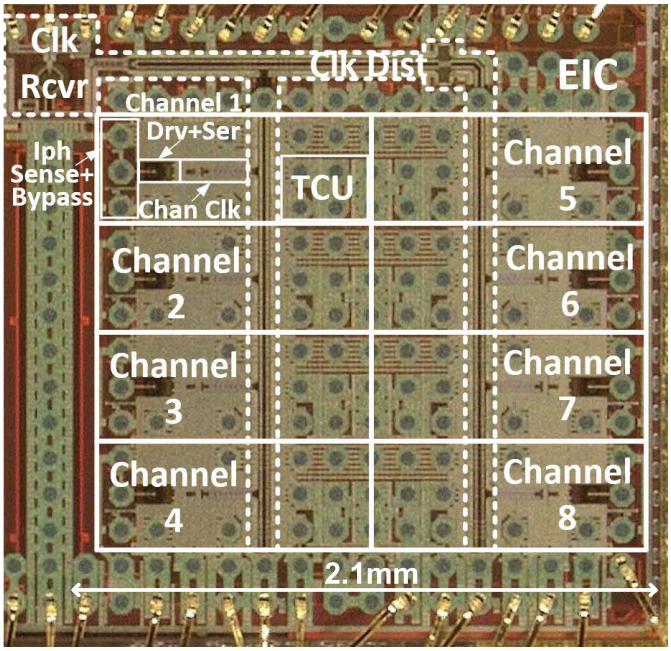

Fig. 9. Micrograph of PIC 28-nm EIC with clocking, eight TX channels, and detail of a single channel annotated.

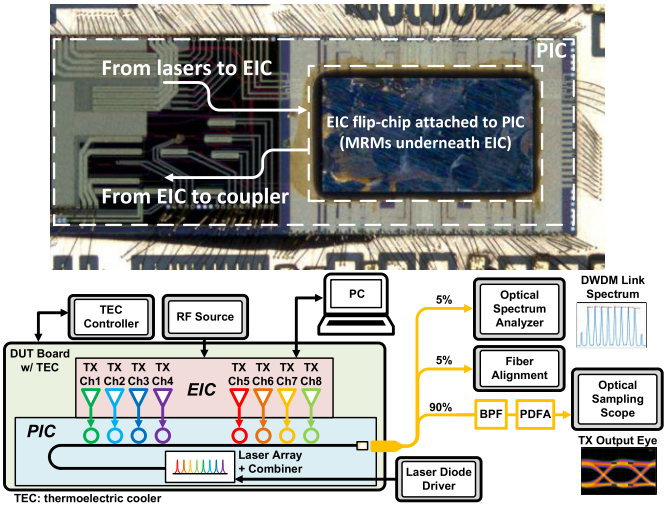

Fig. 10. Micrograph of PIC with EIC attached and optical measurement setup for the 8-λ DWDM OTX prototype.

an analog square-root compression circuit such that the output power varies linearly with heater input code. The final stage of the PDAC is a high-voltage pMOS current mirror driving the MRM heater resistor single-ended to deliver up to 50 mW.

IV. Measurements

The OCI transmitter in this work is composed of an EIC, fabricated in a 28-nm CMOS process (Fig. 9), and a PIC, fabricated in Intel's Si-Ph process, which are flip-chip bonded to each other (Fig. 10). The PIC is then attached to a printed circuit board (PCB) and wire bonds from PCB to PIC bring power, clock, and low-speed control/observability to the die complex. Metallization on the PIC distributes power and signals into the EIC. The active area for each CMOS transmitter in 28-nm CMOS is 0.25 mm^2.

The test setup is also shown in Fig. 10. A signal generator provides a half-rate clock to the EIC. Pattern generators in the TX channels of the EIC are seeded to provide uncorrelated PRBS10 patterns to each channel. An external laser diode driver biases each of the eight lasers in the DFB laser array, and each wavelength is modulated by the corresponding MRM, which is thermally tuned to align with the appropriate laser wavelength. The 8-λ DWDM signal is then free-space coupled out of the PIC. The DWDM signal is split to provide 5% power to the optical spectrum analyzer (OSA), 5% to an active fiber alignment module, and the remaining 90% for observation of the optical eye at each wavelength. A tunable optical bandpass filter (BPF) is used to separate individual wavelengths for optical eye measurement. This is used in place of the microring-resonator-based filter in the DWDM receiver, which separates wavelengths in complete link measurements [26]. The following praseodymium-doped fiber amplifier (PDFA) compensates

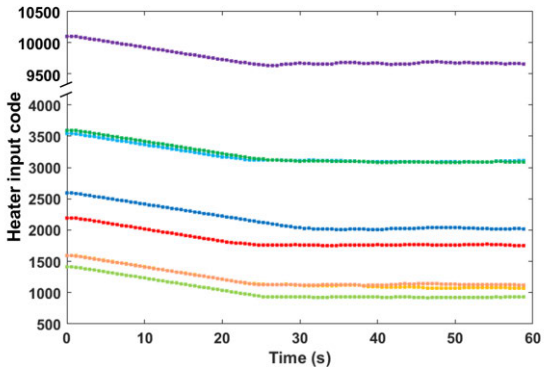

Fig. 11. 14-b heater code (power delivered to the MRM heater) converges for all eight thermal control loops running concurrently. The loop bandwidth is intentionally low to capture settling over a low-speed serial test interface.

for external coupling/component losses, amplifying the BPF output to enable eye capture by an optical sampling scope.

To verify that our thermal control scheme can successfully lock all eight MRMs to the 8-λ laser grid concurrently, we begin by running an open-loop sweep of the heater power applied to each ring. This helps determine the approximate heater power required to lock each MRM to the desired laser λ with 5-dB MRM IL. As discussed in Section II-B, this MRM IL delivers close-to-maximum OMA with >4-dB ER. Simultaneous closed-loop thermal control of all eight rings is then enabled by first initializing the PDAC driving each MRM to a value higher than the open-loop value. This ensures that each ring remains in the stable red-bias ($\lambda_{\text{MRM resonance}} > \lambda_{\text{laser}}$) region as its thermal control loop settles. All PDACs converge to values close to those expected from the initial open-loop sweep (Fig. 11), indicating that there is little interaction between the eight simultaneous thermal control loops. Note that to extract the convergence curves in Fig. 11, the eight TCU loops were intentionally slowed down to allow capture of the heater codes through a low-speed serial test interface. In normal operation, the loops converge to the desired lock point within milliseconds, indicating a loop bandwidth of hundreds of hertz.

We previously demonstrated this OTX with simultaneous 32-Gbps transmission on 8-λ for an aggregate data rate of 256 Gbps/fiber [25]. The energy efficiency was reported as 1.34 pJ/bit for an always alternating data pattern (i.e., 16-GHz clock pattern) at the electrical TX output. We have also demonstrated transceiver optical loopback measurements with the integrated ORX on the same assembly achieving a BER better than 10^{-12} for all eight channels [26]. Further measurement optimizations of the OTX described in [25] have enabled increasing per-wavelength data rate to 50 Gbps, resulting in an aggregate data rate of 400 Gbps/fiber using 8-λ DWDM. The 50-Gbps NRZ optical eyes measured using a tunable BPF when all eight laser wavelengths are simultaneously modulated by independent PRBS10 patterns are shown in Fig. 12. An ER of better than 4.5 dB is achieved for all channels. The optical spectrum captured from the OSA is shown in Fig. 13.

For DWDM transmissions, crosstalk between channels is a potential concern. Crosstalk in the OTX can occur as a result of: 1) insufficient spacing between adjacent wavelengths for a given signal bandwidth; 2) residual modulation placed on the desired channel from an adjacent TX MRM due to insufficient ring quality factor [31]; and 3) any intermodulation distortion generated by optical components in the PIC. In our previous analysis [31], we have shown that with 200-GHz wavelength spacing and an MRM quality factor of ∼5 K, crosstalk from the signal bandwidth and shape of the MRM resonance is negligible for 50-GBaud data. Our measured eye diagrams in Fig. 12, and the modulated optical spectrum in Fig. 13 also confirm that intermodulation distortion is small enough to not impact the optical TX output in all eight DWDM channels.

TABLE I
MRM-BASED Si-Ph DWDM TX WITH INTEGRATED DRIVERS

Reference	This work	[31]	[45]	[34]	[46]
# Lanes	8	4	8	4	8
Laser band	O	O	O	O	C
Per-λ Gbps	50	112	25	50	100
Per fiber Gbps	400	448	200	200	800
Mod. scheme	Low latency NRZ	PAM4	Low latency NRZ	Low latency NRZ	PAM4
Integration	Flip-chip	Wirebond	Monolithic	Wirebond	Flip-chip
EIC process	28nm CMOS	28nm CMOS	45nm SOI CMOS	N/A	22nm CMOS
Int. heater ctrl	yes	yes	yes	no	N/R
Absorbed power sense scheme	MRM iPH	MRM iPH	Drop port + MPD	N/A	N/R
Tuning range (nm)	11.5	9.3	10	9	N/R
Laser source	Integrated MWL	External tunable	External MWL	External tunable	External MWL
Demo mode	All- λ	Per- λ	All- λ	Per- λ	All- λ
Energy efficiency	2.5 pJ/b[(1)]	5.8 pJ/b[(2)]	0.8 pJ/b[(3)]	2 pJ/b[(4)]	2.2 pJ/b[(5)]
Driver swing (V)	1.8	2.5	N/R	2	3.2

MPD: Monitor photodiode; N/R: Not reported; N/A: Not applicable
[(1)] EIC+PIC [(2)] EIC datapath with clock [(3)] EIC datapath no clock [(4)] EIC datapath no clock +MRM heater [(5)] EIC datapath no clock

Table I shows a comparison of this prototype with other Si-Ph wavelength-multiplexed OTX. This prototype demonstrates a very high degree of integration comparable to [45] but avoids the additional loss associated with an input fiber through the use of an integrated multi-λ laser (MWL) array. The MWL also enables simultaneous transmission of 50 Gbps/λ on all 8-λ or 400 Gbps per fiber, which is the highest aggregate data rate demonstrated concurrently in the *O*-band. The choice of NRZ modulation and the low optical fiber dispersion in the *O*-band makes this approach particularly attractive for low-latency and energy-efficient OCIs that target AI/ML/HPC scale-out fabrics.

The measured energy efficiency for the high-speed EIC TX data path and clocking is 1.17 pJ/bit while transmitting PRBS10 patterns on each wavelength (0.56 pJ/bit for data path and 0.61 pJ/bit for clocking). This power consumption is comparable or better than other designs at similar or lower data rates [16], [45]. To understand the complete OTX energy efficiency, we must also consider the optical component power consumption. With the MRM mapping

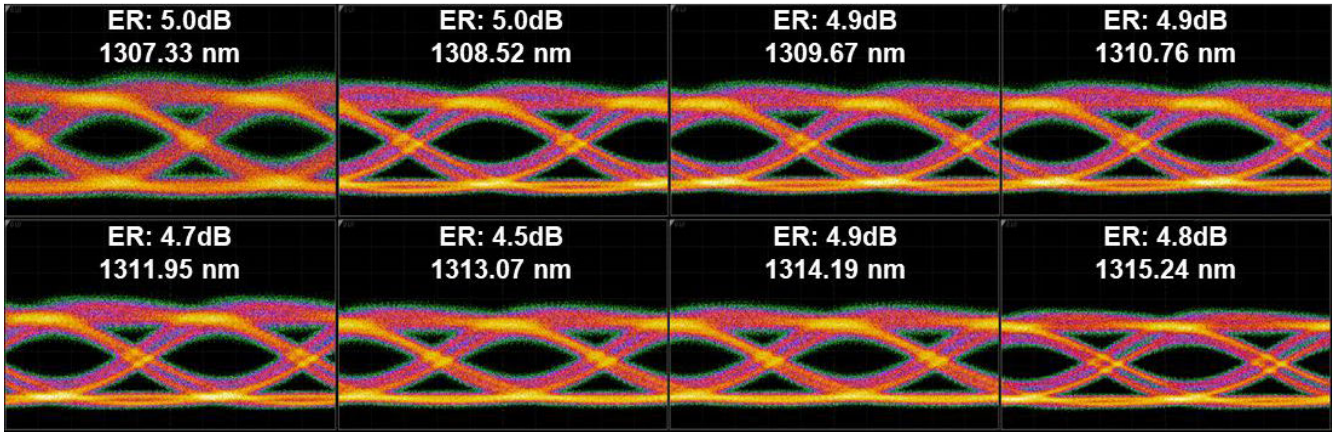

Fig. 12. 50-Gbps NRZ optical eyes for each of the simultaneously transmitted eight wavelengths.

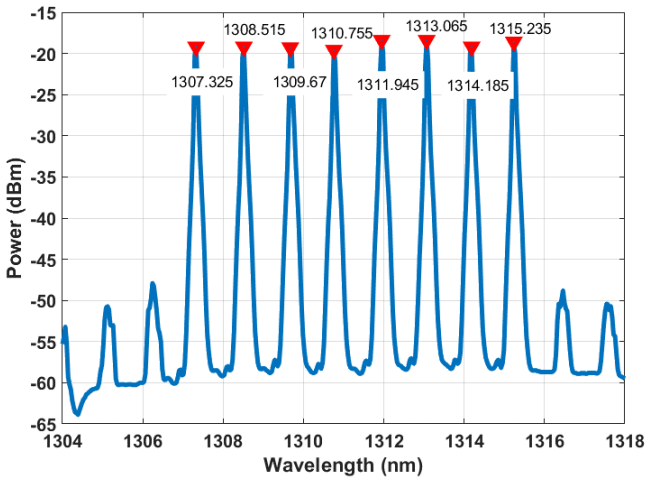

Fig. 13. Spectrum of OTX output showing all eight wavelengths simultaneously modulated.

(choice of laser wavelength modulated by each ring) used in these measurements, the average power delivered to the MRM heaters is 6.25 mW/heater. With ambient temperature variation, we expect this power to increase to track wavelength walk-off between the lasers and rings. As mentioned in Section II and described in [8], the co-integration of lasers and rings reduces this walk-off to 30 pm/°C. The SOA power (350 mW) needed to boost the OMA will be amortized over the eight wavelengths per fiber and has an energy efficiency of 0.9 pJ/b. Finally, the large laser power can be split and amortized over multiple 8-λ DWDM links (Section II). If split over eight fibers, the laser array power (8 $\times$ 100 mA $\times$ 1.45 V) can be amortized over eight OTXs, resulting in a laser energy efficiency of 0.36 pJ/b. Combined, the OTX energy efficiency at 400 Gbps is 2.5 pJ/b.

V. Conclusion

We have demonstrated a heterogeneously integrated O-band DWDM Si-Ph transmitter for low latency, long reach, and energy-efficient OCI. This OTX incorporates all critical electrical and optical components for enabling DWDM links, including an integrated O-band MWL array with 200-GHz channel spacing. The electrical data path includes an energy-efficient high-swing NRZ driver design in 28-nm CMOS, with circuitry to address reliability concerns in scaled-CMOS nodes. The CMOS IC also incorporates background thermal control tuning, critical for robust DWDM with ring resonators. Concurrent locking of all eight ring modulators is demonstrated, and our high-speed link measurements show simultaneous transmission of NRZ data on eight wavelengths at 50 Gbps/λ for an aggregate data rate of 400 Gbps on a single fiber.

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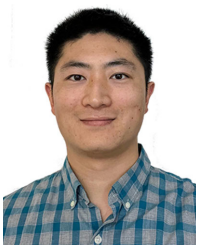

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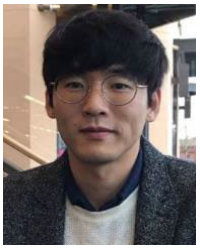

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