Advanced 3D Packaging of 3.2Tbs Optical Engine for Co-packaged Optics (CPO) in Hyperscale Data Center Networks

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Abstract—***This paper describes industry's first 3.2Tbs optical engine with integrated mux-dmux on chip, used for co-packaged optics (CPO) application for high bandwidth switch networking systems. Cisco presents an advanced 3D packaging fanout technology that integrates photonic integrated circuits (PICs) and electrical ICs (EICs), allowing for a compact design and low parasitic electrical connectivity using wafer scale redistribution layers (RDLs). The paper discusses key technical challenges, such as managing heterogeneous layouts of silicon photonics and electrical ICs, designing & fabricating RDL interconnects between various chips, ensuring a seamless input-output (I/O) interface, achieving high density Application Specific Integrated Circuit (ASIC) connectivity, and enabling high channel density die-edge fiber array coupling. We will delve into the integration of packaging design, optimization of signal integrity, development of assembly processes, and control of warpage through different interconnect bonding methods, all of which culminated in a successful co-packaged optics switch system demonstration. This paper presents a reworkable approach for assembling multiple, high bandwidth optical engines on a large body organic substrate, as well as managing large body package warpage and surface mount assembly issues.***

Keywords—Silicon photonic, co-package optics, large package body, Heterogenous integration

I. INTRODUCTION

As the usage of high bandwidth applications such as AI/ML, high quality video streaming, and virtual reality continues to grow, the pressure on data center networks also increases. These ever-increasing demands for more bandwidth lead to the development of faster and more efficient optical interconnects and ASICs. The combined data throughput of switch ASICs and optical devices is doubling roughly every two to three years [1], resulting in both increased speed and power consumption for the host device's pluggable optics electrical interface.

Large interconnect distances between ASIC and Optical modules typically lead to higher channel insertion losses, which in turn require higher power Serializer-Deserializer (Serdes) to close the high-speed channel link. This high power Serdes, coupled with the need for higher power Digital Signal Processors (DSPs) in optical modules, contribute to a large portion of total switch system power [1, 8]. One approach to reduce the increasing power requirements is to bring the Optics and ASICs closer to each other, thus enabling either direct drive or low power Serdes options to drive high speed signals between the ASIC and Optics. Fig.1 depicts various architectural choices available for reducing power consumption between ASICs & optical module interfaces. Most promising solutions for power optimization involve using Co-packaged Optics (CPO) or Near Package Optics (NPO), that allow for low loss, low power Serdes options to be used and eliminating need for Optical DSPs, thus minimizing overall system power and cost [1].

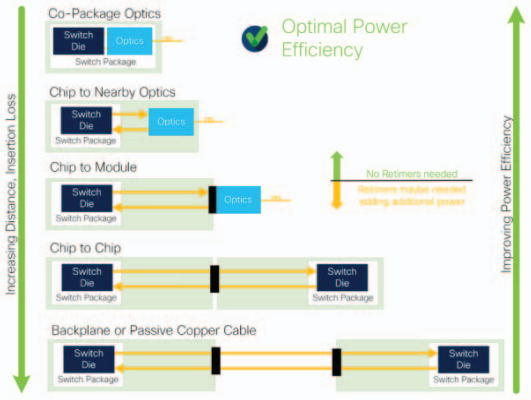

Figure 1 Switch system power optimization by reducing interconnect distances between ASIC and Optical modules.

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Silicon photonics technology offers key building blocks to enable next generation optical interconnects that meet challenging cost/bit and power/bit requirements. Advanced photonics packaging architectures and assembly techniques enable low loss, low power, and reliable optical interconnects for next generation switch and router networking systems [2]. 3D stacking of dies is a critical technology that can help resolve bottlenecks for power delivery, signal integrity, and form factor reduction as well as efficient thermal dissipation. In this paper, we will discuss an advanced 3D fan-out package-on-package technology that enables multi-chip electronic-photonic integration using fine pitch and small fine-line width copper redistribution layers (RDLs). We will discuss associated challenges with design, fabrication, and assembly of such a system along with appropriate risk mitigation steps.

II. Optical Engine

A. Photnics Packaging architecture

Silicon photonics based optical transceiver architecture offers advantages such as high data transmission rates, lower power consumption, and compatibility with existing silicon manufacturing process, making it suitable for applications in data centers, telecommunications, and high-performance computing.

For co-packaging, various packaging approaches were considered as shown below in Fig. 2 below. Co-packaging requires miniaturization and integration of mutliple optical and electrical components within a compact form factor. Wirebonding option as shown in Fig. 2(a) limits the achievable packaging density and integration level due to the space required for wire routing and clearance. Additionally, wirebonds introduce parasitic capacitance and inductance, which can degrade the signal integrity and limit the achievable data rates. On the other hand, a multi-chip integration model shown in Fig. 2(b) tends to introduce additional interconnects and signal paths, leading to increased signal propagation delays. It's a simpler assembly option but may not be scalable due to constraints related to interconnect density, thermal management and reliablity. Fig. 2(c) fan out package on package (FPOP) allows integration of multiple chips within a single package, allowing for shorter incterconnect lengths between optical and electrical ICs (EICs). The compact form factor also improves thermal management. The vias act as channels for efficient heat dissipation coupled with a top heat spreader over the photonics IC (PIC). This packaging architecture offers better routing options enabling efficient multi-chip design integration. It is highly scalable and can accommodate a wide range of chip sizes and configurations.

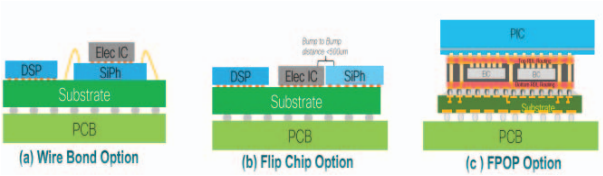

Figure 2 Various optical engine architecture options for Co-Packaged Optics

Redistribution layers on the top and bottom sides enable the best option for circuit routing of the driver (EIC) to optical modulator (PIC), transimpedance amplifier (TIA), and the photodetector (PIC). The high speed I/O, power/ground, and sense/control interconnects are best routed through the backside redistribution layers rather than on silicon photonic metal layers as the RDL dielectric offers shorter channels, lower IR drop and superior signal isolation properties compared to silicon.

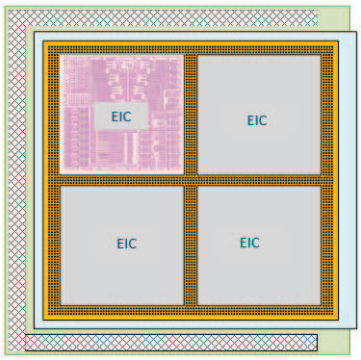

Figure 3 Top view of the Optical Engine fan-out package depicting 4x EICs packaged with 1x PIC & substrate.

To reach 3.2 Tb aggregate bandwidth per optical engine, we integrated four 800G EICs along with a 3.2T PIC in the FPOP package, thus dividing the overall layout into 4 identical quadrants, as shown in Fig. 3 above. Each quadrant contains a single 800G EIC electrically connected to other EICs using RDL interconnects. Correspondingly the PIC layout was divided into four quadrants with each 800G FR4 optical channels connected to each 800G EIC.

The PIC was flip chipped on top of the fanout package after bumping. An overhang for the PIC over the substrate allowed for attachment of a large channel fiber array unit (FAU) using die-edge optical coupling. Top-side redistribution layers in the fanout package connected the EICs to the PIC bumps. Tall copper pillars around and between the EICs connected the top-side RDLs to the bottom-side RDL layers and C4 bumps.

The optical engine package was flip chipped on an organic substrate. This was one of the key steps to maintain the warpage and stress of the assembled package - not just for enabling downstream fiber coupling but for optical engine reliability as well. Several methods to reduce the warpage were utilized, including optimizing metal density in redistribution layers, tall copper pillar density, package thickness and material selection. The right substrate stack-up and core materials were chosen to minimize coefficient of thermal expansion (CTE) differences between the substrate and the fan out package.

To validate the integrity of multiple interconnects in the fanout package, various daisy chains were added to different locations throughout the package and tested at different stages of assembly. Daisy chains between EIC and RDL were tested on the top-side RDL before PIC flip chip assembly, while daisy chains between PIC and bottom RDL were tested by probing C4

bump locations to validate the full package integrity before attaching on the substrate.

B. Simulations

The FPOP package consisted of various components (EIC, the PIC and the RDL package) using different fabrication technologies. Each component was laid out and validated individually using the verification flow for that technology node.

Co-packaging of the silicon and optical ICs allow for much shorter and higher density electrical lines than on-board optical modules. An array of bump and RDL interconnects are shown in Fig. 4 below for the fanout optical engine package.

For CPO, the losses and crosstalk that happen in the package are as important as the losses and crosstalk that happen in the external channel [3]. Due to this, it is important to design a package/channel interface that meets the required signal integrity (SI) specification to guarantee a high speed, low error rate transmission [4]. In the case of the fanout package with 4 EICs in 4 quadrants, signal integrity simulation was carried out on each quadrant.

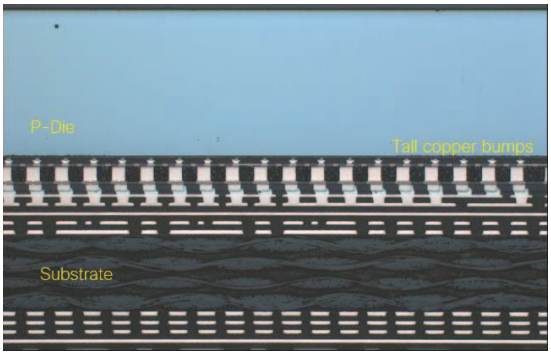

Figure 4 Cross -section of assembled fanout package on package with 2 sided RDL (on top and bottom of EIC)

We compared the options shown in Fig. 2(a) and 2(c) above for signal integrity. Fig 2(c) based fanout package option simulated a differential pair 600um long from the EIC bump to the tall pillar on top-side RDL, the tall pillar itself, the bottom RDL interconnects and C4 bumps. In the wire-bond version we included a differential pair 1.7 mm long on the PIC metal layers from EIC bump to the wire-bond pad and 1.2 mm long wire-bond with 0.8 mil diameter. Substrate was not included in the simulation as we wanted to isolate the optical engine package performance itself. Insertion loss and return loss results from the simulation are shown in Fig. 5(a) for FPOP and 5(b) for the wire-bond package option below. Multiple channels performances were simulated and overlapped.

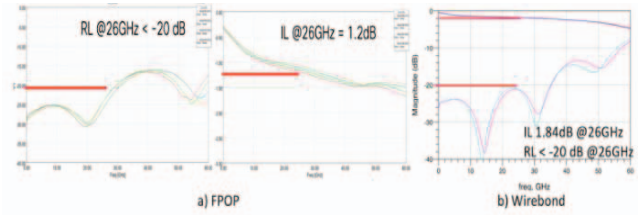

Figure 5 Insertion and return loss simulation results for (a) FPOP and (b) wire bond photonics package option.

Insertion loss at 26 GHz improves as expected from 1.84 dB to 1.2 dB for the fanout package, while return losses are < -20 dB in both cases. This margin helps improve overall signal integrity for the ASIC interconnect channels.

We then included the substrate and the land grid array (LGA) pads of the socket as part of the simulation. Simulation results are shown in Fig 6 below. We observed an increase in return loss at the LGA pads (from -20 dB to -15 dB) and a slight increase of the insertion loss (1.5 dB from 1.2 dB).

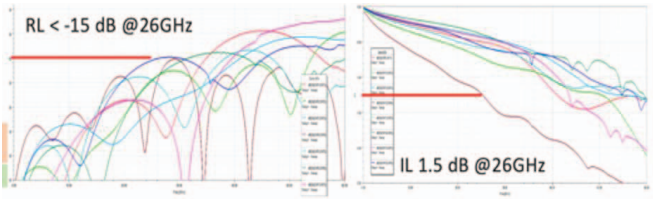

Figure 6 Return and insertion loss simulations for the FPOP option including organic substrate.

At the end, we included in the model the ASIC substrate with the longest path from optical engine package to the ASIC (50 mm). Results are shown in Fig. 7 below. Return losses were still below -14 dB while insertion loss increased to 7 dB. We verified that the worst channel still performs well when used in conjunction with Feed-Forward Equalization (FFE) taps used in the ASIC design for improving signal quality at the receiver.

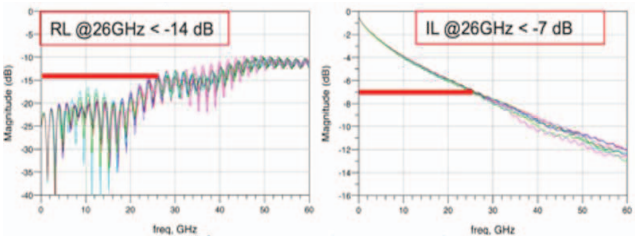

Figure 7 Return and insertion loss simulation results for FPOP Optical Engine co-packaged on ASIC substrate

C. Photonics packaging challenges and solutions

Silicon photonics fabrication leveraged Cisco's standard photonics platform technology using mature and reliable optical design elements (high-speed photodetectors, integrated MUX/DMUX on chip, high-speed modulators) through foundry partners.

The assembly flow for fanout package on package involved precision manufacturing steps to integrate multiple electrical IC's (4x) within a compact fanout package. Residual stress developed during the wafer level molding and redistribution layer steps in package may result in bump joint cracking along the high stress regions of the package (along the corner and edges), while at the center of the package solder squeeze out was observed at the PIC to fan out package interconnect joint. At the fanout package to organic substrate interface, misalignment and solder joint cracking could be observed, as shown in the cross-sectional image in Fig. 8 below. Various mitigation steps were adopted during the design and assembly processes to reduce the impact of package stress – including optimizing mold thickness of the fanout wafer, optimizing fanout package thickness, addition of back-side stress layers on the PIC as well as thermo-compression bonding techniques. The mold to die volume ratio, as well as tall copper pillar density, are also critical in managing the overall warpage of the fan out package.

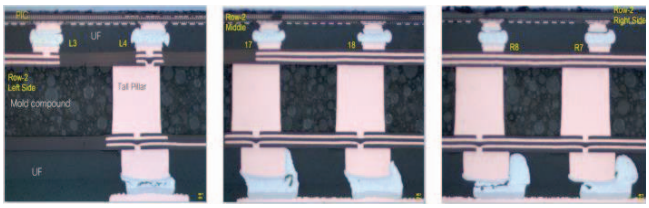

Figure 8 Cross-section of bump joints showing top-side RDL, mold compound, tall cu pillars, and bottom-side RDL to organic substrate.

The fanout package on package also had a heat spreader on top of the PIC, that further enabled flattening the package and reducing overall package warpage as shown in Fig.9 below. This was critical for low-loss, die-edge optical alignment.

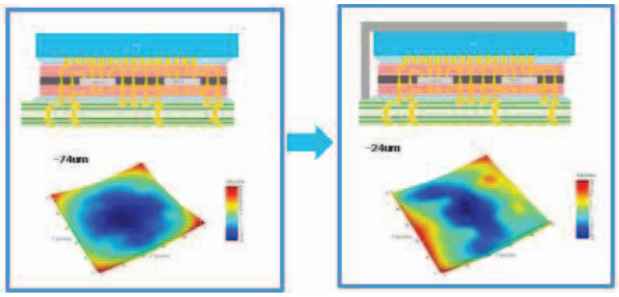

Figure 9 Thermo moire data showing reduced warpage profile (by 50-100um) by using heat spreader in package.

D. Optical Alignment challenges and solutions

Optical fiber coupling to silicon photonics chips is a critical process step required to enable low loss optical transmit and receive channels for the optical transceiver. With increasing number of optical channels required for successive generations of optical modules, alignment of large channel count Fiber Array Units (FAUs) to PIC waveguides becomes challenging. Edge coupling especially is susceptible to small changes in die edge warpage in the waveguide facet region (<1um coplanarity is typically required along the die edge) along with pristine diced edge quality (<5-10um chipping size required) [6]

Optical fiber alignment is especially challenging for co-packaged optics, owing to use of high channel count fiber arrays (~24-80) and sensitivity to small changes in PIC warpage across a large die area. Optical Fiber Arrays typically do not withstand typical flip chip assembly reflow temperatures - hence the optical coupling of fiber arrays needs to be performed post-chip bonding operations. If optical fiber attach is performed after ASIC and Optical Engine assembly, the resulting warpage of the optical package, and specifically the PIC, will pose challenges during fiber alignment. For Cisco's 3.2T Optical Engine assembly, optical fiber coupling using a 24-channel FAU were performed post-chip assembly with <1.5dB per channel optical loss. Fig. 10 below shows the final 3.2T optical engine assembly including heat spreader and attached 24-channel optical fiber array.

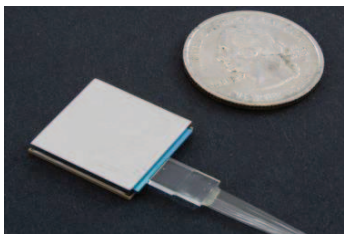

Figure 10 3.2T Optical Engine with 24-channel FAU attached.

III. OPTICAL ENGINE INTEGRATION WITH LARGE BODY SWITCH ASIC PACKAGE

For building a CPO switch system, a 110x110mm^2 low-loss organic ball grid array (BGA) substrate was used to integrate a 25.6T ASIC silicon die assembly along with 8x optical engines using high-speed channel links routed on top layers of the substrate. Fig. 11 shows image of an ASIC package using large body substrate with a metal frame attached. The 110x110mm^2 packaged device used a custom metal frame design that is used for optical engine socketing as well as package warpage control. Optical engine socketing assembly was used to provide a pluggable and serviceable solution for optical engine integration during assembly and field use. In this approach, the optical engines device would not be directly attached to the substrate via traditional Mass Reflow (MR) or Thermal Compression Bonding (TCB) process, but the connectivity was made possible with the use of a custom-

designed uLGA socket design. This would require a novel approach to attach the optical engine onto a large body size substrate since the design and process tolerances were very tight. The custom designed metal frame has features to guide and align the custom uLGA socket to ensure high-speed connectivity between the optical engines and the organic substrate upon optical engine insertion.

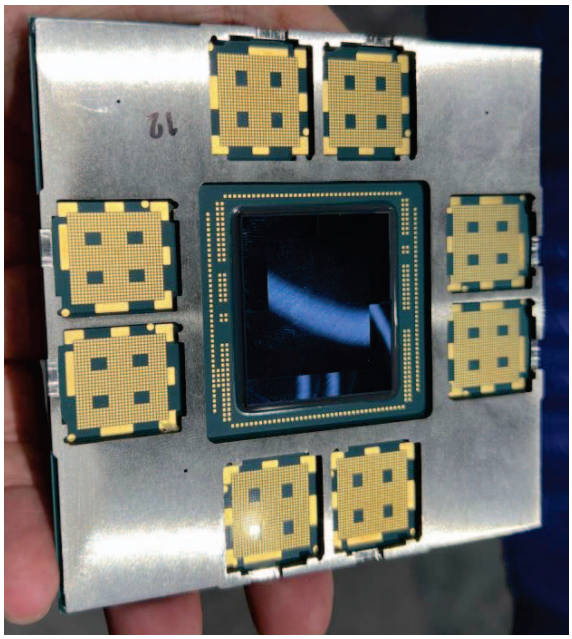

Figure 11 ASIC large body substrate package including metal frame with pockets for optical engine socketing.

One of the most challenging problems in working with a very large body size package is high warpage during assembly. Warpage is derived from CTE mismatch between large organic substrate and bonded silicon die during packaging assembly processes. Warpage has big impacts on board mount manufacturing processes and reliability. The custom designed metal frame was used to facilitate the optical engine alignment registration while also reducing large body package warpage, especially during high temperature surface mount processes – by using non-traditional metal alloys, custom thickness & tolerance control and various other design features.

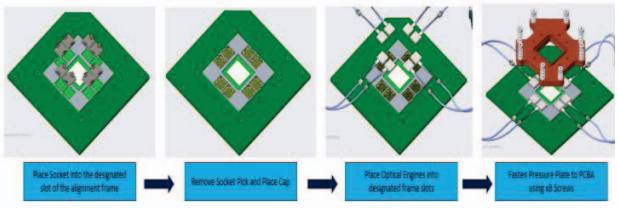

Figure 12 Assembly sequence of the socketed solution for Optical Engine to CPO package

Fig. 12 above shows an assembly sequence used for socketing 8x optical engines on a large body CPO package. A comprehensive study covering jig design, material selection and adhesive analysis led to the establishment of a process flow meeting alignment and tolerance specifications. Through optimization of pad overlap area, socket pin deflection and pressure plate design, we were able to achieve a reliable, high-speed, low loss electrical connectivity between the ASIC and optical engines.

Fig. 13 below shows the overall interconnection scheme for the final assembled CPO system. CPO implementation involved system scale integration of various components – including Optical Engines, ASIC package, fiber arrays, large body substrates, uLGA socket, power management components, thermal assembly as well as routed fiber assembly management.

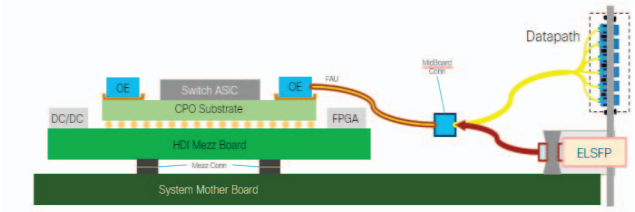

Figure 13 Architecture of a 25.6T CPO system using 3.2T Optical Engines

We used an external pluggable laser source [9] that provided optical power at low loss to the optical engine modules via polarization maintaining optical fibers (PMF). The final CPO system assembly is shown in Fig. 14 below. We were able to demonstrate total system power consumption comparing a traditional 25.6T Switch system versus a 25.6T CPO based system, using the same ASIC and other power components running PRBS31 traffic across all ports. Using this setup, we were able to demonstrate up to 25% power savings using 100G-PAM4 links with Bit-error rate (BER) and packet losses well within IEEE specs [8].

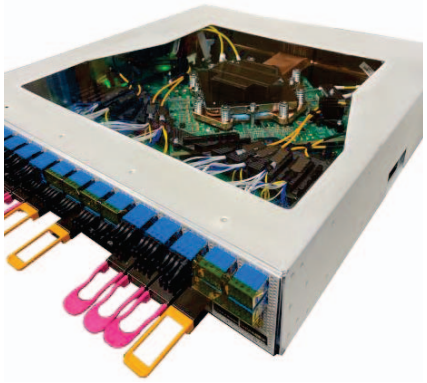

Figure 14 Cisco's 25.6T CPO system demonstration in OFC 2023

IV. CONCLUSION

This paper discussed the escalating demands on data center networks due to high bandwidth applications like AI/ML and

virtual reality, driving the need for faster and more efficient optics and ASICs. Co-packaged optics offer lower power solutions, critical for reducing overall system power. We discussed the design, development, and assembly of a 3.2T (4x800G) Optical Engine with integrated MUX-DMUX on chip, that was used in the successful demonstration of a 25.6T Co-Packaged optics switch system highlighting significant reduction in overall system power.

The Optical Engine design and packaging utilized advanced 3D Fan-Out packaging techniques used to integrate up to 4x800G Electrical ICs together with two-sided redistribution layers along with a 3.2T Photonics IC that was able to meet critical electrical and optical performance specs. 3D die stacking technologies will be critical for development of next generation, high bandwidth, high density optical engines for hyperscale networking and data center applications.

V. ACKNOWLEDGMENT

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