A Sub-500fJ/bit 3D Direct Bond Silicon Photonic Transceiver in 12nm FinFET

Po-Hsuan Chang*[1], Anirban Samanta*[2], Peng Yan[1], Mingye Fu[2], Yu Zhang[2], Mehmet Berkay On[2], Ankur Kumar[1], Hyungryul Kang[1], Il-Min Yi[1], Dedeepya Annabattuni[1], David Scott[3], Robert Patti[4], Yang-Hang Fan[1], Yuanming Zhu[1], S. J. Ben Yoo[2], and Samuel Palermo[1]

[1]Texas A&M University, College Station, TX, [2]University of California, Davis, Davis, CA, [3]Optelligent, Costa Mesa, CA, [4]Nhanced Semiconductors, Batavia, IL, pchang0628@tamu.edu, *These authors contribute equally

Abstract

This paper presents an energy-efficient electronic-photonic co-designed transceiver heterogeneously 3D-integrated with high-density, low-parasitic direct bond interconnect (DBI®) featuring 32-channel silicon photonic microdisk modulator/filter based optical transceivers in 12nm FinFET for wavelength division multiplexing (WDM). The transmitter has $1.2V_{ppd}$ electrical modulation swing and 7dB extinction ratio. The receiver achieves an OMA sensitivity of -18.82dBm at 18Gb/s. The transceiver pair at 18Gb/s achieves 496fJ/bit energy efficiency. The receiver can further operate at 25Gb/s with -16.9dBm OMA and 227fJ/bit efficiency.

Introduction

Silicon photonic (SiP) wavelength-division multiplexing (WDM), driven by the demand for bandwidth capacity of optical link, allows multiple wavelength interconnect via a single fiber/waveguide. Microdisk resonator, with its compact footprint and high *Q* factor, is a competitive candidate for WDM with multiple microdisk modulators and filters integrated onto a single waveguide with high density. The direct bond interconnect (DBI®), a 3D direct bond technology that directly merges the top metal and dielectric of two wafers, has the potential advantage in terms of bandwidth, OMA sensitivity, and power efficiency realized by its high pad density, low-parasitic 3D integration. This paper is a significantly improved demonstration and analysis of [1] and presents a sub-500fJ/bit 12nm FinFET optical transceiver that is co-designed with microdisk resonators and co-optimized with direct bond interconnect at the pitch of 20um to enable 32-channel energy efficient optical interconnects on a compact chip footprint with significantly improved OMA sensitivity.

Transceiver Architecture

Fig. 1 shows the optical transceiver circuit schematics. The optical transmitter, shown on the left side, begins with an 8-to-4 serializer driven by a 1/8-rate clock divided from 4-phase quarter-rate clocks. The injection-locked oscillator (ILO) generates 4 quadrature-spaced quarter-rate clocks that are phase and duty cycle calibrated via quadrature error correction (QEC) and duty cycle correction (DCC) circuits to ensure uniform eye width at the TX output. The DFF-based retimer and NAND/NOR based dynamic tri-state logic generates 1UI data bits that control 4 high impedance MUX segments for 4-to-1 serialization without the need for clocks beyond quarter-rate. The serialized full-rate data is buffered by parallel inverter chains to differentially drive the output. An on-chip bias-tee defines the common mode of the $1.2V_{ppd}$ output electrical swing and ensures the depletion mode modulator's PN junction is reverse-biased driven with optimal bandwidth. The 8-bit parallel input can be multiplexed between 8-bit outputs from a FIFO from electrical interface receivers or an on-chip PRBS-15 generator or programmed as 8-bit clock pattern to serve as a forwarded-clock channel.

The optical receiver, shown on the right side of Fig. 1, has a transimpedance amplifier (TIA) front-end co-designed with 3D direct bond packaging for optimal OMA sensitivity and bandwidth. The TIA includes programmable inverter-based active inductor banks to calibrate for the input node bandwidth variations. A current-mode OTA-based offset calibration loop optimizes the sampler's input common mode, which is affected by the input optical swing. The bandwidth is further optimized by a shunted inverter-based active inductance prior to the sampler. The 4 low-voltage quarter-rate samplers, driven by the per-channel ILO with clock deskew capability, output the 4-bit sampled data that is further deserialized into 8-bit parallel data. The forward clock receiver has an identical analog front-end, but with single-to-differential conversion circuit replacing the sampler and deserializer to drive the clock distribution network.

As shown in the Fig. 2 EIC micrograph, the EIC receives parallel 8-bit 1/8 rate data from FPGA/GPU/ASIC via electrical receiver (ERX). A group of 8 optical transmitters (OTX) serialize the parallel data into full-rate data stream and modulates the laser via microdisk modulator. A group of 8 optical receivers (ORX) deserialize the received optical data back to 1/8 rate parallel 8-bits and send the data to a group of 8 electrical transmitters (ETX) and interface with external FPGA/GPU/ASIC. An on-chip PLL supplies the quarter-rate differential clock to all the optical transmitters and electrical receivers. The 32 optical transmitters are arranged into 4 groups. Each group, with 8 channels, are bundle-clocked by an ILO. The electrical receiver has a full-rate phase interpolator-based CDR, continuous-time linear equalizer (CTLE) front-end with 4.5dB peaking, and directly receives the quarter-rate clock from the distribution network. The 31 optical data receivers are clocked by the distribution network launched from the forward optical clock receiver channel. The electrical transmitters are direct source-series termination (SST) drivers that require no clocking. The SST drivers are designed to bridge with the low-voltage differential signaling (LVDS) termination of FPGA.

Experimental Results

The 12nm EIC micrograph is shown in the left of Fig. 3 with 32-channel optical and electrical transceivers labelled. The layout dimension of single optical transmitter and receiver are 67um by 20um and 80um by 20um, respectively. The 3D direct-bond scheme via DBI and the final packaged, fiber aligned and attached transceiver module are shown on the right side of Fig. 2. The 12Gb/s and 18Gb/s transmitter optical eye is shown on the left side of Fig. 3. The ISI seen on the 18Gb/s eye is due to the parasitic resistance between microdisk modulator's PN junction and the resonance wavelength tuning p-doped diffusion resistor that induces leakage current path, causing IR-drop across the TX output driver's bias-tee resistor and offsets the reverse bias modulation into forward bias region. An equivalent model based on the device layout of [2] and the simulated bandwidth-limited eye diagram which overlaps on the measure 18Gb/s eye are also shown on the left of Fig. 3. The right side of Fig.3 shows the optical RX timing

margin and OMA sensitivity measurements. At 12Gb/s, the OMA sensitivity is -20.3dBm and the timing margin is 12% UI and with -18.82dBm and 5.4% UI at 18Gb/s. The RX power efficiency at 18Gb/s is 339fJ/bit. The RX can operate at 25Gb/s achieving -16.9dBm OMA sensitivity, 6.7% UI, 227fJ/bit power efficiency and 94fJ/bit when excluding the per-channel injection-locked oscillator power consumption. The left of Fig. 4 shows the power breakdown of just the transceiver circuitry and the estimated overall optical interconnect system efficiency. The transceiver circuitry energy efficiency at 18Gb/s is 496fJ/bit. The overall link efficiency at 18Gb/s, including the microdisk resonance tuning power and laser power due to the package/PIC correlated -19.8dB optical loss contributes from the microdisk through/insertion loss, the PIC edge coupler loss, waveguide loss, the 3dB system power margin, and the estimated 30% laser wall-plug efficiency, is 1.261pJ/bit. The right of Fig.5 shows the comparison tables with prior arts and summarize the transceiver performance at both 18Gb/s and 25Gb/s.

Reference

[1] A. Samanta, *OFC*, 2023 [2] E. Timurdogan, *CLEO*, 2013. [3] J. F. Buckwalter, *JSSC,* 2012, pp.1309. [4] C. Li, *JSSC,* 2014, pp. 1419. [5] H. Li, *JSSC*, 2015, pp.3145. [6] C. Sun, JSSC, 2015, pp. 828. [7] K. Yu, *JSSC*, 2016, pp.2129. [8] Y. Chen, *ISSCC*, 2015. [9] I. Ozkaya, *JSSC*, 2017, pp.3458.

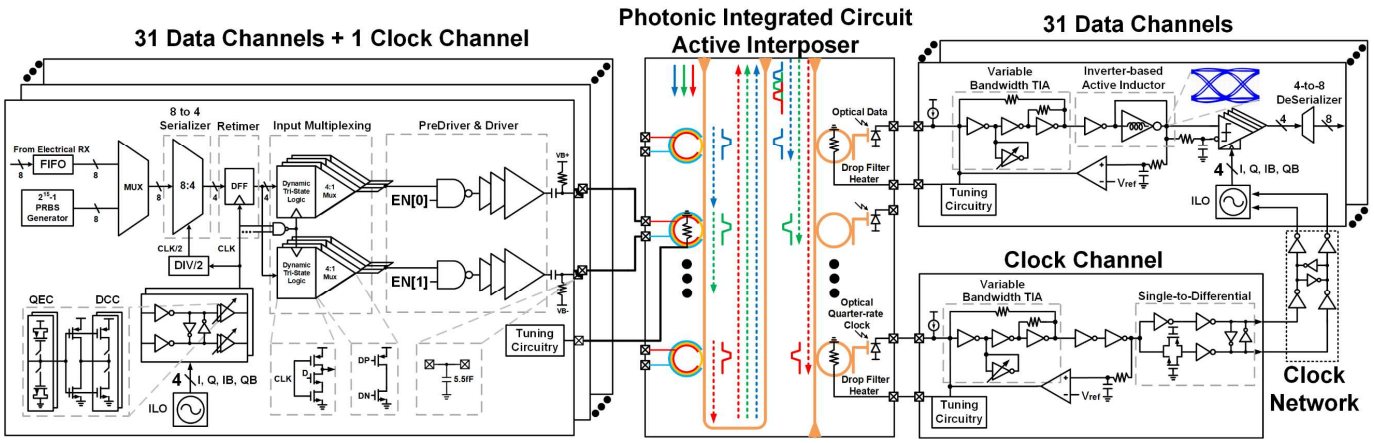


Fig. 1 12nm optical transceiver architecture.

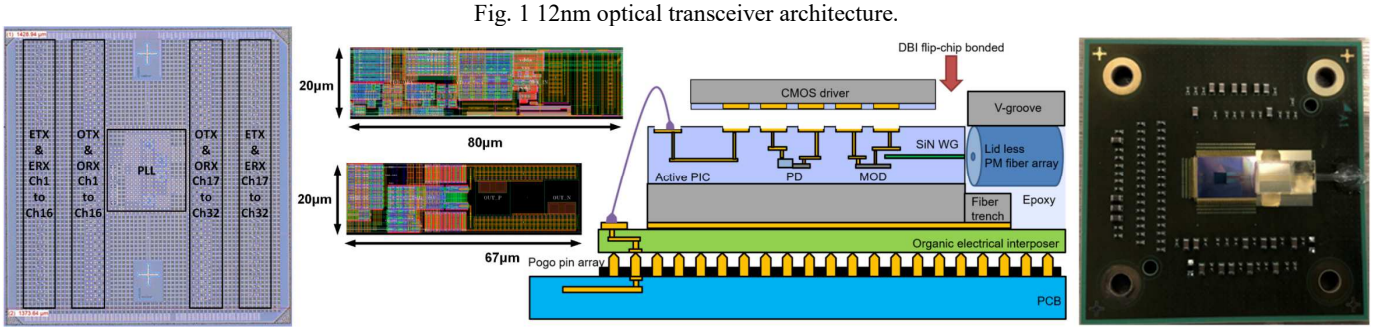


Fig. 2 12nm EIC micrograph, compact optical transceiver layout, 3D direct bond interconnect, and packaged transceiver module.

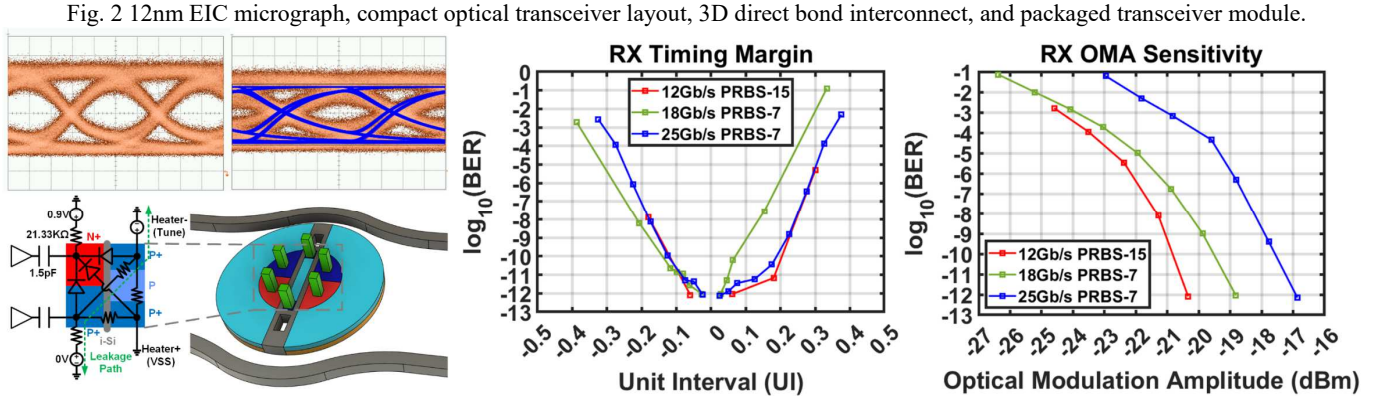
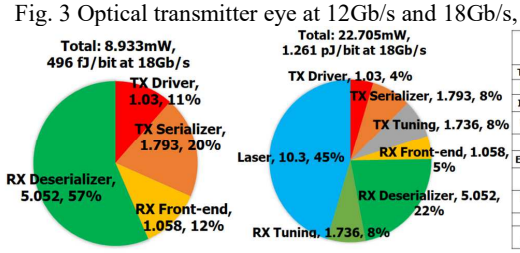


Fig. 3 Optical transmitter eye at 12Gb/s and 18Gb/s, microdisk modulator model, and optical receiver timing margin and OMA sensitivity.



	J. Buckwalter JSSC 2012 [3]	C. Li JSSC 2014 [4]	H. Li JSSC 2015 [5]	C. Sun JSSC 2015 [6]	This work
Technology	130nm SOI	65nm CMOS	65nm CMOS	0.18um CMOS	12nm FinFET
Data rate	25Gb/s	5Gb/s	25Gb/s	5Gb/s	18Gb/s
Integration	Monolithic	Wire-bonding	Wire-bonding	Monolithic	DBI
Modulator	Depletion Micro-ring	Injection Micro-ring	Depletion Micro-ring	Depletion Micro-ring	Depletion **Micro-disk**
Supply	1.5V	1V, 2V & 2.5V	1.2V & 2.4V	2.5V	0.7V
Equalization	2-tap FFE	2-tap FFE	2-tap FFE	None	None
Output Swing	2.4Vpp,diff	4Vpp,diff	4.4Vpp,diff	4.1Vpp,diff	1.2Vpp,diff
Extinction Ratio	6.5dB	12.7db	7dB	7.6dB	7dB
Power	207mW	4.04mW	113.5mW	5.8mW	2.832mW
Power Efficiency	8.28pJ/bit	808fJ/bit	4.54pJ/bit	1.16pJ/bit	157fJ/bit

	J. Buckwalter JSSC 2012 [3]	K. Yu JSSC 2016 [7]	Y. Chen ISSCC 2015 [8]	I. Ozkaya JSSC 2017 [9]	This work	
Technology	130nm SOI	65nm CMOS	28nm CMOS	14nm FinFET	12nm FinFET	
Data Rate	25Gb/s	25Gb/s	25Gb/s	64Gb/s	18Gb/s	25Gb/s
Input Capacitance	20fF	90fF	50fF	>69fF	14fF	
PD Responsivity	0.8A/W	0.45A/W	0.8A/W	0.52A/W	0.8A/W	
Supply	1.5V	1.2V / 1V	1.8V / 0.9V	1.15V / 0.9V	0.9V / 0.8V	0.9V
Clock Structure	NA	Forward CLK + IL LCVCO	CML Input Electrical CLK + ILO	Electrical CLK + ILO	Forward CLK + ILO	
Equalization	NA	CTLE	No, inductive peaking LA	1-tap DFE	No, use active inductor	
Input-Referred Noise Current	NA	1.8uA	5.4uA	NA	0.63uA	
Transimpedance	59dBΩ	66dBΩ	NA	50dBΩ	90dBΩ	
Power	48mW	17mW	50mW	89.6mW	6.11mW	5.67mW / 2.35mW w/o ILO
Sensitivity	-6dBm	-8.0dBm	-8.0dBm	-5.5dBm	-18.82 dBm	-16.9 dBm
Power Efficiency	1.92pJ/bit	680fJ/bit	2pJ/bit	1.4pJ/bit	339fJ/bit	227fJ/bit / 94fJ/bit w/o ILO

Fig. 4 Optical transceiver power breakdown, optical interconnect efficiency estimation, and TX (left) and RX (right) comparison tables.