ISG-D5680H 53Gbaud/s 8-Channel MZ Driver

General Description

ISG-D5680H is a high performance eight channel 53Gbaud/s differential input, differential output MZ driver die for 800Gbps applications. The driver can support input signals up to 600mVpp differential. The device can have an output up to 3.5Vpp output swing in linear mode with low Total Harmonic Distortion (THD).

ISG-D5680H is designed to be DC coupled to the modulator die. The die size is 4.07x1.57mm. The channel pitch is 375um. The driver offers SPI control for setting the gain and bias of the driver. It also allows monitoring the DC common mode voltage between the driver and modulator to accurately set the modulator bias on the PIC. The chip offers functionality to control the heaters on the Silicon PIC heater and operate two independent CW laser in an APC loop if desired.

ISG-D5680H is available in following configurations:

- ISG-D5680H- Flip-chip version
- ISG-D5680HW- Wire bonding version

Application

- Linear Optics
- 800G DR8
- PCIE Gen5/6
- 800G AOC

Ordering Information

Part Number	Ordering Part Number	Die	Shipping information
ISG-D5680H	ISG-D5680H	4.07x1.57x0.435mm	Tray
ISG-D5680HW	ISG-D5680HW	4.07x1.57x0.15mm	Tray

Features

- Supports Data rate up to 53Gbaud/s
- Differential Input, Differential Output
- RF input: AC coupled; RF output: DC coupled
- Typ. 42GHz Bandwidth
- Low power consumption- 360mW/channel @ 3Vpp (DC coupled to Modulator- including modulator load)
- Up to 3.5Vpp linear output
- 375um pitch between channels
- Die size - 4.07mmx1.57mm
- TX LOS detect
- Adjustable TX LOS threshold
- Support Auto Squelch mode
- Common mode voltage monitor to Modulator
- SPI digital interface
- Heater Control for Silicon PIC
- CW laser Control
- MPD current monitoring
- Adjustable low frequency gain from 12-19dB
- Adjustable Equalization up to 8dB at 26.5GHz
- Operating ambient Temperature range: -5°C to +85°C
- SiGe-based product

Block Diagram

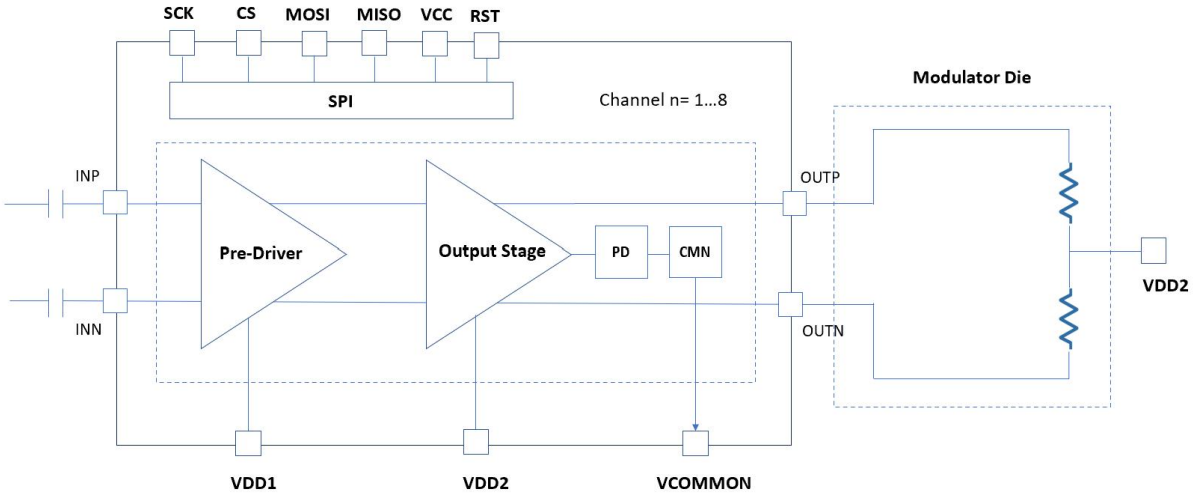


Figure 1 Single Channel Block Diagram

Absolute Maximum Rating

Stresses beyond those listed here may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" and "Typical Specifications" of this datasheet is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter	Description	Min.	Typ.	Max.	Unit
VDD1x[1]	Drain Bias Voltage, 1st Stage	-0.3	-	3.6	V
IDD1x	Drain Bias Current, 1st Stage	-	-	75	mA
VDD2x	Drain Bias Voltage, 2nd Stage	-0.3	-	4.8	V
IDD2x	Drain Bias Current, 2nd Stage	-	-	75	mA
Tstore	Storage Temperature	-40	-	125	°C
Vin_diff	Differential Input	-	-	1200	mVpp
Soldering Reflow	Soldering Reflow Temperature	-	-	250	°C
Pdissp	Absolute Maximum Power Dissipation (per/channel)	-	-	550	mW
VCOMMONx	Common mode voltage between driver and modulator	-	-	3.8	V

Tmax[2]	Short-time operating temperature	-	-	95	°C
Tbake	Bake Temperature (10 hours)	-	150	-	°C
Mstore	Storage Moisture	-	-	95	%

Note: 1."x" stands for the channel number 1 to 8.

2.Short time is defined as less than 96 hours at an operating time and less than 15 days in a year.

Recommended Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Unit
VDD1x	Drain Bias Voltage, 1st Stage	3.1	3.3	3.46	V
VDD2x[3]	Drain Bias Voltage, 2nd Stage	-	4	-	V
VDD_DIG	Digital power supply	3.1	3.3	3.46	V
VPKx	Peak Detector (typical range)	0	-	2	V
VCOMMONx	Common mode voltage between driver and modulator	3.3	3.4	3.5	V
IDD1x[4]	Drain Bias Current, 1st Stage	-	43	-	mA
IDD2x	Drain Bias Current, 2nd Stage	-	50	60[5]	mA
P_{dissp}	Power Dissipation (per channel @ Vout= 3Vpp)	-	360	-	mW
Heater Current	Current for Heater on the PIC	-	-	25	mA
Heater Voltage	Voltage for Heater on the PIC	0	-	2.5	V
Laserx	Laser Current Supply	-	180	-	mA
MPDx	MPD Current	-	-	500	uA
Operating ambient Temperature	Long-time working temperature	-5	-	85	°C
Operating Moisture	Long-time operating moisture	5	-	85	%

3. Stage 2 voltage depends on modulator impedance and max. output swing requirement. This voltage should be adjusted to keep Vcommon voltage in desired range with max Vcommonx value of 3.5V.

4. BW register set to 0.

5. IDD2x cannot exceed max value when using the CHx_OP_CURR register. The value of CHx_OP_CURR should be adjusted to keep IDD2x below the max. value

Typical Specifications (VDD1x=3.3V, VDD2x=4V, 25C, 100 ohm Diff. load)

Parameter	Description	Min.	Typ.	Max.	Unit
BRate	Bit Rate (Support PAM4)	26.6	53.125	56.25	Gbaud
Amplitude (Vpp)	Differential output voltage (100ohm diff. load)	-	-	3.5	Vpp
Vin_Diff	Input Differential voltage	-	450	600	mVppd
Max. Differential S21	Typical Gain at 1GHz	-	19	-	dB
S11 Differential	Input Return Loss, 0.1-28GHz	-	-12	-10	dB
Max. Equalization	Equalization @ 26.5GHz with respect to 1GHz (70ohm Diff. Modulator load)	-	8	-	dB
Bandwidth[6]	-3 dB Bandwidth	30[7]	42	-	GHz
Lower Cut-Off Frequency[8]	Lower Cut-Off Frequency	-	-	200	KHz
Channel-to-Channel Isolation	Crosstalk (0.1-26GHz)		35	-	dB
THD with diff Input @1GHz, Output=2.5V	Total Harmonic Distortion	-	2	4	%
Gain	Small Signal Transimpedance Gain (Reference to 1GHz, the load is 100 ohm)	12	-	19	dB
EQ	Max. Input EQ adjust range		-	8	dB
VDD1x Power Ripple	Power Ripple of VDD1x	-	-	15	mVpp
VDD2x Power Ripple	Power Ripple of VDD2x	-	-	30	mVpp

6.Wire bond inductance < 150pH at input/output

7. Greater than 3dB EQ condition

8. RF input AC capacitor is 0.1uF

SPI Electrical Parameters

Parameter	Description	Min.	Typ.	Max.	Unit
SPI Clock Rate	-	1	-	20	MHz
SPI Control Voltage	Low Logic	0	-	0.8	V
	High Logic	2	-	VDD_DIG	
IO Standard	HVCOMS	3	-	3.46	V
Data Register Width	-	32 (16 bits: Address/command 16 bits: Data)			Bit
Data Register Shift Direction	0: LSB first 1: MSB first	1			-

Environmental Rating

Parameter	Rating
ESD Classification Rating	TBD
Thermal Resistance	TBD
Moisture Sensitivity Level Rating	MSL1

Bias Sequence

Recommended Power Up Sequence

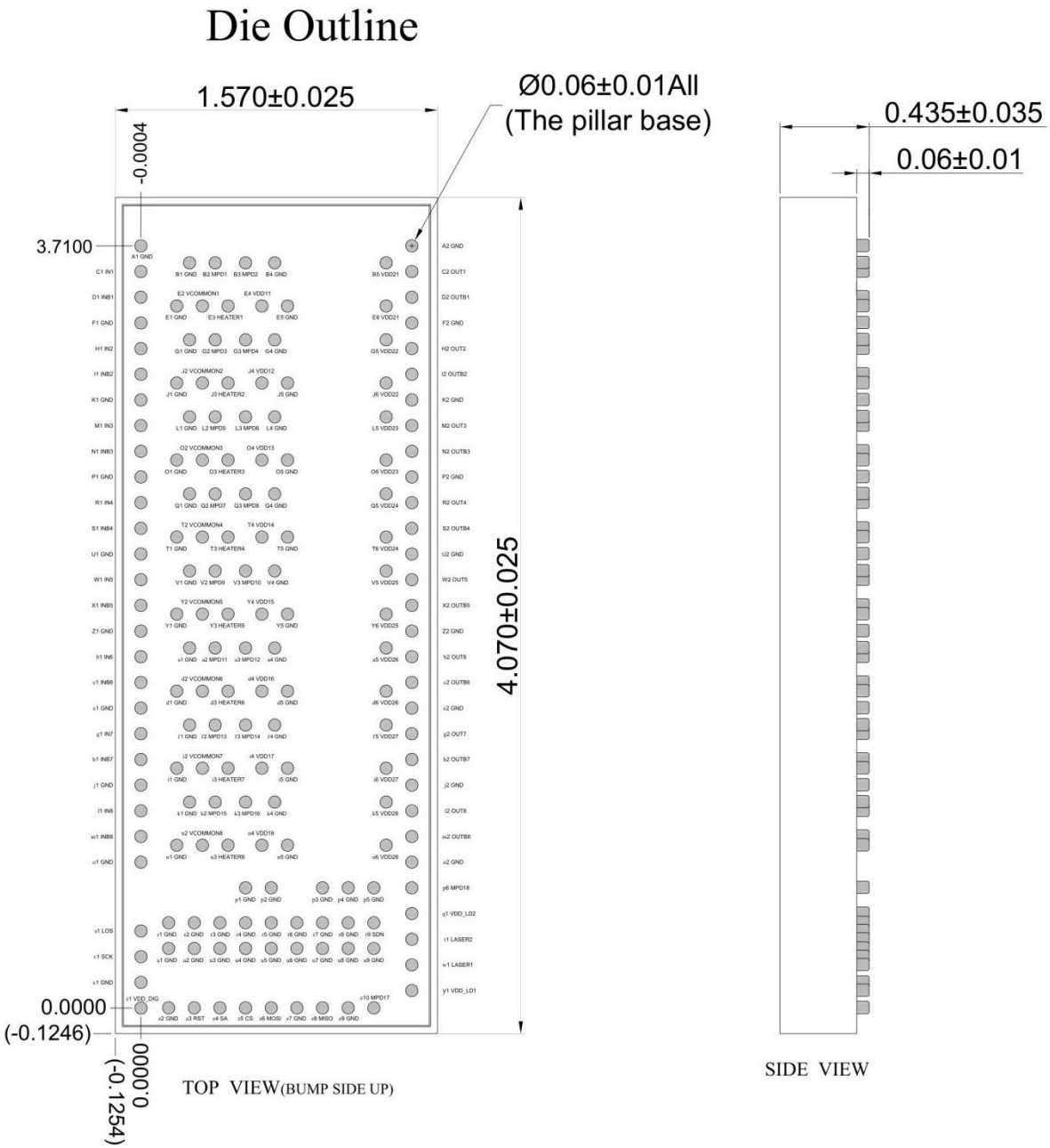
1. VDD1x and VDD2x can be turned on at the same time if the power on sequence meets:

   -1.6V<VDD1x-VDD2x<1V.

Recommended Power Down Sequence

1. No sequence is required as long as VDD1x and VDD2x voltages reach 1V within 50ms.

ISG-D5680H Outline & Pin Configuration



Unit:mm
The Pad center coordinates are referenced to the center of bottom left pad.
Diemsions in ( ) are for reference only.
Pin center position coordinates(X,Y) is showed in table.
Solder alloying: SnAg alloy(1.8% Ag by weight)

Pin center position coordinates

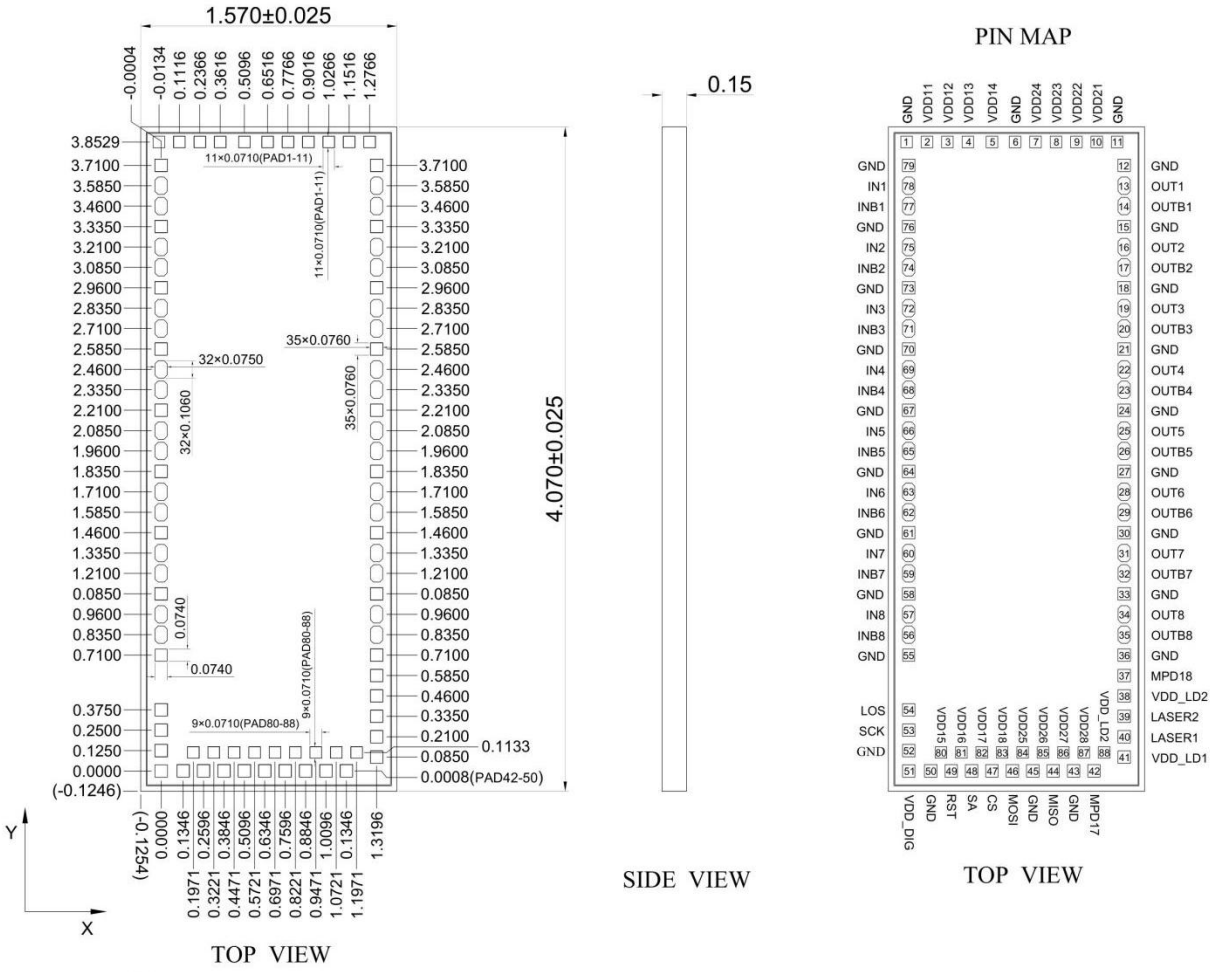
NO	PIN Name	Description	X	Y	NO	PIN Name	Description	X	Y
A1	GND	GND	-0.0004	3.7100	O4	VDD13	Drain Bias, 1st stage, Channel 3	0.5891	2.6675
A2	GND	GND	1.3196	3.7100	O5	GND	GND	0.7141	2.6675
B1	GND	GND	0.2366	3.6275	O6	VDD23	Drain Bias, 2nd stage, Channel 3	1.1946	2.6675
B2	MPD1	MPD 1	0.3616	3.6275	P1	GND	GND	-0.0004	2.5850
B3	MPD2	MPD 2	0.5096	3.6275	P2	GND	GND	1.3196	2.5850
B4	GND	GND	0.6516	3.6275	Q1	GND	GND	0.2366	2.5025
B5	VDD21	Drain Bias, 2nd stage, Channel 1	1.1946	3.6275	Q2	MPD7	MPD 7	0.3616	2.5025
C1	IN1	RF Input voltage(positive) 1	-0.0004	3.5850	Q3	MPD8	MPD 8	0.5096	2.5025
C2	OUT1	RF Output voltage(positive) 1	1.3196	3.5850	Q4	GND	GND	0.6516	2.5025
D1	INB1	RF Input voltage(negative) 1	-0.0004	3.4600	Q5	VDD24	Drain Bias, 2nd stage, Channel 4	1.1946	2.5025
D2	OUTB1	RF Output voltage(negative) 1	1.3196	3.4600	R1	IN4	RF Input voltage(positive) 4	-0.0004	2.4600
E1	GND	GND	0.1741	3.4175	R2	OUT4	RF Output voltage(positive) 4	1.3196	2.4600
E2	VCOMMON1	Common Mode voltage,Channel 1	0.2991	3.4175	S1	INB4	RF Input voltage(negative) 4	-0.0004	2.3350
E3	HEATER1	Voltage for Heater on the PIC Channel 1	0.4241	3.4175	S2	OUTB4	RF Output voltage(negative) 4	1.3196	2.3350
E4	VDD11	Drain Bias, 1st stage, Channel 1	0.5891	3.4175	T1	GND	GND	0.1741	2.2925
E5	GND	GND	0.7141	3.4175	T2	VCOMMON4	Common Mode voltage,Channel 4	0.2991	2.2925
E6	VDD21	Drain Bias, 2nd stage, Channel 1	1.1946	3.4175	T3	HEATER4	Voltage for Heater on the PIC Channel 4	0.4241	2.2925
F1	GND	GND	-0.0004	3.3350	T4	VDD14	Drain Bias, 1st stage, Channel 4	0.5891	2.2925
F2	GND	GND	1.3196	3.3350	T5	GND	GND	0.7141	2.2925
G1	GND	GND	0.2366	3.2525	T6	VDD24	Drain Bias, 2nd stage, Channel 4	1.1946	2.2925
G2	MPD3	MPD 3	0.3616	3.2525	U1	GND	GND	-0.0004	2.2100
G3	MPD4	MPD 4	0.5096	3.2525	U2	GND	GND	1.3196	2.2100
G4	GND	GND	0.6516	3.2525	V1	GND	GND	0.2366	2.1275
G5	VDD22	Drain Bias, 2nd stage, Channel 2	1.1946	3.2525	V2	MPD9	MPD 9	0.3616	2.1275
H1	IN2	RF Input voltage(positive) 2	-0.0004	3.2100	V3	MPD10	MPD 10	0.5096	2.1275
H2	OUT2	RF Output voltage(positive) 2	1.3196	3.2100	V4	GND	GND	0.6516	2.1275
I1	INB2	RF Input voltage(negative) 2	-0.0004	3.0850	V5	VDD25	Drain Bias, 2nd stage, Channel 5	1.1946	2.1275
I2	OUTB2	RF Output voltage(negative) 2	1.3196	3.0850	W1	IN5	RF Input voltage(positive) 5	-0.0004	2.0850
J1	GND	GND	0.1741	3.0425	W2	OUT5	RF Output voltage(positive) 5	1.3196	2.0850
J2	VCOMMON2	Common Mode voltage,Channel 2	0.2991	3.0425	X1	INB5	RF Input voltage(negative) 5	-0.0004	1.9600
J3	HEATER2	Voltage for Heater on the PIC Channel 2	0.4241	3.0425	X2	OUTB5	RF Output voltage(negative) 5	1.3196	1.9600
J4	VDD12	Drain Bias, 1st stage, Channel 2	0.5891	3.0425	Y1	GND	GND	0.1741	1.9175
J5	GND	GND	0.7141	3.0425	Y2	VCOMMON5	Common Mode voltage,Channel 5	0.2991	1.9175
J6	VDD22	Drain Bias, 2nd stage, Channel 2	1.1946	3.0425	Y3	HEATER5	Voltage for Heater on the PIC Channel 5	0.4241	1.9175
K1	GND	GND	-0.0004	2.9600	Y4	VDD15	Drain Bias, 1st stage, Channel 5	0.5891	1.9175
K2	GND	GND	1.3196	2.9600	Y5	GND	GND	0.7141	1.9175
L1	GND	GND	0.2366	2.8775	Y6	VDD25	Drain Bias, 2nd stage, Channel 5	1.1946	1.9175
L2	MPD5	MPD 5	0.3616	2.8775	Z1	GND	GND	-0.0004	1.8350
L3	MPD6	MPD 6	0.5096	2.8775	Z2	GND	GND	1.3196	1.8350
L4	GND	GND	0.6516	2.8775	a1	GND	GND	0.2366	1.7525
L5	VDD23	Drain Bias, 2nd stage, Channel 3	1.1946	2.8775	a2	MPD11	MPD 11	0.3616	1.7525
M1	IN3	RF Input voltage(positive) 3	-0.0004	2.8350	a3	MPD12	MPD 12	0.5096	1.7525
M2	OUT3	RF Output voltage(positive) 3	1.3196	2.8350	a4	GND	GND	0.6516	1.7525
N1	INB3	RF Input voltage(negative) 3	-0.0004	2.7100	a5	VDD26	Drain Bias, 2nd stage, Channel 6	1.1946	1.7525
N2	OUTB3	RF Output voltage(negative) 3	1.3196	2.7100	b1	IN6	RF Input voltage(positive) 6	-0.0004	1.7100
O1	GND	GND	0.1741	2.6675	b2	OUT6	RF Output voltage(positive) 6	1.3196	1.7100
O2	VCOMMON3	Common Mode voltage,Channel 3	0.2991	2.6675	c1	INB6	RF Input voltage(negative) 6	-0.0004	1.5850
O3	HEATER3	Voltage for Heater on the PIC Channel 3	0.4241	2.6675	c2	OUTB6	RF Output voltage(negative) 6	1.3196	1.5850

Pin center position coordinates

NO	PIN Name	Description	X	Y
d1	GND	GND	0.1741	1.5425
d2	VCOMMON6	Common Mode voltage,Channel 6	0.2991	1.5425
d3	HEATER6	Voltage for Heater on the PIC Channel 6	0.4241	1.5425
d4	VDD16	Drain Bias, 1st stage, Channel 6	0.5891	1.5425
d5	GND	GND	0.7141	1.5425
d6	VDD26	Drain Bias, 2nd stage, Channel 6	1.1946	1.5425
e1	GND	GND	-0.0004	1.4600
e2	GND	GND	1.3196	1.4600
f1	GND	GND	0.2366	1.3775
f2	MPD13	MPD 13	0.3616	1.3775
f3	MPD14	MPD 14	0.5096	1.3775
f4	GND	GND	0.6516	1.3775
f5	VDD27	Drain Bias, 2nd stage, Channel 7	1.1946	1.3775
g1	IN7	RF Input voltage(positive) 7	-0.0004	1.3350
g2	OUT7	RF Output voltage(positive) 7	1.3196	1.3350
h1	INB7	RF Input voltage(negative) 7	-0.0004	1.2100
h2	OUTB7	RF Output voltage(negative) 7	1.3196	1.2100
i1	GND	GND	0.1741	1.1675
i2	VCOMMON7	Common Mode voltage,Channel 7	0.2991	1.1675
i3	HEATER7	Voltage for Heater on the PIC Channel 7	0.4241	1.1675
i4	VDD17	Drain Bias, 1st stage, Channel 7	0.5891	1.1675
i5	GND	GND	0.7141	1.1675
i6	VDD27	Drain Bias, 2nd stage, Channel 7	1.1946	1.1675
j1	GND	GND	-0.0004	1.0850
j2	GND	GND	1.3196	1.0850
k1	GND	GND	0.2366	1.0025
k2	MPD15	MPD 15	0.3616	1.0025
k3	MPD16	MPD 16	0.5096	1.0025
k4	GND	GND	0.6516	1.0025
k5	VDD28	Drain Bias, 2nd stage, Channel 8	1.1946	1.0025
l1	IN8	RF Input voltage(positive) 8	-0.0004	0.9600
l2	OUT8	RF Output voltage(positive) 8	1.3196	0.9600
m1	INB8	RF Input voltage(negative) 8	-0.0004	0.8350
m2	OUTB8	RF Output voltage(negative) 8	1.3196	0.8350
n1	GND	GND	0.1741	0.7925
n2	VCOMMON8	Common Mode voltage,Channel 8	0.2991	0.7925
n3	HEATER8	Voltage for Heater on the PIC Channel 8	0.4241	0.7925
n4	VDD18	Drain Bias, 1st stage, Channel 8	0.5891	0.7925
n5	GND	GND	0.7141	0.7925
n6	VDD28	Drain Bias, 2nd stage, Channel 8	1.1946	0.7925
o1	GND	GND	-0.0004	0.7100
o2	GND	GND	1.3196	0.7100
p1	GND	GND	0.5096	0.5850
p2	GND	GND	0.6346	0.5850
p3	GND	GND	0.8846	0.5850
p4	GND	GND	1.0096	0.5850
p5	GND	GND	1.1346	0.5850
p6	MPD18	MPD 18	1.3196	0.5850

NO	PIN Name	Description	X	Y
q1	VDD_LD2	Power supply for Laser 2	1.3196	0.4600
r1	GND	GND	0.1346	0.4150
r2	GND	GND	0.2596	0.4150
r3	GND	GND	0.3846	0.4150
r4	GND	GND	0.5096	0.4150
r5	GND	GND	0.6346	0.4150
r6	GND	GND	0.7596	0.4150
r7	GND	GND	0.8846	0.4150
r8	GND	GND	1.0096	0.4150
r9	SDN	Shut Down	1.1346	0.4150
s1	LOS	Loss of signal	0.0000	0.3750
t1	LASER2	Laser bias supply Channel 2	1.3196	0.3350
u1	GND	GND	0.1346	0.2900
u2	GND	GND	0.2596	0.2900
u3	GND	GND	0.3846	0.2900
u4	GND	GND	0.5096	0.2900
u5	GND	GND	0.6346	0.2900
u6	GND	GND	0.7596	0.2900
u7	GND	GND	0.8846	0.2900
u8	GND	GND	1.0096	0.2900
u9	GND	GND	1.1346	0.2900
v1	SCK	Clock	0.0000	0.2500
w1	LASER1	Laser bias supply Channel 1	1.3196	0.2100
x1	GND	GND	0.0000	0.1250
y1	VDD_LD1	Power supply for Laser 1	1.3196	0.0850
z1	VDD_DIG	Digital power supply	0.0000	0.0000
z2	GND	GND	0.1346	0.0008
z3	RST	Digital Reset	0.2596	0.0008
z4	SA	Slave Address	0.3846	0.0008
z5	CS	Chip Select	0.5096	0.0008
z6	MOSI	Master Output, Slave Input	0.6346	0.0008
z7	GND	GND	0.7596	0.0008
z8	MISO	Master Input, Slave Output	0.8846	0.0008
z9	GND	GND	1.0096	0.0008
z10	MPD17	MPD 17	1.1346	0.0008

ISG-D5680HW Outline & Pin Configuration



Pin Description

No.	PIN Name	PIN Type	PIN Description
1	GND	GND	Ground
2	VDD11	Power	Drain Bias, 1st stage, Channel 1

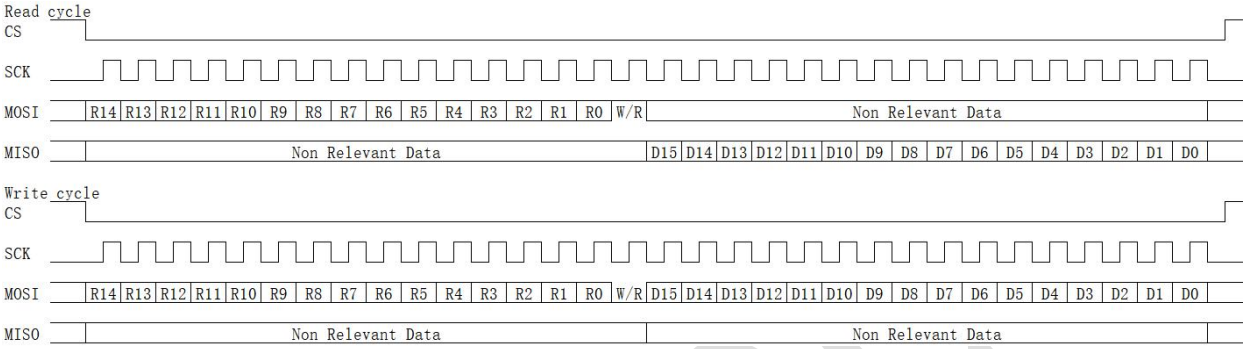
3	VDD12	Power	Drain Bias, 1st stage, Channel 2
4	VDD13	Power	Drain Bias, 1st stage, Channel 3
5	VDD14	Power	Drain Bias, 1st stage, Channel 4
6	GND	GND	Ground
7	VDD24	Power	Drain Bias, 2nd stage, Channel 4
8	VDD23	Power	Drain Bias, 2nd stage, Channel 3
9	VDD22	Power	Drain Bias, 2nd stage, Channel 2
10	VDD21	Power	Drain Bias, 2nd stage, Channel 1
11	GND	GND	Ground
12	GND	GND	Ground
13	OUT1	RF	Output Positive (Channel 1)
14	OUTB1	RF	Output Negative (Channel 1)
15	GND	GND	Ground
16	OUT2	RF	Output Positive (Channel 2)
17	OUTB2	RF	Output Negative (Channel 2)
18	GND	GND	Ground
19	OUT3	RF	Output Positive (Channel 3)
20	OUTB3	RF	Output Negative (Channel 3)
21	GND	GND	Ground
22	OUT4	RF	Output Positive (Channel 4)
23	OUTB4	RF	Output Negative (Channel 4)
24	GND	GND	Ground
25	OUT5	RF	Output Positive (Channel 5)
26	OUTB5	RF	Output Negative (Channel 5)
27	GND	GND	Ground
28	OUT6	RF	Output Positive (Channel 6)
29	OUTB6	RF	Output Negative (Channel 6)
30	GND	GND	Ground
31	OUT7	RF	Output Positive (Channel 7)
32	OUTB7	RF	Output Negative (Channel 7)
33	GND	GND	Ground
34	OUT8	RF	Output Positive (Channel 8)
35	OUTB8	RF	Output Negative (Channel 8)
36	GND	GND	Ground
37	MPD18	Control	MPD18
38	VDD_LD2	Power	Power Supply for Laser2
39	LASER2	Power	Laser Bias Supply (Channel 2)
40	LASER1	Power	Laser Bias Supply (Channel 1)
41	VDD_LD1	Power	Power Supply for Laser1
42	MPD17	Control	MPD17
43	GND	GND	Ground
44	MISO	Control	Master in, Slave out
45	GND	GND	Ground
46	MOSI	Control	Master out, Slave in
47	CS	Control	Chip Select

48	SA	Control	Slave Address
49	RST	Control	Digital Reset
50	GND	GND	Ground
51	VDD_DIG	Power	Digital power supply
52	GND	GND	Ground
53	SCK	Control	Clock
54	LOS	Control	Loss of Signal
55	GND	GND	Ground
56	INB8	RF	Input Negative (Channel 8)
57	IN8	RF	Input Positive(Channel 8)
58	GND	GND	Ground
59	INB7	RF	Input Negative (Channel 7)
60	IN7	RF	Input Positive(Channel 7)
61	GND	GND	Ground
62	INB6	RF	Input Negative (Channel 6)
63	IN6	RF	Input Positive(Channel 6)
64	GND	GND	Ground
65	INB5	RF	Input Negative (Channel 5)
66	IN5	RF	Input Positive(Channel 5)
67	GND	GND	Ground
68	INB4	RF	Input Negative (Channel 4)
69	IN4	RF	Input Positive(Channel 4)
70	GND	GND	Ground
71	INB3	RF	Input Negative (Channel 3)
72	IN3	RF	Input Positive(Channel 3)
73	GND	GND	Ground
74	INB2	RF	Input Negative (Channel 2)
75	IN2	RF	Input Positive(Channel 2)
76	GND	GND	Ground
77	INB1	RF	Input Negative (Channel 1)
78	IN1	RF	Input Positive(Channel 1)
79	GND	GND	Ground
80	VDD15	Power	Drain Bias, 1st stage, Channel 5
81	VDD16	Power	Drain Bias, 1st stage, Channel 6
82	VDD17	Power	Drain Bias, 1st stage, Channel 7
83	VDD18	Power	Drain Bias, 1st stage, Channel 8
84	VDD25	Power	Drain Bias, 2nd stage, Channel 5
85	VDD26	Power	Drain Bias, 2nd stage, Channel 6
86	VDD27	Power	Drain Bias, 2nd stage, Channel 7
87	VDD28	Power	Drain Bias, 2nd stage, Channel 8
88	VDD_LD2	Power	Power Supply for Laser2

Note：MPD cathode connects to MPDx pin, MPD anode connects to GND.

SPI Settings

1.1 Read and Write Cycles



Read Cycle

1. After CS is pulled down, the master sends 15-bit register address (R0~14) and R flag (R is 1 and means read) through MOSI.
2. The slave sends two-byte data (D0~15) through MISO, and the master pulls up CS.

Write Cycle

1. After CS is pulled down, the master sends 15-bit register address (R0~14) and W flag (W is 0 and means write) through MOSI.
2. The master sends two-byte data (D0~15) through MOSI and pulls up CS.

1.2 SPI Slave Address

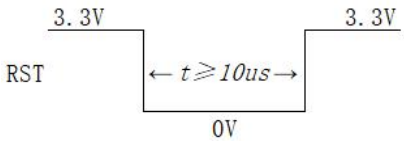
For each device, the first 3-bit address (R12~14) can be set up by SA pin. SA is pulled up to 3.3V internally by default and can be pulled down to 0V.

SA	Slave Address (R12~14)
0V	0x4
3.3V	0x6

1.3 Reset

To reset all registers, there are two options.

1. Hardware rest: pull down the external RST pin to 0V and give a 10us pulse at least. RST should stay at 3.3V in normal condition. RST pin is pulled up to 3.3V internally by default.
2. Software rest: write 0x01 to RESET register.



1.4 Shutdown

To shut down all channels, there are two options.

1. Hardware shutdown: connect SDN pin to 3.3V.
2. Software shutdown: write 0x01 to SHUTDOWN register.

NOTE: if an external voltage is applied to SDN pin, software shutdown cannot work.

Functional detailed description

NOTE: in this section, it introduces registers with default slave address 0x6XXX, otherwise 0x4XXX should be used if SA pin is pulled down to 0V.

1.1 Common Registers for all Channels

A. Reading the Driver (Part) ID and Revision ID
B. Resetting (i. e. Soft Resetting) the Driver.
C. Shutting down the Driver

Register Name	Address	Register Settings	Channel	Description
PID	*0x6002*	**D15|D14|D13|D12|D11|D10|D9| D8|D7|D6|D5|D4|D3|D2|D1|D0**	1-8	**16-bit Driver (Part) ID Default: 0x009D**
REV	*0x6004*	**D15|D14|D13|D12|D11|D10|D9| D8|D7|D6|D5|D4|D3|D2|D1|D0**	1-8	**16-bit Revision ID Default: 0x0000**
RESET	*0x6005*	**x|x|x|x|x|x|x|x|x|x|x|x|x|x|x|D0**	1-8	**D0 = 0: Normal (Default) D0 = 1: Reset State**
SHUTDOWN	*0x6006*	**x|x|x|x|x|x|x|x|x|x|x|x|x|x|x|D0**	1-8	**D0 = 0: Normal (Default) D0 = 1: Shutdown all CH**
SHUTDOWN_CH	*0x601B*	**x|x|x|x|x|x|x|x| D7|D6|D5|D4|D3|D2|D1|D0**	1-8	**D0 = 1: Shutdown CH1 D1 = 1: Shutdown CH2 D2 = 1: Shutdown CH3 D3 = 1: Shutdown CH4 D4 = 1: Shutdown CH5 D5 = 1: Shutdown CH6 D6 = 1: Shutdown CH7 D7 = 1: Shutdown CH8**

1.2 Current Control

For each channel, the stage current can be independently set using CHx_IP_CURR and CHx_OP_CURR register. The range that can be set is from 0x00 to 0xFF.

Register Name	Address	Register Settings	Channel	Description	
CH1_IP_CURR	*0x600B*	x|x|x|x|x|x|x|x| D7|D6|D5|D4|D3|D2|D1|D0	Channel 1	0000_0000 : Min	1111_1111 : Max
				RECOMMENDED	*TBD*
CH2_IP_CURR	*0x6089*	x|x|x|x|x|x|x|x| D7|D6|D5|D4|D3|D2|D1|D0	Channel 2	0000_0000 : Min	1111_1111 : Max
				RECOMMENDED	*TBD*
CH3_IP_CURR	*0x6109*	x|x|x|x|x|x|x|x| D7|D6|D5|D4|D3|D2|D1|D0	Channel 3	0000_0000 : Min	1111_1111 : Max
				RECOMMENDED	*TBD*
CH4_IP_CURR	*0x6189*	x|x|x|x|x|x|x|x| D7|D6|D5|D4|D3|D2|D1|D0	Channel 4	0000_0000 : Min	1111_1111 : Max
				RECOMMENDED	*TBD*
CH5_IP_CURR	*0x6209*	x|x|x|x|x|x|x|x| D7|D6|D5|D4|D3|D2|D1|D0	Channel 5	0000_0000 : Min	1111_1111 : Max
				RECOMMENDED	*TBD*
CH6_IP_CURR	*0x6289*	x|x|x|x|x|x|x|x| D7|D6|D5|D4|D3|D2|D1|D0	Channel 6	0000_0000 : Min	1111_1111 : Max
				RECOMMENDED	*TBD*
CH7_IP_CURR	*0x6309*	x|x|x|x|x|x|x|x| D7|D6|D5|D4|D3|D2|D1|D0	Channel 7	0000_0000 : Min	1111_1111 : Max
				RECOMMENDED	*TBD*
CH8_IP_CURR	*0x6389*	x|x|x|x|x|x|x|x| D7|D6|D5|D4|D3|D2|D1|D0	Channel 8	0000_0000 : Min	1111_1111 : Max
				RECOMMENDED	*TBD*
CH1_OP_CURR	*0x600C*	x|x|x|x|x|x|x|x| D7|D6|D5|D4|D3|D2|D1|D0	Channel 1	0000_0000 : Min	1111_1111 : Max
				RECOMMENDED	*TBD*
CH2_OP_CURR	*0x608A*	x|x|x|x|x|x|x|x| D7|D6|D5|D4|D3|D2|D1|D0	Channel 2	0000_0000 : Min	1111_1111 : Max
				RECOMMENDED	*TBD*
CH3_OP_CURR	*0x610A*	x|x|x|x|x|x|x|x| D7|D6|D5|D4|D3|D2|D1|D0	Channel 3	0000_0000 : Min	1111_1111 : Max
				RECOMMENDED	*TBD*
CH4_OP_CURR	*0x618A*	x|x|x|x|x|x|x|x| D7|D6|D5|D4|D3|D2|D1|D0	Channel 4	0000_0000 : Min	1111_1111 : Max
				RECOMMENDED	*TBD*
CH5_OP_CURR	*0x620A*	x|x|x|x|x|x|x|x| D7|D6|D5|D4|D3|D2|D1|D0	Channel 5	0000_0000 : Min	1111_1111 : Max
				RECOMMENDED	*TBD*
CH6_OP_CURR	*0x628A*	x|x|x|x|x|x|x|x| D7|D6|D5|D4|D3|D2|D1|D0	Channel 6	0000_0000 : Min	1111_1111 : Max
				RECOMMENDED	*TBD*
CH7_OP_CURR	*0x630A*	x|x|x|x|x|x|x|x| D7|D6|D5|D4|D3|D2|D1|D0	Channel 7	0000_0000 : Min	1111_1111 : Max
				RECOMMENDED	*TBD*
CH8_OP_CURR	*0x638A*	x|x|x|x|x|x|x|x| D7|D6|D5|D4|D3|D2|D1|D0	Channel 8	0000_0000 : Min	1111_1111 : Max
				RECOMMENDED	*TBD*

1.3 Frequency Response Control

For each channel, the low frequency response control voltage can be independently set using CHx_LO_FERQ_CTRL register. The range that can be set is from 0 to 2.8 V. For each channel, the high frequency response control voltage can be independently set using CHx_HI_FERQ_CTRL register. The range that can be set is from 0 to 2.8 V.

Register Name	Address	Register Settings	Channel	Description	
CH1_LO_FERQ_CTRL	*0x6007*	x|x|x|x|x|x|x|x| D7|D6|D5|D4|D3|D2|D1|D0	Channel 1	0000_0000 : Min	1111_1111 : Max
				RECOMMENDED	*TBD*
CH2_LO_FERQ_CTRL	*0x6085*	x|x|x|x|x|x|x|x| D7|D6|D5|D4|D3|D2|D1|D0	Channel 2	0000_0000 : Min	1111_1111 : Max

				RECOMMENDED	*TBD*
CH3_LO_FERQ_CTRL	*0x6105*	**x|x|x|x|x|x|x|x| D7|D6|D5|D4|D3|D2|D1|D0**	Channel 3	**0000_0000 : Min**	**1111_1111 : Max**
				RECOMMENDED	*TBD*
CH4_LO_FERQ_CTRL	*0x6185*	**x|x|x|x|x|x|x|x| D7|D6|D5|D4|D3|D2|D1|D0**	Channel 4	**0000_0000 : Min**	**1111_1111 : Max**
				RECOMMENDED	*TBD*
CH5_LO_FERQ_CTRL	*0x6205*	**x|x|x|x|x|x|x|x| D7|D6|D5|D4|D3|D2|D1|D0**	Channel 5	**0000_0000 : Min**	**1111_1111 : Max**
				RECOMMENDED	*TBD*
CH6_LO_FERQ_CTRL	*0x6285*	**x|x|x|x|x|x|x|x| D7|D6|D5|D4|D3|D2|D1|D0**	Channel 6	**0000_0000 : Min**	**1111_1111 : Max**
				RECOMMENDED	*TBD*
CH7_LO_FERQ_CTRL	*0x6305*	**x|x|x|x|x|x|x|x| D7|D6|D5|D4|D3|D2|D1|D0**	Channel 7	**0000_0000 : Min**	**1111_1111 : Max**
				RECOMMENDED	*TBD*
CH8_LO_FERQ_CTRL	*0x6385*	**x|x|x|x|x|x|x|x| D7|D6|D5|D4|D3|D2|D1|D0**	Channel 8	**0000_0000 : Min**	**1111_1111 : Max**
				RECOMMENDED	*TBD*
CH1_HI_FERQ_CTRL	*0x600A*	**x|x|x|x|x|x|x|x| D7|D6|D5|D4|D3|D2|D1|D0**	Channel 1	**0000_0000 : Min**	**1111_1111 : Max**
				RECOMMENDED	*TBD*
CH2_HI_FERQ_CTRL	*0x6088*	**x|x|x|x|x|x|x|x| D7|D6|D5|D4|D3|D2|D1|D0**	Channel 2	**0000_0000 : Min**	**1111_1111 : Max**
				RECOMMENDED	*TBD*
CH3_HI_FERQ_CTRL	*0x6108*	**x|x|x|x|x|x|x|x| D7|D6|D5|D4|D3|D2|D1|D0**	Channel 3	**0000_0000 : Min**	**1111_1111 : Max**
				RECOMMENDED	*TBD*
CH4_HI_FERQ_CTRL	*0x6188*	**x|x|x|x|x|x|x|x| D7|D6|D5|D4|D3|D2|D1|D0**	Channel 4	**0000_0000 : Min**	**1111_1111 : Max**
				RECOMMENDED	*TBD*
CH5_HI_FERQ_CTRL	*0x6208*	**x|x|x|x|x|x|x|x| D7|D6|D5|D4|D3|D2|D1|D0**	Channel 5	**0000_0000 : Min**	**1111_1111 : Max**
				RECOMMENDED	*TBD*
CH6_HI_FERQ_CTRL	*0x6288*	**x|x|x|x|x|x|x|x| D7|D6|D5|D4|D3|D2|D1|D0**	Channel 6	**0000_0000 : Min**	**1111_1111 : Max**
				RECOMMENDED	*TBD*
CH7_HI_FERQ_CTRL	*0x6308*	**x|x|x|x|x|x|x|x| D7|D6|D5|D4|D3|D2|D1|D0**	Channel 7	**0000_0000 : Min**	**1111_1111 : Max**
				RECOMMENDED	*TBD*
CH8_HI_FERQ_CTRL	*0x6388*	**x|x|x|x|x|x|x|x| D7|D6|D5|D4|D3|D2|D1|D0**	Channel 8	**0000_0000 : Min**	**1111_1111 : Max**
				RECOMMENDED	*TBD*

1.4 Heater Current Control

For each channel, the heater current can be independently set using CHx_HEATER register. The range that can be set is from 0x00 to 0xFF. The heater current can be independently enabled using HEATER_EN register.

Register Name	Address	Register Settings	Channel	Description
HEATER_EN	*0x6219*	**x|x|x|x|x|x|x|x|D7|D6|D5|D4|D3|D2|D1|D0**	1-8	**D0 = 1: CH1_ HEATER enabled** **D1 = 1: CH2_ HEATER enabled** **D2 = 1: CH3_ HEATER enabled** **D3 = 1: CH4_ HEATER enabled** **D4 = 1: CH5_ HEATER enabled** **D5 = 1: CH6_ HEATER enabled** **D6 = 1: CH7_ HEATER enabled** **D7 = 1: CH8_ HEATER enabled**

Register Name	Address	Register Settings	Channel	Description	
CH1_HEATER	*0x6019*	**x|x|x|x|x|x|x|x|D7|D6|D5|D4|D3|D2|D1|D0**	Channel 1	**0000_0000 : Min**	**1111_1111 : Max**
				RECOMMENDED	*TBD*
CH2_HEATER	*0x608C*	**x|x|x|x|x|x|x|x|D7|D6|D5|D4|D3|D2|D1|D0**	Channel 2	**0000_0000 : Min**	**1111_1111 : Max**
				RECOMMENDED	*TBD*
CH3_HEATER	*0x610C*	**x|x|x|x|x|x|x|x|D7|D6|D5|D4|D3|D2|D1|D0**	Channel 3	**0000_0000 : Min**	**1111_1111 : Max**
				RECOMMENDED	*TBD*
CH4_HEATER	*0x618C*	**x|x|x|x|x|x|x|x|D7|D6|D5|D4|D3|D2|D1|D0**	Channel 4	**0000_0000 : Min**	**1111_1111 : Max**
				RECOMMENDED	*TBD*
CH5_HEATER	*0x620C*	**x|x|x|x|x|x|x|x|D7|D6|D5|D4|D3|D2|D1|D0**	Channel 5	**0000_0000 : Min**	**1111_1111 : Max**
				RECOMMENDED	*TBD*
CH6_HEATER	*0x628C*	**x|x|x|x|x|x|x|x|D7|D6|D5|D4|D3|D2|D1|D0**	Channel 6	**0000_0000 : Min**	**1111_1111 : Max**
				RECOMMENDED	*TBD*
CH7_HEATER	*0x630C*	**x|x|x|x|x|x|x|x|D7|D6|D5|D4|D3|D2|D1|D0**	Channel 7	**0000_0000 : Min**	**1111_1111 : Max**
				RECOMMENDED	*TBD*
CH8_HEATER	*0x638C*	**x|x|x|x|x|x|x|x|D7|D6|D5|D4|D3|D2|D1|D0**	Channel 8	**0000_0000 : Min**	**1111_1111 : Max**
				RECOMMENDED	*TBD*

1.5 Automatic or Manual Laser Current Control

It has 2 channels of laser current control. The control can be enabled by CHx_LASER_DIS register. Automatic or manual control can be set using CHx_APC_EN register. The automatic or manual laser current control voltage can be set using CHx_APC and CHx_MPC register respectively. The range that can be set is from 0 to 2.8 V.

Register Name	Address	Register Settings	Channel	Description	
CH1_APC	*0x6319*	**x|x|x|x|x|x|x|x|D7|D6|D5|D4|D3|D2|D1|D0**	Channel 1	**0000_0000:Min**	**1111_1111:Max**
				RECOMMENDED	*TBD*
CH2_APC	*0x631A*	**x|x|x|x|x|x|x|x|D7|D6|D5|D4|D3|D2|D1|D0**	Channel 2	**0000_0000:Min**	**1111_1111:Max**
				RECOMMENDED	*TBD*
CH1_MPC	*0x6399*	**x|x|x|x|x|x|x|x|D7|D6|D5|D4|D3|D2|D1|D0**	Channel 1	**0000_0000:Min**	**1111_1111:Max**
				RECOMMENDED	*TBD*
CH2_MPC	*0x639A*	**x|x|x|x|x|x|x|x|D7|D6|D5|D4|D3|D2|D1|D0**	Channel 2	**0000_0000:Min**	**1111_1111:Max**
				RECOMMENDED	*TBD*
CH1_LASER_DIS	*0x6299*	**x|x|x|x|x|x|x|x|**	Channel1	**D4 = 1: Disable (Default)**	

		x|x|x|D4|x|x|x|x		D4 = 0: Enable
CH2_LASER_DIS	*0x6299*	x|x|x|x|x|x|x|x| x|x|D5|x|x|x|x|x	Channel 2	D5 = 1: Disable (Default) D5 = 0: Enable
CH1_APC_EN	*0x6299*	x|x|x|x|x|x|x|x| x|D6|x|x|x|x|x|x	Channel 1	D6 = 0: Manual mode (Default) D6 = 1: Automatic mode
CH2_APC_EN	*0x6299*	x|x|x|x|x|x|x|x| D7|x|x|x|x|x|x|x	Channel 2	D7 = 0: Manual mode (Default) D7 = 1: Automatic mode

1.6 Laser MPD Monitor and Laser Bias Monitor

For each channel, the laser MPD voltage can be independently read from CHx_MPD_MON register. The range that can be read is from 0 to 2.8 V. For each channel, the laser bias voltage can be independently read from CHx_LASER_MON register. The range that can be read is from 0 to 2.8 V.

Register Name	Address	Register Settings	Channel	Description
CH1_MPD_MON	*0x6111*	x|x|x|x|x|x|x|x|D7|D6| D5|D4|D3|D2|D1|D0	Channel 1	Read only Min: 0000_0000 Max: 1111_1111
CH2_MPD_MON	*0x6112*	x|x|x|x|x|x|x|x|D7|D6| D5|D4|D3|D2|D1|D0	Channel 2	
CH1_LASER_MON	*0x6113*	x|x|x|x|x|x|x|x|D7|D6| D5|D4|D3|D2|D1|D0	Channel 1	Read only Min: 0000_0000 Max: 1111_1111
CH2_LASER_MON	*0x6114*	x|x|x|x|x|x|x|x|D7|D6| D5|D4|D3|D2|D1|D0	Channel 2	

1.7 Common Mode

For each channel, the common mode voltage between driver and modulator can be independently read from CHx_VCOMMON register.

Register Name	Address	Register Settings	Channel	Description
CH1_VCOMMON	*0x6211*	x|x|x|x|x|x|x|x|D7|D6| D5|D4|D3|D2|D1|D0	Channel 1	Read only Min: 0000_0000 Max: TBD
CH2_ VCOMMON	*0x6212*	x|x|x|x|x|x|x|x|D7|D6| D5|D4|D3|D2|D1|D0	Channel 2	
CH3_ VCOMMON	*0x6213*	x|x|x|x|x|x|x|x|D7|D6| D5|D4|D3|D2|D1|D0	Channel 3	
CH4_ VCOMMON	*0x6214*	x|x|x|x|x|x|x|x|D7|D6| D5|D4|D3|D2|D1|D0	Channel 4	
CH5_VCOMMON	*0x628D*	x|x|x|x|x|x|x|x|D7|D6| D5|D4|D3|D2|D1|D0	Channel 5	
CH6_ VCOMMON	*0x628E*	x|x|x|x|x|x|x|x|D7|D6| D5|D4|D3|D2|D1|D0	Channel 6	
CH7_ VCOMMON	*0x628F*	x|x|x|x|x|x|x|x|D7|D6| D5|D4|D3|D2|D1|D0	Channel 7	
CH8_ VCOMMON	*0x6290*	x|x|x|x|x|x|x|x|D7|D6| D5|D4|D3|D2|D1|D0	Channel 8	

1.8 Gain control

For each channel, the gain can be controlled independently using CHx_VGC or CHx_VAGC register. The range that can be set is from 0 to 2.8 V. CHx_VAGC is for automatic gain control. The gain control mode can be set independently by CH_VGC_EN register.

Register Name	Address	Register Settings	Channel	Description
CH_VGC_EN	*0x6099*	**x|x|x|x|x|x|x|x|D7|D6|D5|D4|D3|D2|D1|D0**	1-8	**D0 = 1: CH1 Manual mode** **D1 = 1: CH2 Manual mode** **D2 = 1: CH3 Manual mode** **D3 = 1: CH4 Manual mode** **D4 = 1: CH5 Manual mode** **D5 = 1: CH6 Manual mode** **D6 = 1: CH7 Manual mode** **D7 = 1: CH8 Manual mode**

Register Name	Address	Register Settings	Channel	Description	
CH1_VAGC	*0x6008*	**x|x|x|x|x|x|x|x|D7|D6|D5|D4|D3|D2|D1|D0**	Channel 1	**0000_0000 : Min**	**1111_1111 : Max**
				RECOMMENDED	*TBD*
CH2_VAGC	*0x6086*	**x|x|x|x|x|x|x|x|D7|D6|D5|D4|D3|D2|D1|D0**	Channel 2	**0000_0000 : Min**	**1111_1111 : Max**
				RECOMMENDED	*TBD*
CH3_VAGC	*0x6106*	**x|x|x|x|x|x|x|x|D7|D6|D5|D4|D3|D2|D1|D0**	Channel 3	**0000_0000 : Min**	**1111_1111 : Max**
				RECOMMENDED	*TBD*
CH4_VAGC	*0x6186*	**x|x|x|x|x|x|x|x|D7|D6|D5|D4|D3|D2|D1|D0**	Channel 4	**0000_0000 : Min**	**1111_1111 : Max**
				RECOMMENDED	*TBD*
CH5_VAGC	*0x6206*	**x|x|x|x|x|x|x|x|D7|D6|D5|D4|D3|D2|D1|D0**	Channel 5	**0000_0000 : Min**	**1111_1111 : Max**
				RECOMMENDED	*TBD*
CH6_VAGC	*0x6286*	**x|x|x|x|x|x|x|x|D7|D6|D5|D4|D3|D2|D1|D0**	Channel 6	**0000_0000 : Min**	**1111_1111 : Max**
				RECOMMENDED	*TBD*
CH7_VAGC	*0x6306*	**x|x|x|x|x|x|x|x|D7|D6|D5|D4|D3|D2|D1|D0**	Channel 7	**0000_0000 : Min**	**1111_1111 : Max**
				RECOMMENDED	*TBD*
CH8_VAGC	*0x6386*	**x|x|x|x|x|x|x|x|D7|D6|D5|D4|D3|D2|D1|D0**	Channel 8	**0000_0000 : Min**	**1111_1111 : Max**
				RECOMMENDED	*TBD*
CH1_VGC	*0x6009*	**x|x|x|x|x|x|x|x|D7|D6|D5|D4|D3|D2|D1|D0**	Channel 1	**0000_0000 : Min**	**1111_1111 : Max**
				RECOMMENDED	*TBD*
CH2_VGC	*0x6087*	**x|x|x|x|x|x|x|x|D7|D6|D5|D4|D3|D2|D1|D0**	Channel 2	**0000_0000 : Min**	**1111_1111 : Max**
				RECOMMENDED	*TBD*
CH3_VGC	*0x6107*	**x|x|x|x|x|x|x|x|D7|D6|D5|D4|D3|D2|D1|D0**	Channel 3	**0000_0000 : Min**	**1111_1111 : Max**
				RECOMMENDED	*TBD*
CH4_VGC	*0x6187*	**x|x|x|x|x|x|x|x|D7|D6|D5|D4|D3|D2|D1|D0**	Channel 4	**0000_0000 : Min**	**1111_1111 : Max**
				RECOMMENDED	*TBD*
CH5_VGC	*0x6207*	**x|x|x|x|x|x|x|x|D7|D6|D5|D4|D3|D2|D1|D0**	Channel 5	**0000_0000 : Min**	**1111_1111 : Max**
				RECOMMENDED	*TBD*
CH6_VGC	*0x6287*	**x|x|x|x|x|x|x|x|D7|D6|D5|D4|D3|D2|D1|D0**	Channel 6	**0000_0000 : Min**	**1111_1111 : Max**
				RECOMMENDED	*TBD*
CH7_VGC	*0x6307*	**x|x|x|x|x|x|x|x|D7|D6|D5|D4|D3|D2|D1|D0**	Channel 7	**0000_0000 : Min**	**1111_1111 : Max**
				RECOMMENDED	*TBD*

CH8_VGC	*0x6387*	x|x|x|x|x|x|x|x| D7|D6|D5|D4|D3|D2|D1|D0	Channel 8	**0000_0000 : Min**	**1111_1111 : Max**
				RECOMMENDED	*TBD*

1.9 Peak Detector

For each channel, the peak to peak voltage can be independently read from CHx_VPK register.

Register Name	Address	Register Settings	Channel	Description
CH1_VPK	*0x618D*	x|x|x|x|x|x|x|x|D7|D6| D5|D4|D3|D2|D1|D0	Channel 1	**Read only** **Min: 0000_0000** **Max: TBD**
CH2_ VPK	*0x618E*	x|x|x|x|x|x|x|x|D7|D6| D5|D4|D3|D2|D1|D0	Channel 2	
CH3_ VPK	*0x618F*	x|x|x|x|x|x|x|x|D7|D6| D5|D4|D3|D2|D1|D0	Channel 3	
CH4_ VPK	*0x6190*	x|x|x|x|x|x|x|x|D7|D6| D5|D4|D3|D2|D1|D0	Channel 4	
CH5_VPK	*0x620D*	x|x|x|x|x|x|x|x|D7|D6| D5|D4|D3|D2|D1|D0	Channel 5	
CH6_ VPK	*0x620E*	x|x|x|x|x|x|x|x|D7|D6| D5|D4|D3|D2|D1|D0	Channel 6	
CH7_ VPK	*0x620F*	x|x|x|x|x|x|x|x|D7|D6| D5|D4|D3|D2|D1|D0	Channel 7	
CH8_ VPK	*0x6210*	x|x|x|x|x|x|x|x|D7|D6| D5|D4|D3|D2|D1|D0	Channel 8	

1.10 LOS

The LOS/SD mode can be set using LOS_SEL. The status of LOS/SD can be read independently from LOS_SD register. The LOS threshold control voltage can be set by using LOS_TH register. The hysteresis range can be set by using HYS register.

Register Name	Address	Register Settings	Channel	Description	
LOS_TH	*0x611A*	x|x|x|x|x|x|x|x|D7|D6| D5|D4|D3|D2|D1|D0	1-8	**0000_0000 : Min**	**1111_1111 : Max**
				RECOMMENDED	*TBD*
HYS	*0x6119*	x|x|x|x|x|x|x|x|x| x|x|D3|D2|D1|D0	1-8	**0000 : Min**	**1111 : Max**
				RECOMMENDED	*TBD*
LOS_SEL	*0x6119*	x|x|x|x|x|x|x|x|D7|x| x|x|x|x|x|x	1-8	**D7 = 1: SD mode** **D7 = 0: LOS mode**	
LOS_SD	*0x6003*	x|x|x|x|x|x|x|x|D8|D7|D6| D5|D4|D3|D2|D1|D0	1-8	**D0 = 1: CH1 LOS/SD** **D1 = 1: CH2 LOS/SD** **D2 = 1: CH3 LOS/SD** **D3 = 1: CH4 LOS/SD** **D4 = 1: CH5 LOS/SD** **D5 = 1: CH6 LOS/SD** **D6 = 1: CH7 LOS/SD** **D7 = 1: CH8 LOS/SD** **D8 = 1: At least one CH LOS/SD**	

1.11 Auto Squelch

For each channel, the auto squelch function can be set by using SQ_EN register. When it is enabled and LOS_SD register is 1, channel will be shutdown.

Register Name	Address	Register Settings	Channel	Description
SQ_EN	*0x601C*	**x|x|x|x|x|x|x|x|D7|D6|D5|D4|D3|D2|D1|D0**	1-8	**D0 = 1: CH1 auto squelch enabled** **D1 = 1: CH2 auto squelch enabled** **D2 = 1: CH3 auto squelch enabled** **D3 = 1: CH4 auto squelch enabled** **D4 = 1: CH5 auto squelch enabled** **D5 = 1: CH6 auto squelch enabled** **D6 = 1: CH7 auto squelch enabled** **D7 = 1: CH8 auto squelch enabled**

Revision History

Revision Information	Release Date	Description
V1	Aug 28, 2024	Advanced version release