Electronic-Photonic Co-design for Next Generation Optical Transceivers

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Abstract: Recent advances in monolithically integrated energy efficient high data-rate optical receivers, transmitters, and WDM light sources are presented and opportunities and challenges of next generation optical transceivers are discussed. © 2025 The Author(s)

1. Introduction

Energy efficient high data-rate optical interconnects are essential for today's data centers and AI systems. Wavelength-division multiplexing (WDM) is a key technology for achieving beyond Tb/s data-rates in such optical links. Such systems typically consist of a multi-carrier optical source such as a frequency comb or a laser array, a transmitter, and a receiver. While the multi-carrier source is often implemented as a separate module, the transmitter and receiver units are implemented using hybrid or monolithic integration approaches, where in the former, separate electronic and photonic chips are packaged, and in the latter, electronic and photonic devices are integrated on the same chip. In hybrid approach, state-of-the-art CMOS electronics and silicon photonic platforms can be used [1] but often at the cost of complex chip-to-chip packaging and reduced energy efficiency and per channel data-rate due to packaging parasitics. Monolithic approach using advanced silicon photonics enabled CMOS platforms offer reduced packaging complexity and parasitics and can lead to a higher energy efficiency for a higher data-rate per channel. In this paper, the design considerations of multi-wavelengths optical sources and the recent advances in the design of monolithically implemented optical transceivers for the next generation of optical interconnects are discussed.

2. Design considerations and trade-offs

Figure 1(a) shows the simplified block diagram of a typical NRZ WDM single-fiber link. A multi-wavelength light source (e.g. a Kerr frequency comb, mode-locked laser, or laser array) is coupled to the optical transmitter (OTX), where carriers are separated using an optical demultiplexer, modulated (e.g. using ring or disk modulators) by different bit-streams, and multiplexed back to a single output using a multiplexer. The OTX output is coupled to a single-mode fiber and delivered to the optical receiver (ORX), where modulated carriers are separated using a demultiplexer and demodulated using photodiodes followed by trans-impedance amplifiers (TIA) and limiting amplifiers (LA).

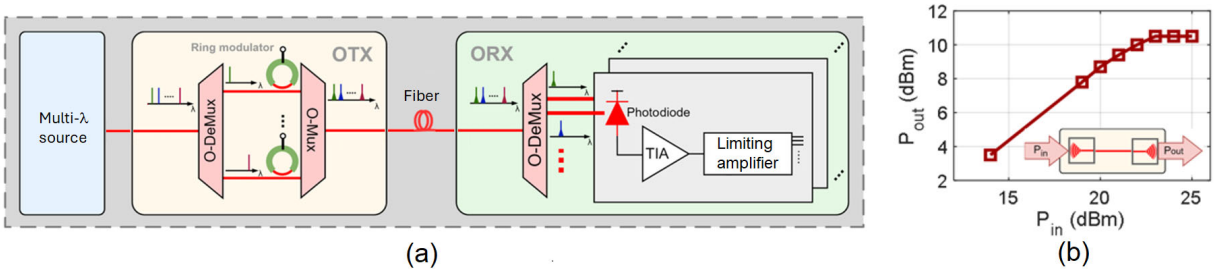

Figure 1. (a) Simplified block diagram of a typical NRZ WDM system. (b) Two-photon absorption effect and power saturation in a silicon GC-waveguide-GC structure implemented on GF45PCLO process.

Given the sensitivity of the ORX (typically limited by the photodiode shot noise and receiver noise), a minimum level of OMA per carrier is needed for error-free operation. Considering the coupling loss between the fiber and the chips, the modulation extinction ratio, and loss of components on the OTX and assuming a high enough optical SNR of the carriers, a minimum level of optical power per carrier, P_o, is needed for error-free operation. As a result, the total power of the optical signal at the input of the OTX for N carriers needs to be NP_o. The maximum achievable per carrier data-rate, d, is limited by the f_{max} of the electronics and the maximum bandwidth of the photodiodes and modulators. The maximum coupled power through the grating coupler (GC) or edge coupler (EC) on the silicon chip, P_{max}, is limited by the two-photon absorption (and depending on the platform, other non-linear effects). Therefore, the maximum number of carriers is written as $N=P_{max}/P_o$ and the total aggregate link data-rate, D, is set as $D = dP_{max}/P_o$. Figure 1(b) shows the measured optical power at the output of a silicon GC-waveguide-GC structure implemented on

GlobalFoundries GF45CLO process as a function of the input power. Note that the loss of a single GC in this structure is about 5 dB.

To overcome the aggregate data-rate limit set by the maximum coupled power to the OTX, besides reducing the optical loss (including the coupling loss) and utilizing error-correction and digital processing techniques, the input stage of the OTX could be implemented using silicon nitride (or similar materials) with a negligible two-photon absorption and a high power-handling. Note that using multiple grating or edge couplers in a multi-fiber link approach may increase the packaging complexity and cost, and its scalability limitations should also be considered.

A laser array [2] or an optical frequency comb [3] can serve as the multi-wavelength carrier source. Comb sources offer several advantages, including a smaller footprint, lower power consumption for thermal stabilization, and inherently polarization-matched channels, eliminating the need for additional per-channel polarization-adjustment. However, laser arrays provide greater control over individual carrier wavelengths and power levels, making it easier to realize a multi-wavelength source with a flat spectral response. Additionally, laser arrays offer higher reliability; if a single laser fails, only a fraction of the link is affected, whereas with a comb source, failure of the source can result in the loss of the entire link.

Optical demultiplexers (O-DeMux) within OTX and ORX chips and the optical multiplexer (O-Mux) within OTX chip are essential components of a WDM link, that should be designed to provide sufficient channel-to-channel isolation (to prevent crosstalk) while introducing a small insertion loss. The O-DeMux/O-Mux blocks typically consist of one or more wavelength-selective optical filters, which need to be frequency aligned to the target frequency grid (i.e. the carriers) and be tuned to compensate for process and temperature variations to ensure error-free operation. Thermally tuned Mach-Zehnder interferometers (MZIs) or ring resonators have been commonly used as the core building blocks for the O-DeMux and O-Mux systems [1, 4]. However, despite large tuning range, thermal tuning often results in reduced link energy-efficiency when utilized in O-DeMux/O-DeMux systems with a large number of channels. Additionally, thermal crosstalk makes the independent tuning and control of different channels rather challenging.

Monolithic integration of optical transceivers on photonics-enabled CMOS processes (such as GlobalFoundries 9WG and 45CLO) allows for use of the thin gate oxide layer for implementation of semiconductor-insulator-semiconductor capacitor (SISCAP) optical phase shifters. The structure of a fabricated SISCAP phase shifter is depicted in Fig. 2(a), where the optical mode is formed within a vertically stacked silicon, thin oxide, and polysilicon layer configuration [5]. In such a device, there is an overlap between the optical mode and the charge profile within the capacitor and by changing the applied voltage across the capacitor, the effective index can be changed resulting in an optical phase shift at a zero static power consumption.

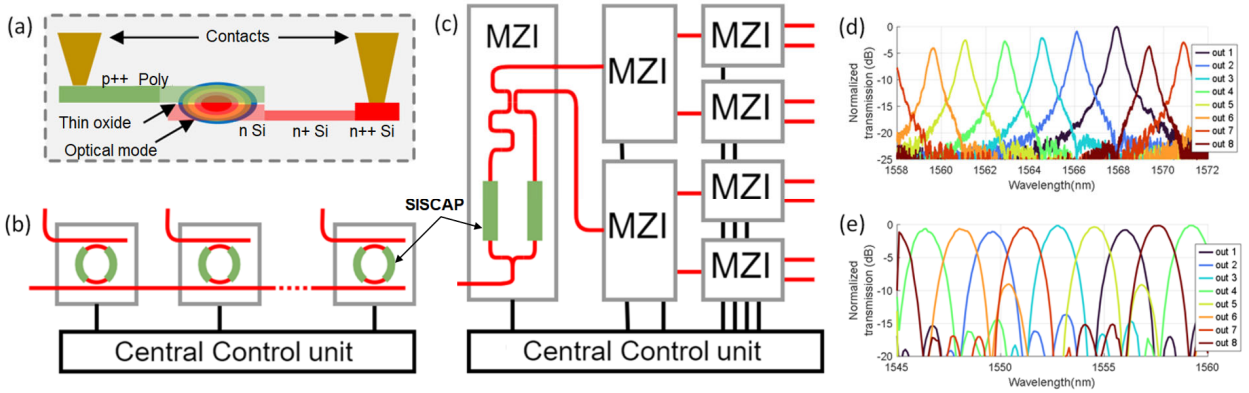

Figure. 2. (a) Cross-section of a SISCAP phase shifter. (b) Block diagram of a monolithic 1:8 cascaded ring resonator O-DeMux. (c) Block diagram of a monolithic 1:8 MZI-based O-DeMux. (d) Optical response of the 8-channel capacitively tuned ring resonator-based O-DeMux, and (e) the optical response of the 8-channel capacitively tuned MZI-based O-DeMux.

Figures 2(b) and 2(c) show the block diagram of fully integrated 8-channel O-Mux/O-DeMux systems based on cascaded drop ring resonators and unbalanced MZI tree, respectively [5]. Both designs are capable of autonomous locking to and tracking of the source carrier wavelengths using capacitive tuning, where a central control unit sequentially selects each channel, and its SISCAP phase shifter is tuned in a feedback loop to lock the response of the selected channel to the corresponding target wavelength. Figures 2(d) and 2(e) present the DeMux optical response for the ring resonator-based and the MZI-based systems, respectively. The entire O-DeMux/O-Mux block consumes only 2.4 mW of static power for sequential tuning (only by the control unit), corresponding to an energy efficiency of 10 fJ/bit for an 8-channel WDM system at a data-rate of 32 Gb/s per channel.

Figure 3(a) shows the structure of the two section micro-ring modulator (MRM) used to implement the monolithic OTX chip. The MRM has a p-n section (Fig. 3(b)) for high frequency modulation and a capacitive section (Fig. 3(c)) used to tune and lock the MRM to the corresponding carrier wavelength. The heater within the MRM is only used in unlikely cases where the capacitive tuning range is insufficient for locking the MRM to the target wavelength. Figure 3(d) shows the block diagram of the monolithically integrated OTX, where the output of the on-chip PRBS generator

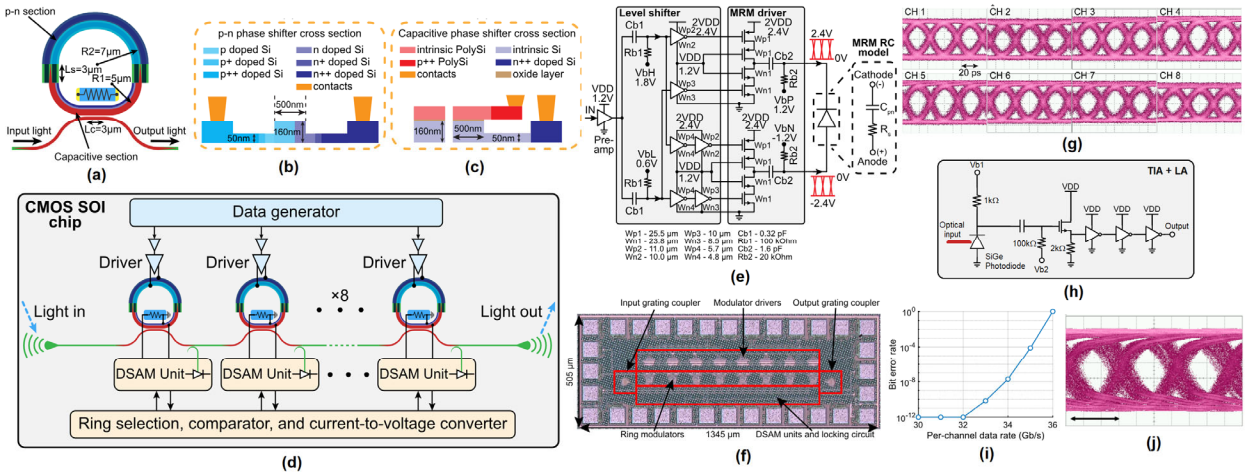

Figure 3. (a) The top view of the implemented MRM structures with (b) p-n and (c) capacitive sections. (d) Block diagram of the monolithically integrated optical transmitter based on 2-section p-n/capacitive micro-ring modulators. (e) Schematic of the pre-driver and MRM driver. (f) Micrograph of the 8 channel OTX implemented using GlobalFoundries 45CLO process. (g) Eye diagrams of all 8 channels at per-channel data rate of 32 Gb/s. (h) Schematic of a channel of the low power receiver. (i) Measured BER versus per-channel data rate at 5 dBm optical power at the modulator input, and (j) the typical eye-diagram of the 32Gb/s low power receiver. DSAM: dual sensing, actuation, and memory.

is routed to 8 MRMs modulating the corresponding carriers [6]. Figure 3(e) shows the schematic of the on-chip pre-driver and MRM driver. The MRM driver stage consists of stacked two pMOS and two nMOS transistors, increasing the output voltage swing to improve the modulation index without overstressing the transistors. Figure 3(f) shows the micrograph of the 8 channel OTX implemented using GlobalFoundries 45CLO process within a footprint of 0.68mm^2. Figure 3(g) shows the measured photo-detected eye diagrams at 32 Gb/s per-channel for all 8 channels at BER<10^{-12}. The eye diagrams are measured while all channels are electrically driven concurrently. The energy efficiency of the MRM, including capacitive wavelength tuning and locking, is 63 fJ/bit at 32 Gb/s/channel and 15 fJ/bit at 5Gb/s/channel for a BER <10^{-12}. The energy efficiency of the 8 channel OTX is 328 fJ/b at 32 Gb/s (for the aggregate data-rate of 256Gb/s) and 113 fJ/b at 10 Gb/s for a BER <10^{-12}. Figure 3(i) depicts the measured BER versus per-channel data-rate when the optical power at the MRM input is set to 5 dBm.

Figure 3(h) shows the schematic of one channel of the ORX. The SiGe photodiode output is converted to a voltage using a passive trans-impedance amplifier (TIA), a resistor. The voltage across the resistor is buffered using a source follower structure and is further amplified to digital logic levels using 3 stages of inverters forming a limiting amplifier (LA). The typical detected eye-diagram at the output of one channel of ORX at 32Gb/s is shown in Fig. 3(j), where an energy efficiency of 55 fJ/b is achieved.

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