Theoretical Analysis of Energy Efficiency and Bandwidth Limit of Silicon Photonic Modulators

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***Abstract*—Parallel optical interconnects at the extreme scale hold the key to resolve the grand challenge of moving enormous amount of data between on-chip cores and within multi-chip modules. Silicon photonic modulators, as one of the most pivotal devices conducting electronic to photonic signal conversion, must excel in energy efficiency and bandwidth density in order to meet the stringent requirement of extreme scale photonic interconnects. In this manuscript, the energy efficiency and bandwidth limit of ultra-compact resonator-based silicon photonic modulators are analyzed from three fundamental perspectives: free carrier dispersion strength of the active materials, Purcell factors of the resonators, and electrical configuration of the capacitors. Our simulation results reveal convincing advantages of photonic crystal nanocavity over micro-ring and micro-disk resonators in terms of energy efficiency and device footprint. While for the electro-optic modulation region, metal-oxide-semiconductor (MOS) capacitors truly outperform reversed PN junctions due to the large capacitance density. However, all resonator-based silicon photonic modulators suffer the intrinsic trade-off between energy efficiency and resistance-capacitance-delay limited bandwidth. The general model developed herein lays the theoretical foundation and identify possible routes to achieve atto-joule per bit energy efficiency and how to approach the bandwidth limit of silicon photonic modulators.**

***Index Terms*—Electro-optic modulators, optical interconnects, optical resonators, plasma dispersion effect, silicon photonics.**

I. Introduction

As CLOCK frequency scaling ended in the mid-2000s, the microelectronics industry has progressively embraced parallel computing architecture to sustain performance improvement. Parallel architectures are now pervasive across most high-performance electronic devices. For example, a NVIDIA Tesla V100 includes up to 100 central process units (CPUs) with 5120 cores in a single graphic process unit (GPU), which can achieve 125 teraflops computation but requires GPU-to-memory bandwidth close to 10 terabits per second (Tbps) [1]. The benefits of parallel computing systems, however, are currently constrained not by the limits of computation at individual nodes, but by the interconnect bottleneck, namely, how to move data between nodes with high energy efficiency. Although photonics technologies have been widely agreed as the most essential solution to resolve the interconnect bottleneck, existing optical input/output (I/O) that has taken the form of pluggable modules on circuit boards cannot completely resolve the challenge due to their high power dissipation and low areal bandwidth density limit. Photonic integrated circuits (PICs) with high density parallel data links have the capacity to meet the high bandwidth density requirement of parallel computing systems. Nevertheless, PIC-based optical interconnects are also facing the same challenge in energy efficiency and bandwidth limit as electrical interconnects because the margin shrinks unfavorably for shorter distance optical interconnects. D. Miller pointed out that the key question is whether optics can reduce energy to atto-joule per bit level in interconnects inside cabinets, racks, and circuit boards, down at least to the edges of the chips themselves, and possibly even on the chip [2]. This unprecedented requirement in energy efficiency poses tremendous challenges to existing PIC devices, even to the state-of-the-arts silicon photonics.

The development of silicon photonics in the past two decades offers the most feasible platform to fulfill parallel optical interconnects due to its inherent CMOS compatibility. As III-V compound semiconductor light sources can be off-chip coupled or heterogeneously integrated [3]–[6], and Si/Ge photodetectors can potentially be directly powered by the signal light [7], electro-optic (E-O) modulators becomes one of the most critical active devices that will consume the biggest portion of the on-chip power in the optics module, especially for high-speed high-density parallel optical links. Considering the system level integration with microelectronics, our investigation of energy-efficient, high-speed E-O modulators will only focus on devices that are compatible with silicon photonics. While there have been very encouraging progresses on III-V compound semiconductors [8]–[12], plasmonics [13]–[20], $LiNbO_3$ [21]–[24], and E-O polymer platforms with high bandwidth and high energy efficiency [17], [19], [25]–[29], we will refrain from discussing these devices due to the completely different working mechanism. The energy efficiency and scaling laws of broad type modulators have been reviewed by a few excellent papers recently [2], [30]–[34].

For every E-O modulator, the performance is ultimately determined by three main factors: active materials, photonic device design, and electrical structure. Due to the intrinsic symmetric crystalline structure, silicon does not have the Pockel effect. Silicon photonic modulators either have to use the free carrier

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plasma dispersion effect from silicon itself or take advantage of the E-O effects from heterogeneously integrated materials such as germanium [35]–[39], E-O polymers [25]–[29], ferroelectric materials [40]–[43], transparent conductive oxides (TCOs) [44]–[48], graphene and 2-D materials [49]–[55], and most recently phase change materials [56]–[61]. Again, these emerging materials offer very unique, and often very large E-O effects but are very difficult to conduct rigorous analysis of the energy efficiency and bandwidth limit because of the inconsistency of the material properties. On the other hand, the majority of the reported E-O modulators are based on the refractive index perturbation induced by free carrier plasma dispersion effect from silicon or heterogeneously integrated materials. Therefore, the scope of this manuscript is limited to free-carrier-driven silicon E-O modulators, including silicon modulators with heterogeneously integrated materials.

From the photonic device perspective, an E-O modulator requires either Mach-Zehnder interferometer (MZI) or resonator structure to convert the phase modulation from refractive index perturbation to amplitude modulation. Conventional MZI based E-O modulators are mature, however, not suitable for on-chip interconnects due to the large footprint usually in hundreds of microns in length and the relative large energy consumption above pico-joule per bit [62]. Even considering the slow light effect such as photonic crystal waveguides to enhance the performance of MZI modulators, the reduction in size and energy consumption is still not comparable to micro-resonators [63]–[65]. Instead, resonator-based E-O modulators have been widely accepted as the most energy-efficient devices for future on-chip optical interconnects. By enhancing the light-matter interaction inside a high-quality factor (Q-factor) micro-resonator, such as micro-ring [6], [7], [74]–[78], [66]–[73], micro-disk [79]–[82] or photonic crystal (PC) nanocavity [47], [48], [83]–[85], a resonator-based E-O modulator occupies ultra-compact device footprint and can achieve both high speed operation and low energy consumption. In addition, micro-resonators can work as multiplexers/de-multiplexers as well allowing high density optical network-on-chip system [74], [75], [86]. The first microprocessor that communicates with on-chip photonic interconnect link has been demonstrated by C. Sun, *et al.* in 2015 using micro-ring modulators for the E-O modulation [9].

There are three electrical structures for silicon E-O modulators: forward biased p-i-n diode using carrier injection, reverse biased p-n junction based on carrier depletion, and metal-oxide-semiconductor (MOS) capacitor based on carrier accumulation. Among these electrical structures, p-i-n diode can induce large index changing through heavy carrier injection. However, it is not suitable for future optical interconnects due to two major drawbacks: slow minority-carrier-lifetime-limited operation speed (only a few GHz) and large static energy consumption under forward bias. Therefore, we will constrain our comparison between reverse biased p-n junction and MOS capacitor silicon E-O modulators, which can potentially reach atto-joule/bit energy efficiency and greater than 10 GHz bandwidth.

As an explicit statement, this manuscript will provide in-depth analysis and objective comments of resonator-based E-O modulators on silicon photonic platform driven by free carriers, the scope of which is defined by comprehensive consideration of device footprint, energy efficiency, bandwidth, fabrication processes, and compatibility with silicon photonics and CMOS circuits. The manuscript is organized in the following sequence. First, we review the free carrier dispersion effect of different active materials in Section II, which proves that many heterogeneously integrated E-O modulators should have higher E-O modulation efficiency than pure silicon photonic modulators. In Section III, we comprehensively analyze the energy efficiency of E-O modulation, showing that the carrier dispersion strength, the Purcell factor of the resonator and the total capacitance are the three prime parameters to improve the energy efficiency. Based on that, we propose new design schemes to push the energy efficiency boundary into the atto-joule per bit range by utilizing high Purcell factor resonators—PC nanocavities with hybrid silicon MOS capacitors. In Section IV, we evaluate the bandwidth of the resonator E-O modulators from the perspective of Q-factor and RC delay due to the electrical structure of the device. In addition, the trade-off between the energy efficiency and bandwidth is outlined. In Section V, we discuss two other main sources of power dissipation which play dominate roles in practical PICs: wavelength control and driving electronic circuits. At last in Section VI, we conclude this manuscript with our perspectives toward future high-speed atto-joule/bit E-O modulators.

II. Free Carrier Dispersion Effects of Various Semiconductor Materials

The relationship between free carriers and semiconductor permittivity can be described by the well-known Drude model:

$$\varepsilon_r = \varepsilon_\infty - \frac{\omega_p^2}{\omega(\omega + i\Gamma)} \tag{1}$$

where ε_r is relative permittivity of the semiconductor, ε_∞ is the high-frequency permittivity, Γ is the collision frequency. The critical term here is the plasma frequency ω_p^2, which is proportional to the free carrier density N_c by $\omega_p^2 = N_c q^2/\varepsilon_0 m^*$, where ε_0 is the vacuum permittivity, q is the electron charge and m^* is the carrier effective mass. Then we can have the relationship between the relative permittivity perturbation $\Delta\varepsilon/\varepsilon$ and the change of free carrier density ΔN_c:

$$\frac{\Delta\varepsilon}{\varepsilon} = -\frac{\Delta N_{\boldsymbol{c}} q^2}{\varepsilon_0 \varepsilon_{\boldsymbol{r}} m^*} \frac{1}{\omega(\omega + i\Gamma)} \approx -\frac{\Delta N_{\boldsymbol{c}} q^2}{\varepsilon_0 \varepsilon_{\boldsymbol{r}} m^*} \frac{1}{\omega^2} \tag{2}$$

To simplify the discussion, we ignore the imaginary part here for two reasons. First, the major modulation of a resonator-based E-O modulator comes from the resonance peak shift, which is due to real part of permittivity change. Second, in most cases the collision frequency ($10^{12} \sim 10^{13}$ Hz) in the imaginary part, which is determined by the carrier mobility μ, is much smaller than the optical frequency (1.93×10^{14} Hz for 1.55 μm wavelength). To be mentioned here, the E-O efficiency of MZI modulators is determined by the absolute change of the refractive index, which corresponds to the phase shift per unit length waveguide. However, for an optical resonator working at the resonance wavelength, the material permittivity and device

TABLE I
PARAMETERS FOR TYPICAL ACTIVE MATERIALS

material	Type	ε_r	Mobility (cm^2/Vs)[a]	Effective mass (m_0)	N_{ENZ} ($\times 10^{20}$ cm^{-3})
n-Si	IV group	12.1	720	0.26	19.75[b]
p-Si	IV group	12.1	290	0.37	9.78[b]
n-Ge	IV group	8.8	1000	0.12	4.93
n-InGaAsP [10], [107]	III-V group	10.65	1800	0.06	2.98
n-InP [10], [107]	III-V group	9.95	2000	0.08	3.71
ITO [108]	TCO	3.9	28	0.35	6.37
CdO [109], [110]	TCO	5.3	205	0.24	5.93
Graphene [88]	2D material	9.03	1000 [111]	~	1.33

[a]Mobilities of IV and III-V group semiconductors listed here are considered with carrier density of 1×10^{18} cm^{-3}; mobilities of TCOs are considered with carrier density of $\sim 1 \times 10^{20}$ cm^{-3}; mobility of graphene is under condition when in-plane permittivity reach maximum (Fermi level $\mu_c = 0.4eV$).
[b]N_{ENZ} for silicon is calculated using the carrier dispersion coefficient K from (4) at doping level of 2.5×10^{18} cm^{-3}.

physical dimension are correlated. The E-O efficiency is actually determined by the relative permittivity perturbation $\Delta\varepsilon/\varepsilon$. Here we define the carrier dispersion coefficient K to describe the strength of the free carrier dispersion effect of a semiconductor material:

$$K = -\frac{\partial \Delta\varepsilon/\varepsilon}{\partial \Delta N_c q} = \frac{q}{\varepsilon_0 \varepsilon_r m^* \omega^2} = \frac{1}{qN_{ENZ}} \tag{3}$$

The physics meaning of K can be revealed by rewriting it into the fourth term of (3), where $N_{ENZ} = \varepsilon_0 \varepsilon_r m^* \omega^2 / q^2$ indicates the carrier concentration that is required to reduce the real part of permittivity to zero, or in other word, to reach epsilon-near-zero condition (ENZ). Table I lists the parameters of some typical carrier-driven active materials that are compatible with silicon photonics platform and the corresponding N_{ENZ} at 1.55 μm according to (3). Fig. 1 shows the carrier dispersion coefficient K of different materials as a function of free carrier density perturbation ΔN_c. From (3) we know that the plasma dispersion is only determined by the free carrier effective mass m^* and the semiconductor permittivity ε_r. N-type III-V semiconductors exhibit 5~6× stronger plasma dispersion effect than n-type silicon due to their small electron effective mass at the Γ point of the conduction band. On the other hand, TCOs exhibit ~3× stronger plasma dispersion which mainly comes from the smaller permittivity due to their wide bandgap. While n-type germanium is between TCOs and III-V semiconductors, which has ~4 enhancement of plasma dispersion benefited from

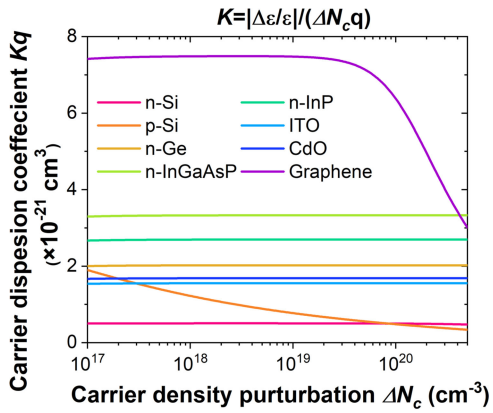

Fig. 1. Carrier dispersion coefficient K of typical active materials as a function of carrier density perturbation ΔN_c.

both slightly smaller permittivity and effective mass at L point. Although Ge-on-Si is usually used for electro-absorption (EA) modulators, it also has the potential to improve the efficiency of a resonator-based E-O modulator. While for p-type semiconductors, due to the similar valence band structures, the difference in hole effective mass is much smaller compared with electron. Therefore, only p-type silicon is listed as the difference is minor. We have to point out that the plasma dispersion model in (2) is simplified. In reality, the permittivity is determined by the complex band structure especially for large band bending. We also did not consider other carrier density-based mechanisms such as band-filling effect [2]. However, the principle of analysis still holds valid when the index perturbation is moderate or the driving voltage is not excessive, which applies to most on-chip E-O modulators. For silicon that serves as the baseline for comparison of various semiconductor materials, we use the more widely accepted model for plasma dispersion given in [87]:

$$\Delta n = -8.8 \times 10^{-22} N_n - 8.5 \times 10^{-18} (N_p)^{0.8} \tag{4}$$

Similarly, we can also define the carrier dispersion coefficient K for graphene. Unlike most bulk semiconductors in which plasma dispersion is dominated by the Drude-like intra-band transitions, 2D material like graphene also exhibits large carrier induced dispersion due to the combined effect of both inter-band and intra-band transitions. The permittivity of graphene can be calculated from its in-plane conductivity given by the Kubo formula [88]:

$$\sigma_P = \frac{iq^2(\omega - i2\Gamma)}{\pi(2\pi h)^2} \times \left[\frac{1}{(\omega - i2\Gamma)^2} \int_0^\infty \varepsilon \left(\frac{\partial f_d(-\varepsilon)}{\partial \varepsilon} - \frac{\partial f_d(\varepsilon)}{\partial \varepsilon} \right) d\varepsilon - \int_0^\infty \frac{f_d(-\varepsilon) - f_d(\varepsilon)}{(\omega - i2\Gamma)^2 - 4(\varepsilon/2\pi h)^2} d\varepsilon \right], \tag{5}$$

$$\varepsilon_P = 1 - \frac{\sigma_\parallel}{i\omega\varepsilon_0 \Delta}. \tag{6}$$

TABLE II
PARAMETERS FOR REPORTED RESONATOR-BASED MODULATORS

Ref	Capacitor /resonator type	Q-factor	V_m ($(\lambda/n_{Si})^3$)	gF_p	C (fF)	E_{bit} (fJ/bit)
[79]	vertical PN junction /micro-disk	9700	4.46	166	20	61
[80]	vertical PN junction /micro-disk	6480	6.82	146.5	17	1
[71]	lateral PN junction /micro-ring	14500	36.29	87.5	50	50
[112]	Si/oxide/Si MOS /micro-ring interleaver	3500	21.20	28	320	180
[66]	PN junction /micro-ring	14500	105.74	29	66	66
[48]	hybrid Si-ITO MOS /PC nanocavity	3700	0.55	855	13	3.25

Here $f_d(\varepsilon) = 1/\{e^{(\varepsilon-\mu_c)/k_BT}+1\}$ is the Fermi-Dirac distribution, μ_c is the Fermi level, h is the plank constant, and $\Delta = 0.35$ nm is the graphene thickness. The first and second term of (5) correspond to the intra-band and inter-band transitions, respectively. When the fermi level μ_c reaches half of the photon energy, the permittivity of graphene reaches maximum as is listed in Table II. Further increasing the Fermi level (increasing carrier density of course), the inter-band absorption in graphene will be prohibited due to Pauli blocking [89], which dramatically decrease the imaginary part of the permittivity. In the meantime, there is a dramatic decrease of the real part of the permittivity due to the Kramers-Kronig relation. The combined effect of both inter-band and intra-band transitions offers the largest carrier dispersion effect enhancement of $\sim$15$\times$ compared with n-Si and the smallest N_{ENZ}. However, an initial bias of graphene is required in order to achieve such huge enhancement. Moreover, the enhancement factor reduces to $\sim$4$\times$ when the inter-band transitions are completely blocked as $\Delta N_c > 10^{20}\,\mathrm{cm}^{-3}$ and the intra-band transition becomes the dominating effect.

III. RESONATOR-BASED MODULATORS

A. General Model of the Energy Efficiency of Resonator-Based Modulators

For a carrier-driven resonator-based modulator, the process to convert electronic signals into coded optical signals can be divided into three steps as illustrated in Fig. 2a. First, the electrical energy is consumed by charging the active capacitor, changing the distribution of free carriers inside the device; next, the modified free carrier distribution changes the local material optical permittivity or refractive index; finally, the change of

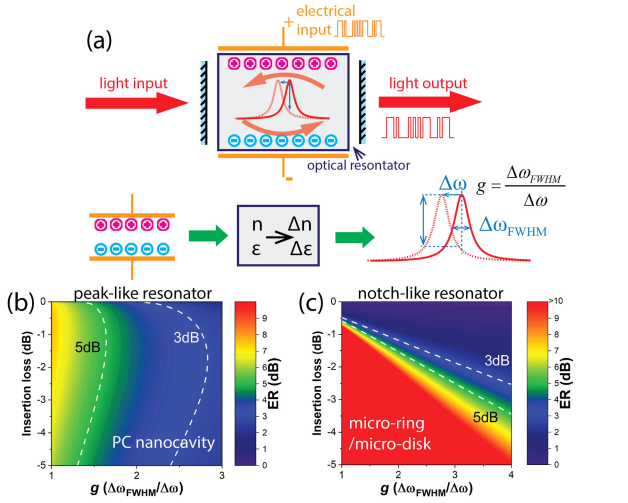

Fig. 2. (a) Principle schematic of a carrier-driven resonator-based E-O modulator. (b) and (c) Extinction ratio as a function of insertion loss and wavelength detuning factor g for peak-like (PC nanocavity) and notch-like (micro-ring/micro-disk) resonator, respectively.

local optical properties detune the resonator, modulating the transmitted optical waves. Considering an optical resonator with a Q-factor of Q operating at the resonant frequency of ω, the resonance detuning $\Delta\omega$ of the resonator can be described by cavity perturbation theory [90]:

$$\Delta\omega = \frac{-\frac{\omega}{2}\int \Delta\varepsilon |E|^2 dv}{\int \varepsilon |E|^2 dv} \tag{7}$$

where ε and $\Delta\varepsilon$ are the distribution of the initial and perturbed permittivity, and E is the electric field distribution of the optical resonance mode. The required resonance detuning to achieve certain extinction ratio (ER) can be expressed as $\Delta\omega = \Delta\omega_{FWHM}/g = \omega/(\mathrm{gQ})$, where wavelength detuning factor g is defined as the ratio of the full width at half maximum (FWHM) of the resonance, $\Delta\omega_{FWHM}$, to the required resonance detuning. This factor depends on the resonator type, whether it has a peak (PC nanocavity) or a notch (micro-ring and micro-disk) in the transmission spectrum, and the target ER. Fig. 2b and 2c plot the ER as a function of the insertion loss (IL) and g factor for peak-type and notch-type resonator, respectively. In the calculation, we assume both resonators having Lorentzian-shape resonance. To simplify the analysis, the effect of carrier absorption is ignored since most resonator modulators only require moderate free carrier concentrations. Generally, a g factor of 1$\sim$2 is required for a reasonable IL. However, for the notch-like resonator, much smaller wavelength detuning is possible by sacrificing the IL.

Then, by plugging (2) and (3) into (7) and considering both n-type (ΔN_e) and p-type (ΔN_h) free carriers, we can rewrite (7) as:

$$\frac{1}{\mathrm{gQ}} = \frac{\Delta\omega}{\omega} = \frac{\int \varepsilon(K_n\Delta N_e + K_p\Delta N_h)q|E|^2 dv}{2V_m \max(\varepsilon|E|^2)} = \frac{\alpha K Q_{tot}}{2V_m} = \frac{\alpha(K_nQ_n + K_pQ_p)}{2V_m} \tag{8}$$

where $K_n = q/\varepsilon_0\varepsilon_r {m_e}^*\omega^2$ and $K_p = q/\varepsilon_0\varepsilon_r {m_h}^*\omega^2$.

Here V_m is the optical mode volume of the resonant mode which is defined as $V_m = \int \varepsilon |E|^2 dv / \max(\varepsilon |E|^2)$ [91]. The overlapping factor $\alpha = [\int \varepsilon(\Delta N_e + \Delta N_h) q |E|^2 dv] / [Q_{tot} \max(\varepsilon |E|^2)]$, describes the overlapping between the carrier distribution perturbation and the optical mode. Based on this definition, the maximum efficiency ($\alpha = 1$) happens when all the free carrier distribution perturbation is induced at the region where the optical field has the maximum electrical energy density. From (8) we can get that the total charge Q_{tot} required to drive the modulator is inversely proportional to the ratio between the Q-factor and the mode volume (Q/V_m), which is more often referred to as the Purcell factor, F_p, which is an intrinsic factor of an optical resonator defined by (10) [92].

$$Q_{tot} = \frac{2V_m}{\alpha K g Q} \propto \frac{V_m}{Q} \propto \frac{1}{F_p} \tag{9}$$

$$F_p = \frac{3}{4\pi^2}\left(\frac{\lambda}{n}\right)^3 \frac{Q}{V_m} \tag{10}$$

Here λ is the resonance wavelength, and n is the refractive index of the semiconductor. Now, bridging the relationship between the free carrier and optical resonator, we analyze the electrical energy consumption. Since every silicon E-O modulator is essentially a capacitor. The energy consumption per bit can be estimated by:

$$E_{bit} = \frac{1}{4} C V^2 = \frac{1}{4} \frac{(Q_{tot}/2)^2}{C} \tag{11}$$

where C is the capacitance of the E-O modulator and V is the operation voltage. Since we have shown that the total charge perturbation Q_{tot} is directly related to the optical modulation, it is more straightforward to consider the energy consumption based on the rightmost side of (8). In a short summary, by plugging (9) and (10) into (11), we can quantitatively calculate the energy efficiency of the E-O modulator:

$$E_{bit} = \frac{9}{64\pi^4}\left(\left(\frac{\lambda}{n}\right)^3 \frac{1}{gF_p}\right)^2 \frac{(qN_{ENZ})^2}{\alpha^2 C} \propto \frac{1}{K^2} \cdot \frac{1}{g^2 F_p^2} \cdot \frac{1}{\alpha^2 C} \tag{12}$$

From (12) it is very clear to see how the three factors can determined the energy consumption of an E-O modulator: the active material determines the carrier dispersion coefficient K; the resonator design determines the Purcell factor F_p and wavelength detuning factor g; and the electrical configuration determines the total capacitance C and the overlapping factor α.

Similarly, we can express the electrical wavelength tunability and the required driving voltage as:

$$\frac{\Delta\lambda}{V} = \lambda\left(\alpha \cdot K \cdot \frac{C}{V_m}\right) \tag{13}$$

$$V = \frac{3}{4\pi^2}\left(\left(\frac{\lambda}{n}\right)^3 \frac{1}{gF_p}\right) \frac{(qN_{ENZ})}{\alpha C} \propto \frac{1}{K} \cdot \frac{1}{gF_p} \cdot \frac{1}{\alpha C} \tag{14}$$

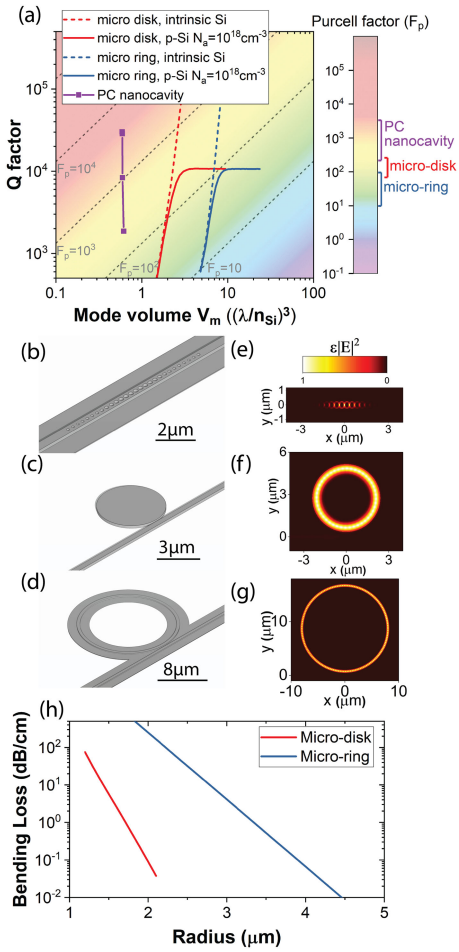

Fig. 3. (a) Simulated Q-factor of the three resonator designs as a function of mode volume V_m. The dashed lines refer to the case of intrinsic silicon when the Q factor is only limited by the bending loss of the micro-disk/micro-ring; and solid lines refer to the case of moderately doped Si with doping level of 10^{18} cm^{-3} when carrier absorption limits the Q factor at large mode volume; (b)–(d) 3D schematics of the PC nanocavity. (b) Micro-disk. (c) Micro-ring. (d) Resonator used in the simulation. (e)–(g) Simulated corresponding electrical energy density distribution of resonators shown in (b)–(d). (h) Simulated bending loss of micro-disks and micro-rings as a function of radius.

B. Micro-Resonator Designs

Three main optical resonator designs have been used for E-O modulators: PC nanocavity, micro-disk and micro-ring. Fig. 3a plots the simulated Q-factor versus the cavity mode volume of these three kinds of resonators. The exact structures in our simulation are illustrated in Fig. 3b–3d. Fig. 3e–3g plot the electrical energy density (εE^2) distribution of the corresponding resonators shown in Fig. 3b–3d. We can directly see the difference in mode volume of these three resonators. For the PC nanocavity, we consider the 1D ridge PC nanobeam cavity design from [84]. We need to point out that there are other more complex PC nanocavity designs that can offer even smaller mode volume [93], [94]. But we limit our analysis to this design due to its design simplicity. Here, two PC mirror segments are placed back to back with air hole size quadratically tapered from the center to the edge of the cavity. The waveguide is 500 nm in width and 250 nm in height, and the slab thickness is 50 nm. The thickness

of the micro-disk resonator is 220 nm used in [80]. The micro-ring resonator has the ridge waveguide cross section in [72] with 500 nm waveguide width, 220 nm waveguide thickness, and 60 nm slab thickness. Because of the rotation symmetry, the micro-disk and micro-ring resonators can be simulated by solving the cross section eigenmode using 2D finite element method (FEM). Then the Q factor can be calculated as [95]: $Q = \pi n_g L\sqrt{ra}/[\lambda(1-ra)]$, where n_g is the group index, L is the round trip length, a is the single-pass amplitude transmission and r is the self-coupling coefficient which equals to a under critical coupling condition. On the other hand, PC nanocavities have to be simulated by 3D finite-difference time-domain (FDTD) method. The Q factor is calculated from the slope of the envelope of the decaying signal. Here, the simulations are conducted by Lumerical MODE and FDTD software, respectively.

The micro-disk and micro-ring resonators are similar to some extent. The Q-factor scales up with the resonator radius due to smaller bending loss (Fig. 3h). However, the whisper-gallery-mode in micro-disk provides better mode confinement compared with the waveguide confinement in micro-ring, micro-disk offers 2.5× smaller mode volume compared with micro-ring to reach the same Q-factor. In principle, ultra-high Q-factor can be achieved in both micro-disk and micro-ring as shown by the dashed lines in Fig. 3a. However, in reality the Q-factor is limited due to many engineering reasons such as surface roughness, carrier absorption, and concerns of photon lifetime. For example, the solids lines in Fig. 3a plot the cases when micro-disk or micro-ring is uniformly p-type doped to carrier density of 10^{18} cm^{-3}, in which the carrier absorption limit the Q-factor to $\sim 10^4$. So typically, a micro-ring resonator gives a Purcell factor less than 100 and a micro-disk resonator exhibits a Purcell factor between 70 and 250.

The Q-factor of the PC nanocavity is majorly limited by the mirror strength of the PC segment which is determined by the number and tapering manner of air holes [96]. In Fig. 3a, three purple dots correspond to the cases with 11, 14 and 17 air holes in each PC mirror segment. We can see that as the Q-factor increases to $\sim 10^4$, the mode volume is almost a constant since the mode volume is only determined by how the air holes are tapered in the center region of the nanocavity. Compared with micro-disk, a PC nanocavity provides 5∼7× reduction in mode volume, thus yielding a Purcell factor from 200 to 4000. Clearly, PC nanocavity surpasses micro-disk and micro-ring resonators in terms of the Purcell factor, which is very crucial for atto-joule/bit E-O modulators.

C. Case Study

Fig. 4a plots the calculated energy consumption per bit of a silicon resonator-based E-O modulator as a function of the effective Purcell factor (gF_p), which includes the effect of wavelength detuning factor g, and total capacitance under maximum overlapping factor condition ($\alpha = 1$) operating at 1.55 μm according to (12). The corresponding regions of different types of resonators are outlined. For better illustration, we also analyze some reported resonator-based silicon E-O modulators from

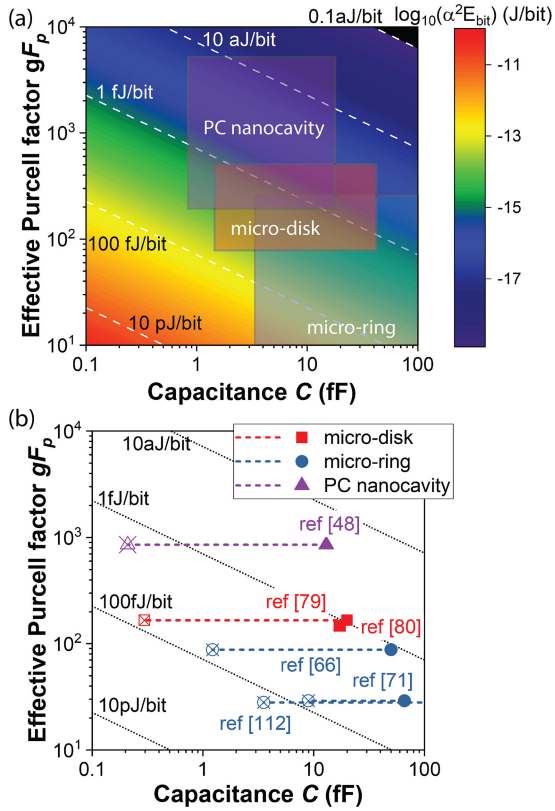

Fig. 4. (a) Energy consumption per bit of a pure silicon resonator-based E-O modulator operating at 1.55 μm as a function of the effective Purcell factor and the capacitance under maximum efficiency condition ($\alpha = 1$). The result is calculated assuming a silicon doping level of 2.5×10^{18} cm^{-3} for both n-type and p-type. The wavelength detuning factor g used to estimated the upper boundary of PC nanocavity, micro-disk and microring are 1.6, 2 and 2.7, respectively. (b) Visualization of the relationship among Purcell factor, total capacitance, overlapping factor and energy efficiency for reported E-O modulators.

literatures by comparing the effective Purcell factor, capacitance, and energy efficiency. The results are summarized in Fig. 4b, which is overlaid on top of Fig. 4a. The solid symbols indicate the theoretical limit of the energy efficiency, which is calculated from the reported capacitance and calculated effective Purcell factor in each reference based on the assumption of perfect overlapping factors. In most cases, however, the capacitor-induced free carrier charge is not perfectly overlapped with the optical mode. Therefore, the reported energy consumption is always higher than the theoretical limit, the results of which are represented by the cross-centered symbols. The overlapping factor can be extracted by $C_{solid}/C_{cross} = 1/\alpha^2$. From this, we can also obtain the effective capacitance that contributes to the E-O modulation as C_{solid}/α.

Parameters for the case study are listed in Table II. We briefly comment on these three different resonator E-O modulators. Micro-ring resonator E-O modulators have been extensively developed [6], [7], [74]–[78], [66]–[73] and can be fabricated using standard silicon photonics foundry. Here we just list some representative examples with different doping configurations. Due to the relative small Purcell factors, the energy efficiency

of micro-ring E-O modulators using on-off key (OOK) signal is typically limited to a few tens of femto-joule per bit. Using more advanced coding techniques such as pulse-amplitude modulation (PAM) can further improve the energy efficiency of micro-ring modulator [72], but may require higher energy for decoding on the receiver side. For the micro-disk E-O modulators, the state-of-the-art experimental demonstration achieved ~1fJ/bit energy efficiency at 25 Gb/s data rate using a vertical p-n junction electrical configuration. [80] We can see that this result is already the theoretical limit of the modulator design due to the excellent overlapping factor. To further reduce the energy consumption, it requires one or more of following approaches: reducing the micro-disk size to increase the Purcell factor, integrating more efficient active materials, or implementing new electrical configuration with larger capacitance density while still maintaining the overlapping factor. In comparison, a PC nanocavity based modulator driven by hybrid Si-ITO MOS capacitor demonstrated in [47] has the smallest theoretical energy consumption due to the high Purcell factor enabled by the ultra-compact mode volume and the large capacitance of the MOS capacitor in the active region. The energy efficiency of 3fJ/bit was majorly limited by the low overlapping factor, which can be further improved by optimizing modulator design.

D. Reversed p-n Junction vs. MOS Capacitor

Two electrical configurations of free carrier-driven modulators have been demonstrated: reversed p-n junction and MOS capacitor as schematically represented in the inset of Fig. 5a and 5b. According to (12), the energy efficiency of a resonator-based E-O modulator is proportional to its total capacitance. Given the size of an optical resonator, especially for ultra-compact resonator like PC nanocavity, the key metric to determine the energy efficiency is the capacitance density. The capacitance density of an abrupt p-n junction under reverse bias approximately follows:

$$\frac{C_j}{A} \approx \frac{1}{2}\sqrt{\varepsilon_0 \varepsilon_s q \frac{N}{V+\phi_B}} \propto N^{\frac{1}{2}}, \tag{15}$$

assuming equal donor and acceptor concentration $N_D = N_A = N$, ε_s is the static relative permittivity of the semiconductor and ϕ_B is the built-in potential. For given semiconductors, the only parameter we can tune is actually the doping concentration N. However, higher doping concentration also leads to higher optical loss, which can limit the Q-factor. As a result, almost all experimentally reported silicon E-O modulators choose the doping concentration to around 10^{18} cm^{-3}, which balance the energy efficiency with other performance metrics. The room to improve the capacitance density of reversed p-n junction is very limited.

While for MOS capacitors, the capacitance density can be estimated as:

$$\frac{C_{MOS}}{A} \approx \frac{\varepsilon_0 \varepsilon_{ox}}{t_{ox}}, \tag{16}$$

Where ε_{ox} is the static relative permittivity of the gate oxide, and t_{ox} is the gate oxide thickness. MOS capacitors offer us the freedom to scale up the capacitance density over a wide range by varying the gate oxide thickness or using high-k gate oxide materials such as HfO_2. As comparison, Fig. 5c plots the capacitance densities of p-n junction and Si/oxide/Si MOS capacitor as a function of the applied voltage simulated by SILVACO Atlas assuming a silicon doping concentration of 10^{18} cm^{-3}. Three different gate oxide layers (10 nm SiO_2, 5 nm SiO_2, 5 nm HfO_2) are simulated for the MOS capacitor. At 1 V applied voltage, the capacitance density of MOS capacitor with 10 nm SiO_2 gate oxide is comparable to that of a reversed p-n junction. While for MOS capacitors with 5 nm SiO_2 and 5 nm HfO_2 gate oxide layers, the capacitance densities are 2.8× and 9.6× times larger than that of the p-n junction, respectively. In the current 32 nm CMOS technology node, the equivalent oxide thickness (EOT) is now less than 1 nm [97]. Therefore, there is still room for further increase of the capacitance density using the MOS structure. Besides, we can see that the capacitance density of both configurations is a function of the applied voltage. Figure 5(a) and 5(b) plot the carrier density distribution of the p-n

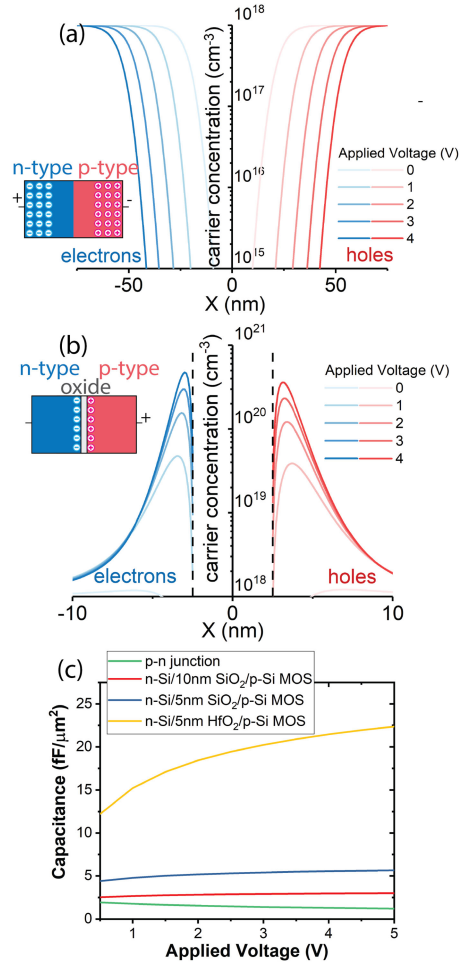

Fig. 5. (a)–(b) Free carrier distribution of (a) p-n junction and (b) Si/5 nm SiO_2/Si MOS at different applied voltage. Inset: schematics of two capacitor configurations. (c) Capacitance density as a function of the applied voltage for different configurations.

junction and MOS capacitor at different applied voltage. For p-n junction, the voltage dependence is implied in (15), as applied voltage increases electrons and holes are more separate from each other; while for the MOS capacitor, this is because as voltage increases, the average center of the accumulation layer moves towards oxide interface as is shown. Obviously, the two different configurations have completely different distributions of the free carrier perturbation. While such difference won't affect the modulation efficiency. According to (8), the resonance detuning is only proportional to the total charge perturbation, as long as the charge is overlapped with optical field. The even extreme case would be that all the charge perturbation is induced at the maximum electrical energy density point. The ability to enhance the E-O efficiency by a MOS capacitor configuration has been verified in MZI based E-O modulators. The most efficient Si MZI modulator was demonstrated using Si/oxide/Si MOS configuration in the accumulation mode fabricated by 130 nm CMOS technology node (gate oxide thickness ~2 nm), exhibiting a $V_\pi L$ of 2 V·mm [98], which is nearly one order of magnitude improvement compared with the common lateral p-n junction MZI modulators [99], [100]. Moreover, because n-type and p-type semiconductors are separated by a thin oxide layer in a MOS capacitor, it is easier to heterogeneously integrate other active semiconductor materials with silicon in a hybrid MOS configuration to further improve the energy efficiency. Still using MZI modulators as examples, a $V_\pi L$ of 0.9 V·mm was demonstrated using InGaAsP/Si hybrid MOS capacitor [8], and a $V_\pi L$ of 2.8 V·mm using graphene/Si hybrid MOS capacitor [53], both of which use 10 nm SiO_2 as the gate oxide.

Only until recently, there have been resonator-based silicon modulators using MOS or hybrid MOS configurations [47], [48], [68], [75], [101]. The over-all performance still cannot compete with the best reversed p-n junction modulators because of the relative large capacitance and poor overlapping between carrier and optical mode due to increased fabrication complexity. However, by improving the overlapping factor using advanced slot waveguide structures [93], [94], the MOS capacitor can potentially achieve better energy efficiency than p-n junction.

IV. Trade-Off Between Bandwidth and Energy Efficiency

Although the energy efficiency has been the primary driving force for future on-chip optical interconnects, the bandwidth is still the most basic requirement for an E-O modulator. A minimum data rate of 25 Gb/s is expected, which means the E-O modulator should operate at the frequency above 10 GHz. The bandwidth of a resonator-based modulator is determined by both the optical bandwidth and the electrical modulation bandwidth. The optical bandwidth is limited by the photon life time of the resonator cavity, which can be extracted by the Q-factor of the resonator by $f_{opt} = f/\mathrm{Q}$, where f is the resonance frequency of the resonator. The electrical bandwidth is determined by the RC time delay constant $\tau_{RC} = RC$, by $f_{el} = 1/(2\pi\tau_{RC})$. Then the total 3 dB bandwidth can be calculated as $(1/f_{3dB})^2 = (1/f_{opt})^2 + (1/f_{el})^2$. Contrary to the energy efficiency, the bandwidth of an E-O modulator decreases as increasing the Q-factor and the RC time constant, which is proportional to the Purcell factor $(1/f_{opt} \propto \mathrm{Q} \propto F_p)$ and capacitance $(1/f_{el} \propto \tau_{RC} \propto C)$, respectively. Then, we can get the general relationship between the energy efficiency and bandwidth from (12) as

$$E_{bit} \propto f_{opt}^2 f_{el}. \tag{17}$$

Clearly, there is an intrinsic trade-off between the bandwidth and the energy efficiency. For certain 3 dB bandwidth, we can also obtain the optimized relationship between the optical bandwidth and electrical bandwidth to minimize the energy consumption as $f_{el} = \sqrt{2} f_{opt}$. At this minimum energy consumption condition, the total power consumption *P* scales with the fourth power of modulation bandwidth as $P \propto f_{3\,\mathrm{dB}}^4$. Therefore, in order to keep the total power consumption at acceptable levels while scaling up the modulation bandwidth, it becomes especially critical to reduce the energy consumption per bit.

The total capacitance of a waveguide-based modulator is proportional to the device length, while the total resistance is inversely proportional to the device length. Therefore, the RC time constant of a resonator modulator is almost independent of the resonator size or even type, which can simplify our comparison. The electrical bandwidth is indeed only determined by the electrical configuration of the waveguide cross section. Here we compare some typical electrical configurations of silicon or silicon hybrid E-O modulators by calculating the two metrics: capacitance per length (*C/L*) and resistance length product (*RL*). The cross sections of different configurations are illustrated in Fig. 6a–6e. Three types of MOS configurations are considered according to the gate materials: high-index semiconductors (Fig. 6a) such as Si [98] and InAsGaP [8], [10], TCOs such as ITO (Fig. 6b) [47], [48], and 2D material such as graphene (Fig. 6c) [53]. 10 nm SiO_2, 5 nm SiO_2 and 5 nm HfO_2 as gate oxide layer are calculated. Besides, Fig. 6d shows the lateral p-n junction which is the most widely used in micro-ring modulators. Fig. 6e plots the vertical p-n junction used in micro-disk modulators. For comparison, a waveguide core with height of 220 nm and width of 500 nm are chosen for all cases. Highly doped semiconductor regions and metal contact are placed 500 nm away from the core except for the vertical p-n junction in the micro-disk, in which the active region has a width of 1 μm [80]. The slab cladding thickness in Fig. 6b–6d is 60 nm; and in Fig. 6a and 6e, the moderately doped region has a thickness of 100 nm. All the moderately doped semiconductor regions (light blue and light red), which contributes to the majority of the resistance, have a doping level of 1×10^{18} cm^{-3}. The results are summarized in Fig. 6g, where different symbols represent the cross-section configurations and different colors symbolize the capacitor configurations. We can see that the resistance-length product of different configurations doesn't vary too much, ranging from 3000~5500 $\Omega{\cdot}\mu$m. Since the resistance is the sum of both the n-side resistance R_n and p-side resistance R_p. Although n-type III-V semiconductor and graphene produce a lower R_n due to its larger carrier mobility, the total resistance is limited by the relatively large silicon resistance on the p-side.

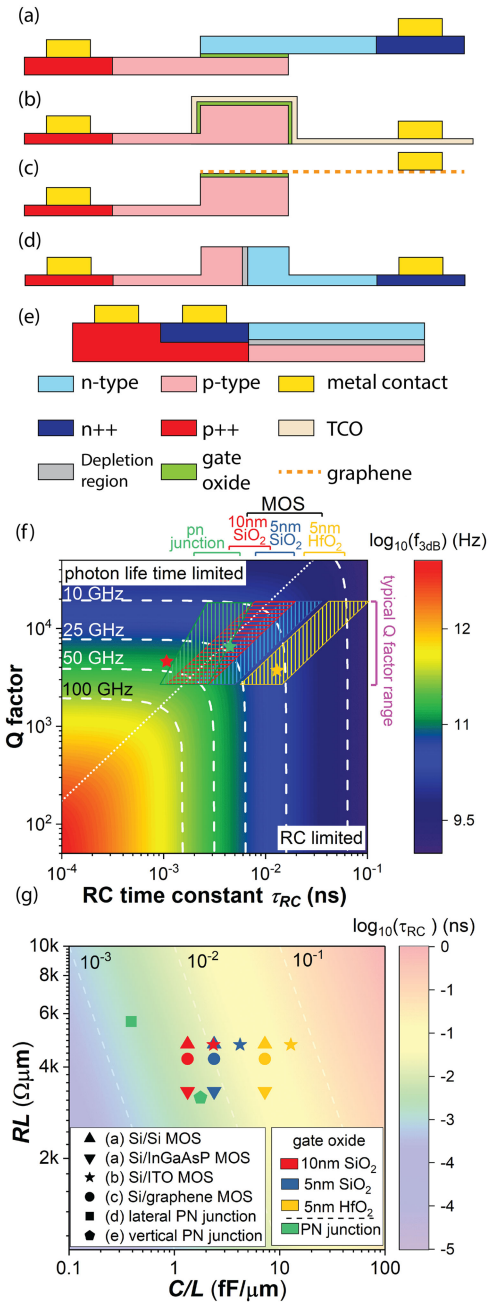

Fig. 6. (a)–(e) Waveguide cross sections of typical silicon or silicon hybrid modulators. (a) Si MOS or III-V/Si MOS. (b) Si/TCO MOS. (c) Si/graphene MOS. (d) Lateral PN junction. (e) Vertical PN junction (micro-disk). (f) 3 dB bandwidth as a function of RC time constant and Q factor at 1.55 μm. Solid symbols: Q factor and RC time constant reported in ref [102] (red), ref [80] (green), and ref [48] (yellow). (g) Capacitance per length and resistance-length product of waveguide cross sections shown in (a)–(e).

20 nm thick ITO gate with doping of 1×10^{20} cm^{-3} produces a similar resistance as the n-Si gate in Fig. 6a. While for the capacitance per length, different configurations produce values across over two orders of magnitude, so as the RC time constant.

Fig. 6f plots the 3 dB bandwidth of an E-O modulator as a function of the Q-factor and RC time constant at 1.55 μm. The minimun energy consumption condition ($\sqrt{2}f_{opt} = f_{el}$) is indicated by the dotted line. The shadowed areas in Fig. 5f mark the corresponding region of different electrical configurations versus typical Q-factor range. As discussed in Section III, the Q-factor is related to the size of the resonator and the doping induced loss. This offers us the freedom to control the Q-factor, typically ranging from a few thousand to $\sim 10^4$. For example, an E-O modulator operating at 10 GHz requires a Q-factor below 2×10^4. Because different parameters scale differently versus the doping concentration, such as free-carrier-limited Q factor $\mathrm{Q} \propto \mathrm{N}^{-1}$, resistance $\mathrm{R} \propto \mathrm{N}^{-1}$, p-n junction capacitance $\mathrm{C}_j \propto \mathrm{N}^{1/2}$ and MOS capacitance $\mathrm{C}_{MOS} \propto \mathrm{N}^0$, we can have the relationship between the free-carrier-limited Q factor and the RC time constant as $\mathrm{Q} \propto \tau^2_{RC,\mathrm{junction}}$ and $\mathrm{Q} \propto \tau_{RC,MOS}$, which is represented by the slope of the shadowed area boundary. Generally, pn junction configurations have the smallest τ_{RC} due to the small capacitance density, which are suitable for high bandwidth application. However, the majority of the p-n junction region (green shadow area) is above the matching condition. This means the bandwidth of p-n junction driven modulator is always limited by the optical bandwidth, while some of the electrical bandwidth is actually wasted. The red star in Fig. 6f labels the recently demonstrated 128 Gb/s micro-ring modulator [102]. The capacitance per length still has the potential to increase for better energy efficiency. The green star labels the micro-disk modulator with vertical p-n junction in [80], which shows a balance between optical bandwidth and electrical bandwidth due to the large capacitance density of the micro-disk resonator design and vertical junction. It is similar for MOS configurations with 10 nm SiO_2 gate oxide layer. The corresponding region (red shadow area) shows good overlapping with the mininmun energy consumption condition for a wide bandwidth up to 50 GHz. For example, a Q-factor of 10^4 and a RC time constant of 10 ps would be desired for an E-O modulator operating around 15 GHz. Increasing the capacitance density by reducing the gate oxide thickness can improve the energy efficiency based on previous discussion, however, we have to sacrifice the bandwidth due to the increased τ_{RC}. For the example of 5 nm HfO_2 gate oxide MOS, based on the assumption of 1×10^{18} cm^{-3} doping concentration, it will limit the electrical bandwidth to a few GHz. Further increasing the bandwidth requires the reduction of the series resistance, usually at the cost of reduced Q factor. PC nanocavity offers a unique advantage over micro-ring and micro-disk in this aspect. Because of the standing wave pattern in a PC nanocavity, we can use the mode-matched doping method by highly doping the anti-node (low energy region) [83] to reduce the distance between the highly doped region and the active capacitor. This method may potentially reduce the resistance by one order of magnitude without increasing the loss or reducing the Q factor. While this strategy cannot be applied to travel-wave resonators such as micro-ring and micro-disk. The yellow star in Fig. 6f labels the estimated τ_{RC} of a PC nanocavity modulator in [48] using the node-matched doping method. An operation speed larger than 12 GHz is achievable with 10 nm HfO_2 gate oxide layer, while maintaining the potential to achieve attojoule/bit energy efficiency.

V. Wavelength Control and Driving Electronic Integrated Circuits

A. Wavelength Control

In practice, in order to compensate the fabrication error and temperature fluctuation, active control of the resonance wavelength is always necessary. Thermal tuning is the most widely used method. State-of-the-art integrated heaters based on embedded silicided c-Si can achieve a high tuning efficiency of $\sim$1.6 nm/mW (3.5 μW/GHz) on 45 nm CMOS platform [103]. For a micro-ring resonator based dense wavelength division multiplexing (DWDM) system with channel distance of $\sim$1 nm, it requires an average wavelength tuning range of $\sim$2 nm [104]. Then, it consumes $\sim$1.25 mW power for each micro-ring, which corresponds to energy efficiency of 50fJ/bit for 25 Gb/s OOK channel and 10fJ/bit for 128 Gb/s PAM4 channel. The thermal tuning efficiency can be further increased to 4.8 nm/mW (1.67 μW/GHz) by improving the thermal isolation between the resonator and the silicon substrate through topside silicon undercut-etching [105], which means $\sim$3.3fJ/bit for 128 Gb/s channel. However, better thermal isolation also increases the response time to sub-millisecond range. It would be chalenging to further reduce the energy consumption using thermal tuning. Alternatively, electrial wavelength tuning is much faster and more energy efficient. According to the analysis in Section III, we can optimize the electrical wavelength tunability based on (13). Large wavelength tunability (>250 pm/V) that is comparable with thermal tuning can be achieved. For example, the micro-disk modulator in [80] can compensate 10 °C temperature change using electrical tuning with power consumption less than 50 μW. A recent demonstration of hybrid TCO-silicon MOS-structured micro-ring achieved extremely large wavelength tunability of 271 pm/V and tuning range of 2 nm with a negligible static power consumption of 0.16 pW [106]. This near-zero-energy wavelength tuning method can potentially replace the power-hungry thermal tuning in future on-chip optical interconnect systems.

B. Driving Electronic Integrated Circuits

According to the power break down analyis of a micro-ring based DWDM transmitter in [103], it is the driving electrical ICs that limit the total energy efficiency to 0.83 pJ/bit. There are two groups of ICs that consume most power: modulator driver (33% of total power) and timing-issue related ICs (55% of total power), such as phase-locked loop (PLL), clock distribution, serializer, etc. To reduce the energy consumpton of the modulator driver, it is essential to reduce the required driving voltage of the modulator to eliminate the use of electrial amplifer. Such optimizaiton can similarly be done based on (14). The ideal case would be that the switching of an opitcal modulator can be comparable to fliping an electrical transistor [2]. For the timing-issue related ICs, it can only be solved by optimizing the IC architecture, which is beyond the scope of this manuscript. Ref [2] provided a thorough review and insightful perspectives on this issue by pointing out that such timing-issue related energy disspation may potentially be eliminated by optical approaches, such as optical clock distribution and pulsed opitcal readout.

VI. Conclusion and Outlook

In this paper, we developed a general model to quantitatively describe the energy efficiency of carrier-driven resonator-based silicon photonic modulators. Three most fundamental factors, namely the free carrier dispersion strength of the active materials, the Purcell factor of the resonators, and the electrical configuration of the capacitors, are identified as the most critical factors to achieve atto-joule/bit energy efficiency. The development of future atto-joule/bit modulators should consider one or all of these three aspects. We analyzed the approach of heterogeneous integration of silicon photonics with different active materials benefited from the enhanced free carrier plasma dispersion effect, which shows the possibility to improve the energy efficiency by 3$\sim$100$\times$. We also proved that PC nanocavities surpasses micro-ring and micro-disk resonators in terms of Purcell factor, and MOS capacitor is more efficient than PN junction due to its larger, more scalable capacitance density and compatibility with other active semiconductor materials. Through the aforementioned investigation, we conclude the possibility theoretically to reach atto-joule/bit energy efficiency using existing carrier-driven resonator-based silicon photonic modulators.

In addition, we investigated the intrinsic tradeoff between the energy efficiency and bandwidth, which is caused by both the photon lifetime of the resonators and the RC delay product. To maximize the energy efficiency while still achieving high bandwidth, both optical bandwidth and electrical bandwidth need to be carefully engineered. The use of MOS capacitor configuration offers additional design freedom to tune the capacitance density. It is shown that MOS capacitors with 10 nm SiO_2 gate oxide layer offer a good balance between the energy efficiency and bandwidth up to 50 GHz. Moreover, our model also guides the optimization of large electrical wavelength tunability and low driving voltage, which provides the possibility to eliminate the energy dissipation from thermal wavelength control.

To conclude, the modeling and simulation in this paper laid a solid theoretical foundation for silicon photonic modulators to continue to play key roles in extreme scale parallel optical interconnects between on-chip cores and within multi-chip modules. However, to truly realize atto-joule/bit energy efficiency for the entire optical interconnect system, efforts are required to minimize or eliminate the energy consumption from wavelength tuning and electronic driving Ics in parallel to the photonic device advancement.

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