Intel 8085
CS-252

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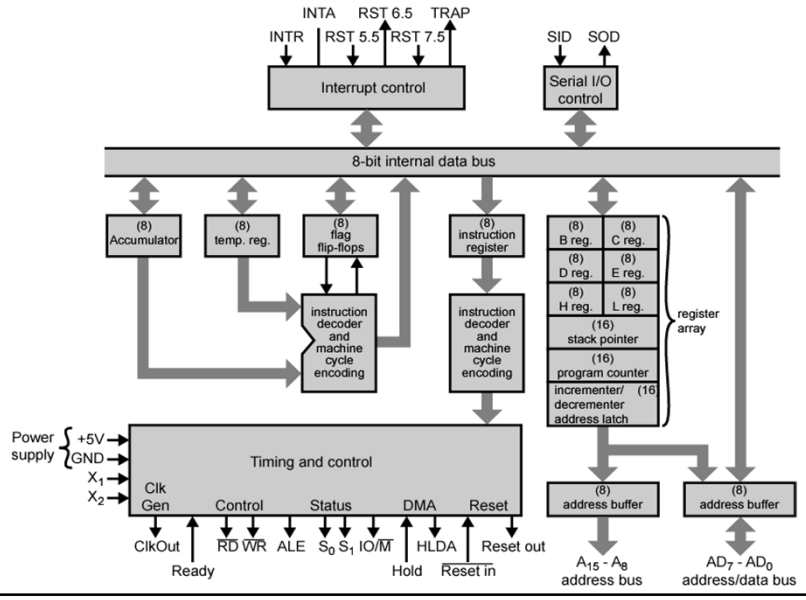
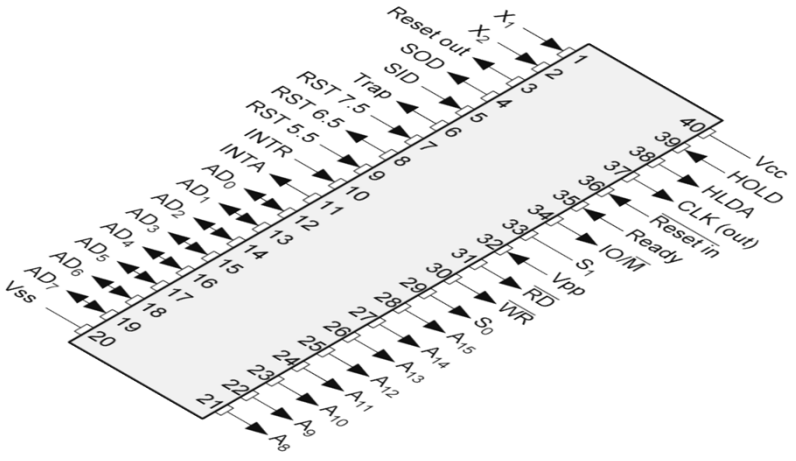
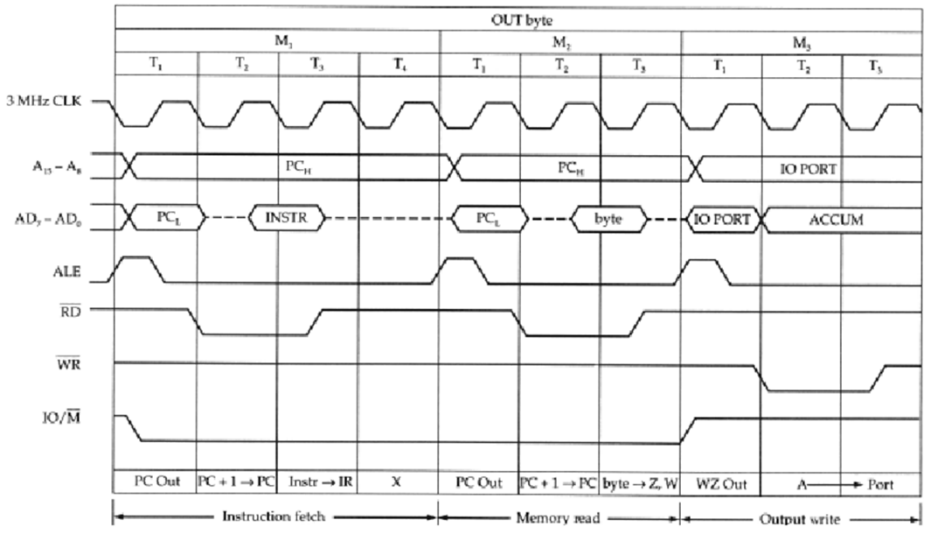
Intel 8085 CPU Block Diagram



Intel 8085 Pin Configuration



Intel 8085 OUT Instruction Timing Diagram



Address Bus and Data Bus

The address bus is a group of sixteen lines i.e A0-A15. The address bus is unidirectional, i.e., bits flow in one direction from the microprocessor unit to the peripheral devices and uses the high order address bus.

Control and Status Signals

- **ALE –** It is an Address Latch Enable signal. It goes high during first T state of a machine cycle and enables the lower 8-bits of the address, if its value is 1 otherwise data bus is activated.
- **IO/M' –** It is a status signal which determines whether the address is for input-output or memory. When it is high(1) the address on the address bus is for input-output devices. When it is low(0) the address on the address bus is for the memory.
- **SO, S1 –** These are status signals. They distinguish the various types of operations such as halt, reading, instruction fetching or writing.

IO/M' vs S0 and S1

IO/M'	S1	S0	Data Bus Status
0	1	1	Opcode fetch
0	1	0	Memory read
0	0	1	Memory write
1	1	0	I/O read
1	0	1	I/O write
1	1	1	Interrupt acknowledge
0	0	0	Halt

Control Signals

- **RD' –** It is a signal to control READ operation. When it is low the selected memory or input-output device is read.
- **WR' –** It is a signal to control WRITE operation. When it goes low the data on the data bus is written into the selected memory or I/O location.
- **READY –** It senses whether a peripheral is ready to transfer data or not. If READY is high(1) the peripheral is ready. If it is low(0) the microprocessor waits till it goes high. It is useful for interfacing low speed devices

Power Supply and Clock Frequency

- **Vcc –** +5v power supply
- **Vss –** Ground Reference
- **XI, X2 –** A crystal is connected at these two pins. The frequency is internally divided by two, therefore, to operate a system at 3MHZ the crystal should have frequency of 6MHZ.
- **CLK (OUT) –** This signal can be used as the system clock for other devices.

Interrupts and Peripheral Initiated Signals

- The 8085 has five interrupt signals that can be used to interrupt a program execution.
- (i) INTR
  (ii) RST 7.5
  (iii) RST 6.5
  (iv) RST 5.5
  (v) TRAP
- The microprocessor acknowledges Interrupt Request by INTA' signal. In addition to Interrupts, there are three externally initiated signals namely RESET, HOLD and READY. To respond to HOLD request, it has one signal called HLDA.
- **INTR –** It is an interrupt request signal.
- **INTA' –** It is an interrupt acknowledgment sent by the microprocessor after INTR is received.

Reset Signals

- **RESET IN' –** When the signal on this pin is low(0), the program-counter is set to zero, the buses are tristated and the microprocessor unit is reset.
- **RESET OUT –** This signal indicates that the MPU is being reset. The signal can be used to reset other devices

DMA Signals

- **HOLD –** It indicates that another device is requesting the use of the address and data bus. Having received HOLD request the microprocessor relinquishes the use of the buses as soon as the current machine cycle is completed. Internal processing may continue. After the removal of the HOLD signal the processor regains the bus.
- **HLDA –** It is a signal which indicates that the hold request has been received after the removal of a HOLD request, the HLDA goes low.

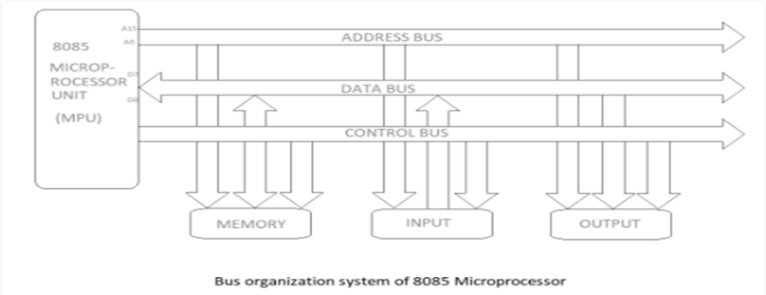
Serial I/O Ports

Serial transmission in 8085 is implemented by the two signals,

- **SID and SOD –** SID is a data line for serial input where as SOD is a data line for serial output.

Bus organization of 8085 microprocessor

- Bus is a group of conducting wires which carries information, all the peripherals are connected to microprocessor through Bus.
- Diagram to represent bus organization system of 8085 Microprocessor.



Bus organization system of 8085 Microprocessor

Address bus

- It is a group of conducting wires which carries address only. Address bus is unidirectional because data flow in one direction, from microprocessor to memory or from microprocessor to Input/output devices (That is, Out of Microprocessor) Length of Address Bus of 8085 microprocessor is 16 Bit (That is, Four Hexadecimal Digits), ranging from 0000 H to FFFF H, (H denotes Hexadecimal). The microprocessor 8085 can transfer maximum 16 bit address which means it can address 65, 536 different memory location.

Address bus

- The Length of the address bus determines the amount of memory a system can address. Such as a system with a 32-bit address bus can address 2^32 memory locations. If each memory location holds one byte, the addressable memory space is 4 GB. However, the actual amount of memory that can be accessed is usually much less than this theoretical limit due to chipset and motherboard limitations.

Data bus

- It is a group of conducting wires which carries Data only. Data bus is bidirectional because data flow in both directions, from microprocessor to memory or Input / Output devices and from memory or Input / Output devices to microprocessor. Length of Data Bus of 8085 microprocessor is 8 Bit (That is, two Hexadecimal Digits), ranging from 00 H to FF H. (H denotes Hexadecimal).

Data bus

- When it is write operation, the processor will put the data (to be written) on the data bus, when it is read operation, the memory controller will get the data from specific memory block and put it into the data bus.
- The width of the data bus is directly related to the largest number that the bus can carry, such as an 8 bit bus can represent 2 to the power of 8 unique values, this equates to the number 0 to 255.A 16 bit bus can carry 0 to 65535.

Control bus

- It is a group of conducting wires, which is used to generate timing and control signals to control all the associated peripherals, microprocessor uses control bus to process data, that is what to do with selected memory location. Some control signals are :
- Memory read
- Memory write
- I/O read
- I/O Write
- Opcode fetch
- If one line of control bus may be the read/write line. If the wire is low (no electricity flowing) then the memory is read, if the wire is high (electricity is flowing) then the memory is written.

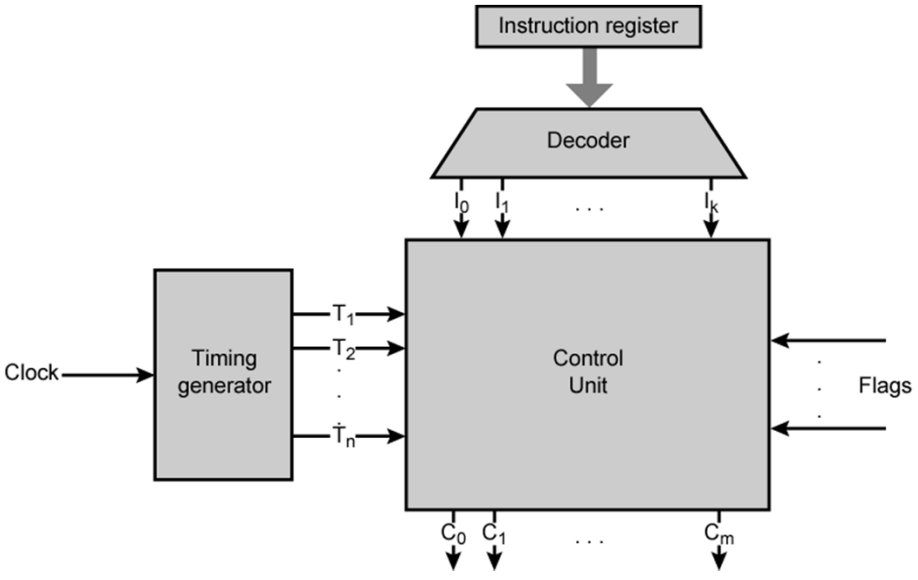
Hardwired Implementation (1)

- Control unit inputs
- Flags and control bus
  - Each bit means something
- Instruction register
  - Op-code causes different control signals for each different instruction
  - Unique logic for each op-code
  - Decoder takes encoded input and produces single output
  - *n* binary inputs and 2^n outputs

Hardwired Implementation (2)

- Clock
  - Repetitive sequence of pulses
  - Useful for measuring duration of micro-ops
  - Must be long enough to allow signal propagation
  - Different control signals at different times within instruction cycle
  - Need a counter with different control signals for t1, t2 etc.

Control Unit with Decoded Inputs



Problems With Hard Wired Designs

- Complex sequencing & micro-operation logic
- Difficult to design and test
- Inflexible design
- Difficult to add new instructions

Thank You