EL3032-POWER ELECTRONICS

LAB MANUAL

DEPARTMENT OF ELECTRICAL ENGINEERING,

FAST-NU, LAHORE

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EXPERIMENT 01

ANALYZING A COMPOSITE AMPLIFIER

Objective

To analyze the working and performance of a composite amplifier

Material and Equipment

1. Capacitance (0.1 µF non-polar)
2. Assorted resistors(10 Ω, 120 Ω,39.2k Ω)
3. LM317
4. Op-amp 741
5. Signal Generator
6. Oscilloscope
7. Breadboard

Circuit Diagram

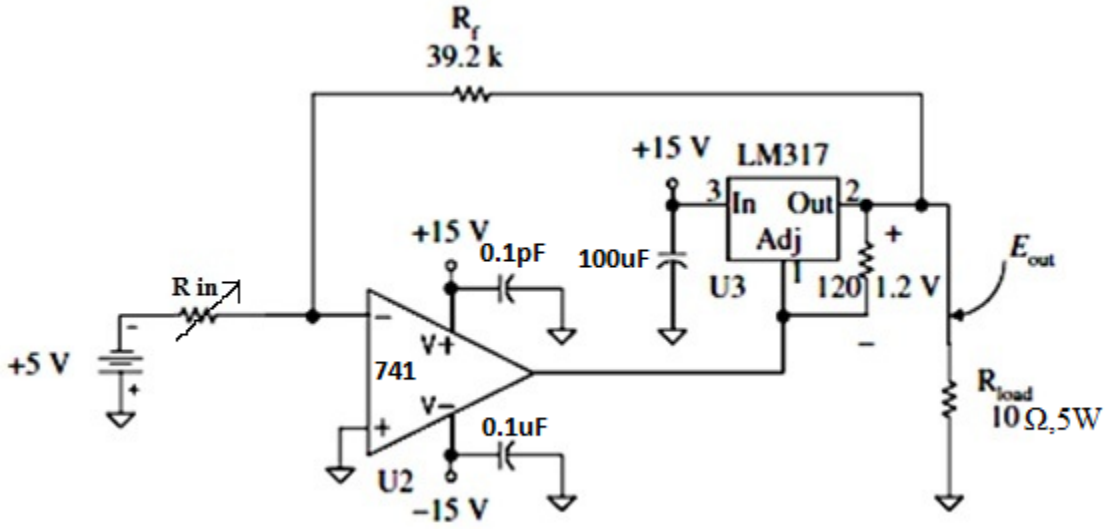


Figure 1. Circuit schematic of composite amplifier

Task

1. Build the circuit as shown in Figure 1.
2. Use a load resistance in the range of 100 to 10k Ω.
3. Apply -5V on inverting pin of amplifier through R_{in}.

4. Vary input resistance (R_{in}) and measure the corresponding V_{out} across the load ($R_L = 10\Omega$) and fill in Table 1.
5. With R_{in} = 33 kΩ, vary the load resistance in the given range. Note the readings in Table 2.
6. Calculate the input power and the output power for each of the given R_{in} and tabulate.

Observations and Calculations

Table 1. Line-regulation with R_L=10Ω

Sr.no.	**Resistance (Ω)**	**V_{out} (V)**	**I_{load} (A)**	**P_{in}**	**P_{out}**
1	27 k				
2	33 k				
3	39 k				
4	47 k				
5	56 k				

Table 2. Load-regulation with R_L= 33 kΩ

Sr.no.	**Load Resistance (Ω)**	**V_{out} (V)**	**I_{load} (A)**	**P_{in}**	**P_{out}**
1	100				
2	2.2k				
3	3.3 k				
4	6.8 k				
5	10k				

POST LAB QUESTIONS:

1. What is the effect of changing R_{in} on the output and why?
2. Explain what is observed when the load resistances are changed, while input is kept constant.

EXPERIMENT 02

ANALYZING AN AUDIO AMPLIFIER

Objective

- To learn the working of an audio amplifier.
- To analyze the frequency response of an audio amplifier

Material and Equipment

1. LM386
2. Assorted resistors (10 Ω, 620 Ω, 15 kΩ)
3. Capacitors (10 uF, 47 nF, 10 nF, 0.05 uF, 250 uF)
4. Signal Generator
5. Oscilloscope
6. DC Power Supply
7. Breadboard

Circuit Diagram

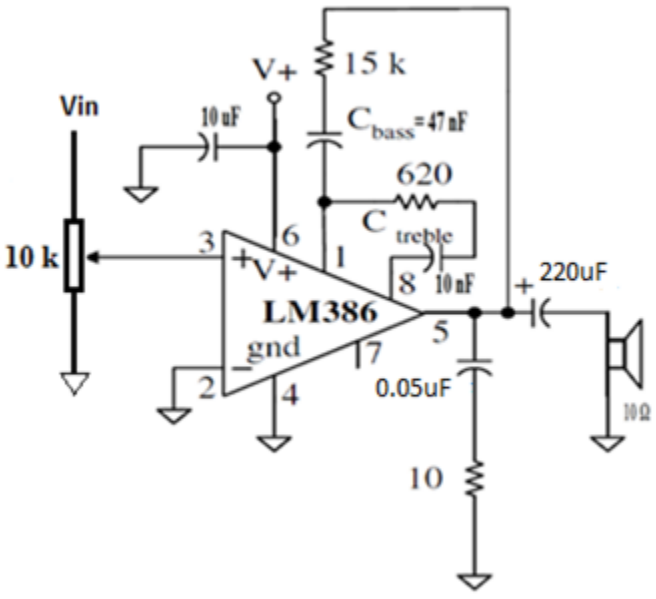


Figure 1. Audio amplifier circuit

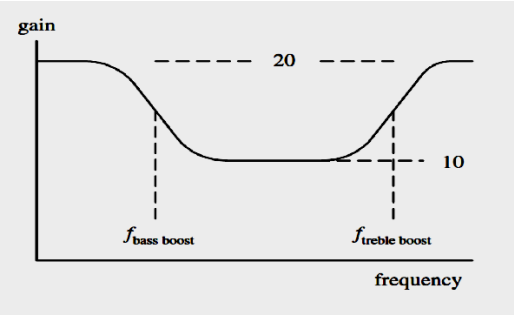


Figure 2. Frequency characteristics of audio amplifier

Tasks

1. In the lab, connect the circuit of Figure 1 without the speaker. Use 10Ω resistor in place of a speaker. The frequency characteristics are shown in Figure 2.
2. Use +12 V as input supply for LM386.
3. Apply a sinusoid 1 V_{p-p} signal as input signal from function generator.
4. Use a 10 kΩ variable resistor at the input to limit the input signal. Adjust the input resistor to get a stable response.
5. Increase the frequency of input signal starting from 10 Hz and observe the amplitude of output signal on oscilloscope. And note the readings in Table 1.

Observations

Table 1. Output-voltage and gain response

Sr.no.	Frequency (kHz)	Output Voltage (V)	Gain
1	0.1		
2	0.5		
3	1		
4	2		
5	4		
6	6		
7	8		
8	10		

f_{base} = _____
f_{treble} = _____

POST LAB QUESTIONS:

1. Draw the frequency response and show the 3.0 dB bandwidth.
2. What changes must be done in the circuit to make it a high power audio amplifier?

EXPERIMENT 03

IMPLEMENTATION AND ANALYSIS OF A PUSH-PULL AMPLIFIER

Objective

- To implement and analyze the working of a push-pull amplifier.

Material and Equipment

1. Capacitance (0.1 µF non-polar)
2. Assorted resistors(520 Ω,820 Ω, 22k Ω,10k Ω)
3. 10KΩ or 50KΩ variable resistor
4. IRF 540
5. IRF 9540
6. Op-amp 741
7. Bulb
8. Signal Generator
9. Oscilloscope
10. Breadboard

Circuit Diagram

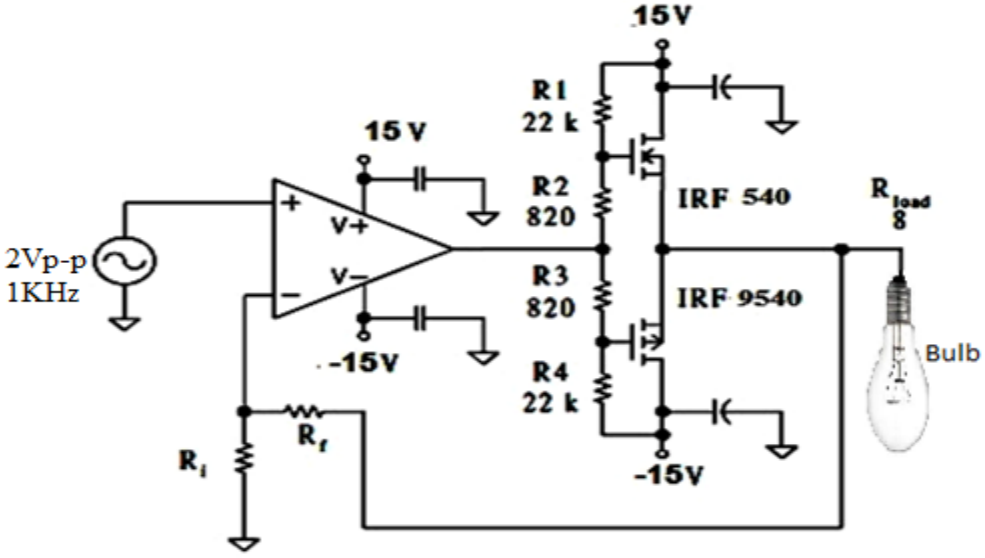


Figure 1. Push-Pull amplifier circuit

Task

1. Build the circuit as shown in Figure 1.
2. Use a bulb as a load instead of resistor.
3. Use different values for R_f resistor to change the gain of amplifier. And see the effect on the brightness of bulb.
4. Measure load voltage, load current and calculate the load power for different values of R_f and fill in the Table 1.

Observations:

Table 1. Output signal response with R_i=1.0 KΩ

Sr. no.	R_f(KΩ)	V_{load}(V)	I_{load} (A)	P_{load} (W)
1	10			
2	15			
3	22			
4	33			
5	47			

POST LAB QUESTIONS:

1. What is the effect of R_f on the brightness of the load?
2. What is the purpose of the op-amp stage and what is the purpose of the MOSFET stage on the amplifier?
3. What is the application of a push-pull amplifier?

EXPERIMENT 04

DESIGN AND IMPLEMENTATION OF A LOW SIDE SWITCH

Objective

- To design and implement N-channel low side MOSFET switch
- To calculate the power dissipated in a motor load when duty cycle of the input pulse is varied

Equipment

1. IRF 540
2. SN 7406
3. Capacitors (0.1 µF, 470 µF)
4. Assorted resistors (560 Ω, 10 Ω)
5. DC Motor (12V)
6. Power supply
7. Signal Generator
8. Multimeter
9. Oscilloscope

Circuit Diagram

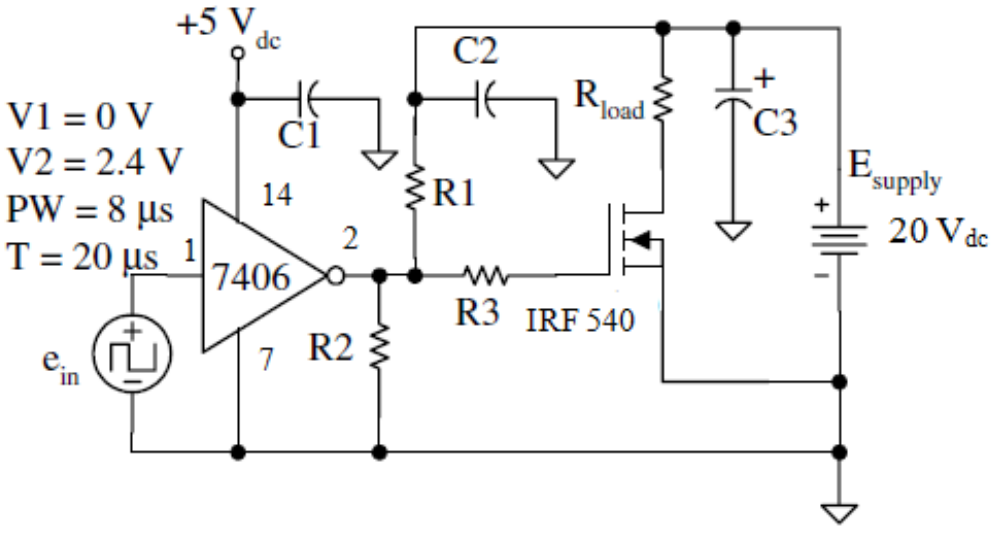


Figure 1. Low-side switch circuit

Circuit Design

- The input pulse amplitude is only 2.4 V_p. Most MOSFETs need 10 V_p to turn hard *on*. The 7406 has been added to convert the logic level at its input to 10 V_p to 20 V_p. Be sure to include C_1 = 0.1 μF capacitor *close* to the 7406's power pin, as shown in Figure 1.
- The IRF540 needs a gate voltage between 10 V_p and 20 V_p. But the only pull-up supply is 20 V_{dc}. Resistors R_1 and R_2 divide the 20 V_{dc} in half when the 7406's output goes *open*. Also 7406 provides a voltage of 0.7 V_{dc} when the output is *closed.* As 7406 can sink a maximum of 40mA_p current, we can calculate R1 as follows:

$$R_1 > \frac{20\ V_{dc} - 0.7\ V_p}{40\ mA_p} = 483\ \Omega$$

- Since R_1 and R_2 divide 20 V_{dc} in half when the 7406's output goes *open,* we can select R_1 = R_2 = 560 Ω. A decoupling capacitor C_2 = 0.1 μF is also connected as close to R_1 as practical.
- From the junction of R_1 and R_2 the signal travels to the gate. Although it may seem an open circuit when looking into the gate, there is about 640 pF of parasitic capacitance between the gate and source. Also, the leads and traces contain inductance. The result is a series resonant circuit. When a pulse from 7406 reaches this resonant circuit is starts to resonate. Here resistor R_3 dampens that parasitic tank. Set R_3 in the 10 Ω to 100 Ω range.
- Capacitor C_3 should be connected as close to the power end of the load as practical. Place a 470 μF electrolytic capacitor, in parallel with a 0.1 μF film capacitor, as shown in Figure 2.

Task

- Build the circuit in Figure 1. Select suitable values of R_1 and R_2. Take particular care to keep the leads as short as possible, and to provide the separate common returns for the logic, the motor, and the decoupling capacitors. The load in this case is a DC motor. Connect a Schottky diode *directly* across the load terminals.

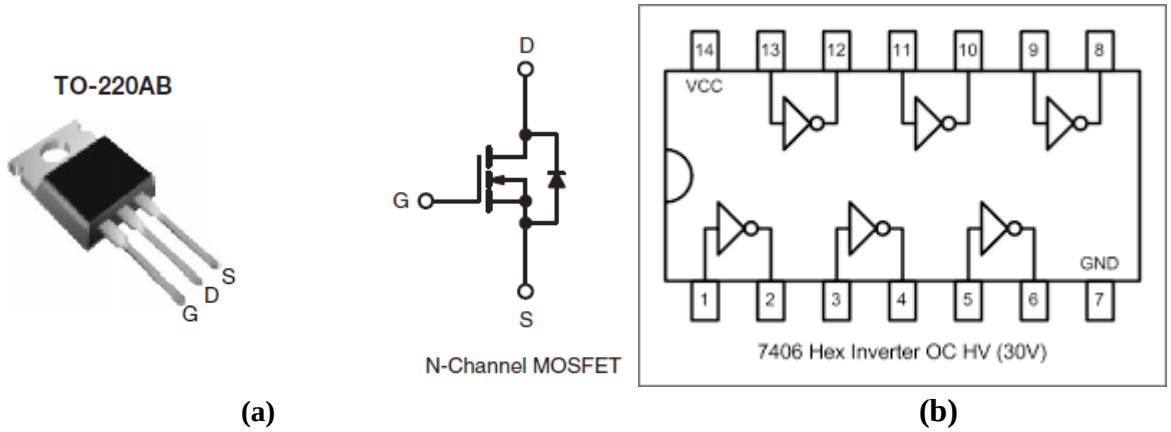
  Precaution: Connect a heat sink to the MOSFET as it gets heated up quickly due to high current load.
- From the function generator, provide a signal of 0 V to 2.4 V, 50% duty cycle square wave at *50 kHz*.
- The motor *should* run. Assure that your circuit is correct.
- Verify that the output is correct by displaying both the input and the drain waveform with an oscilloscope. Look carefully at the drain low voltage level and the pulse widths.

- Record the wave shapes of the voltage at the input and across the transistor. Be sure to accurately record the low and the high levels of the signal across the load.
- Vary the duty cycle and observe the variation in the speed of the DC motor. Take five different readings by varying the duty cycle of the input and fill Table 1.
- Calculate the power dissipated by the load using the formula:

$$\boldsymbol{P_{load} = (1-D)v_p i_p = {(1-D)(v_p)^2}/{R_{load}}}$$

$$\boldsymbol{V_{load} = (1-D)Vdc}$$

R_{load} of the motor is a few ohms and can be measured practically.



(a) **(b)**

Figure 2: (a) Pin configuration of IRF 540 (b) Pin configuration of SN7406

Observations:

Table 1. Output-voltage response with R_{Load}=10Ω,5W

#	Duty cycle of e_{in} D1 (%)	Duty cycle at output of 7406 D2 = 100% - D1(%)	V_p (output) (V)	P_{load} (W)
1	80			
2	60			
3	50			
4	40			
5	20			

POST LAB QUESTIONS:

1) Compare high side and low side switches. What are their advantages over one another?

EXPERIMENT 05

DESIGN AND IMPLEMENTATION OF A HIGH SIDE SWITCH

Objective

- To design and implement P-channel high side MOSFET switch
- To calculate the power dissipated in a motor load when duty cycle of the input pulse is varied.

Equipment

1. IRF 9540
2. SN 7406
3. Capacitors (0.1 µF, 100 µF)
4. Assorted resistors (330 Ω, 390 Ω, 10Ω)
5. DC Motor (12V)
6. Power supply
7. Signal Generator
8. Multimeter
9. Oscilloscope

Circuit Diagram

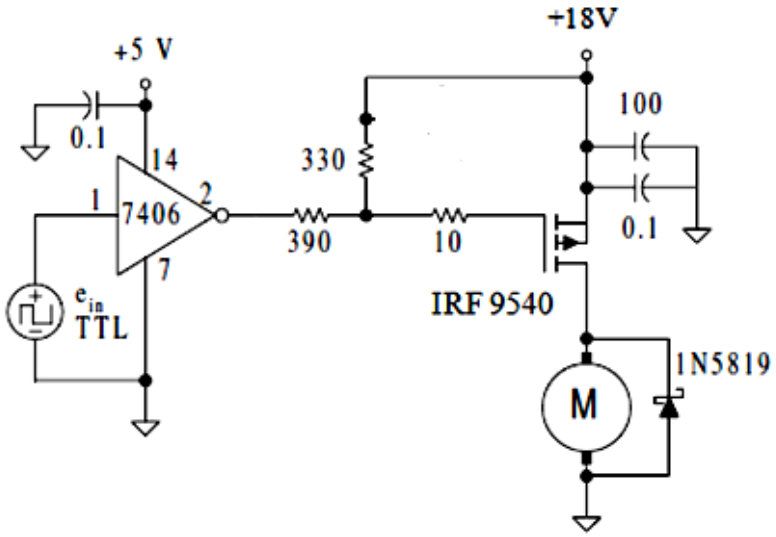


Figure 1. High-side switch circuit

Circuit Design

- To drive the circuit with a logic level, add the 7406 open collector to the input. It requires a pull-up resistor, R_1, connected to the high voltage supply. Since this supply is greater than the 18 V maximum V_{GS} that the IRF9540 can withstand, a voltage divider must be included, R_2. This voltage divider is different from the one used with the *n*-channel low side switch. Both the source and the gate of the MOSFET are at +18Vdc, as shown in Figure 1.
  Since the source is at a constant +18 V_{dc}, the MOSFET stays on without damaging the gate.
- Let $R_1 = 330\ \Omega$ and $R_2 = 390\ \Omega$. This allows the transistor's gate parasitic capacitance to charge and discharge through minimum resistance. Resistor R_3 is in the 10Ω to 100 Ω range.
- The capacitors, C_1 and C_2, should be placed as close to the IC or transistor pin as possible. Set C_1 to about 0.1 μF. Select C_2's value at about 100 μF for each ampere of load current.
- The Schottkyfly back diode is almost always necessary. Place the diode close to the drain lead of the MOSFET, on the circuit board, as shown in Figure 2.

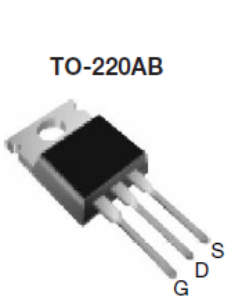
Task

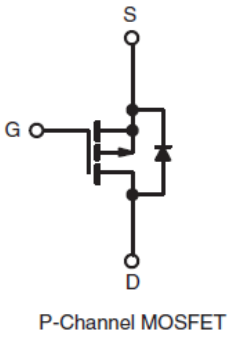
- Build the circuit in Figure 1. Take particular care to keep the leads as short as possible, and to provide the separate common returns for the logic, the motor, and the decoupling capacitors. The load in this case is a DC motor. Connect a Schottky diode *directly* across the load terminals.
  Precaution: Connect a heat sink to the MOSFET as it gets heated up quickly due to high current load.
- From the function generator, provide a signal of 0 V to 2.4 V, 50% duty cycle square wave at *50 kHz*.
- The motor *should* run. Assure that your circuit is correct.
- Verify that the output is correct by displaying both the input and the drain waveform with an oscilloscope. Look carefully at the drain low voltage level and the pulse widths.
- Record the wave shapes of the voltage at the input and across the load. Be sure to accurately record the low and the high levels of the signal across the load.
- Vary the duty cycle and observe the variation in the speed of the DC motor. Take five different readings by varying the duty cycle of the input and fill Table 1.
- Calculate the power dissipated by the load using the formula:

$$\boldsymbol{P_{load} = Dv_p i_p = {D(v_p)^2}/{R_{load}}}$$

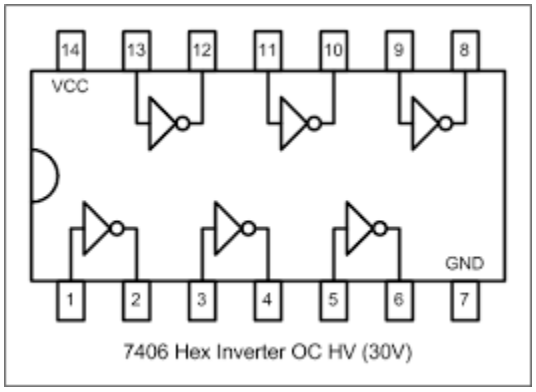
$$V_{load} = (D)Vdc$$

R_{load} of the motor is a few ohms and can be measured practically.





(b)



(b)

Figure 2: (a) Pin configuration of IRF 9540 (b) Pin configuration of SN7406

Observations

Table 1. Output-voltage response with R_{Load}=10Ω, 5W

S. No.	Duty cycle of e_{in} D1 (%)	Duty cycle at output of 7406 D2 = 100% - D1(%)	V_p (output) (V)	P_{load} (W)
1	80			
2	60			
3	50			
4	40			
5	20			

POST LAB QUESTIONS:

1. Comment on the variation of the output power with the duty cycle of the input signal.

EXPERIMENT 06

IMPLEMENTATION OF OPTICALLY ISOLATED GATE DRIVER FOR N-CHANNEL MOSFET

Objectives

- To become familiar with the use of opto-coupler in power electronics circuits.
- Implementation of gate driver circuit for N-Channel MOSFET
- Study the effect of duty cycle variation in DC to DC conversion

Material and Equipment

1. Opto-Coupler (4N-35)
2. BJT (2N3904)
3. N-Channel MOSFET (IRF540)
4. Assorted resistors
5. Digital Multimeter
6. DC Supply
7. Breadboard

Circuit Diagram

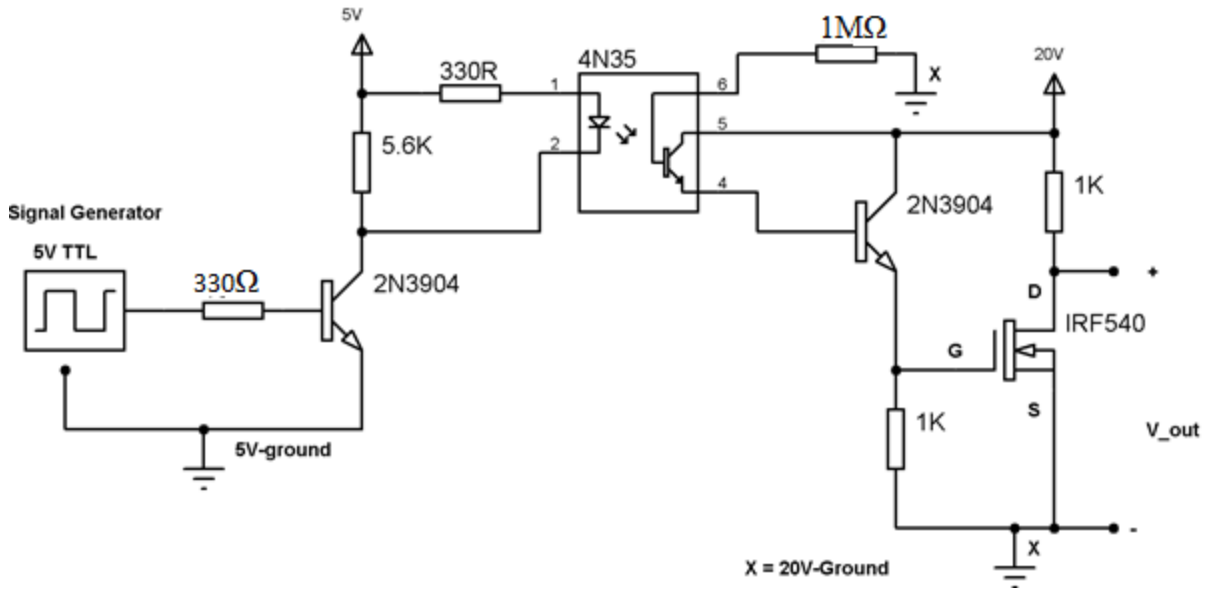


Figure 1. Optically isolated gate driver circuit for MOSFET

Task

1. Implement the circuit diagram shown in Figure 1.
2. Vary the duty cycle from signal generator and observe the output DC voltage of the circuit.
3. Sketch load-voltage waveforms for selected values of duty-cycle.

Design Procedure

1. Set the signal generator such that it gives square wave at frequency of 1 kHz. Apply a $5V_{pp}$ or $10V_{pp}$ TTL signal from the signal generator. Duty cycle can be varied by pulling out and varying the duty knob on the signal generator. Vary the duty cycle and observe its range with the help of oscilloscope.
    a. Minimum duty cycle ratio = _____
    b. Maximum duty cycle ratio = _____
2. Connect the signal generator with opto-coupler through transistor as shown in figure. Ground of signal generator and 5 V supply is common.
3. The 4N-35 diode forward current is approximately 15 mA. Since the input voltage is 5V, hence the value of R1 comes out to be equal to 330 Ω.
4. Connect the output side of opto-coupler with MOSFET through transistor as shown in figure. Supply on the output side should be adjusted to 20 V.
   Note: *Make sure that the GROUND of 5V and 20V supply are separate from each other.*
5. Record voltage across the load resistance for at least ten different values of duty cycle ratio in Table 1 and also plot the waveforms observed on oscilloscope.
6. Compare the practical and theoretical output voltages using the following relationship:

$$V_{out} = V_{in} \times (1 - DCR)$$

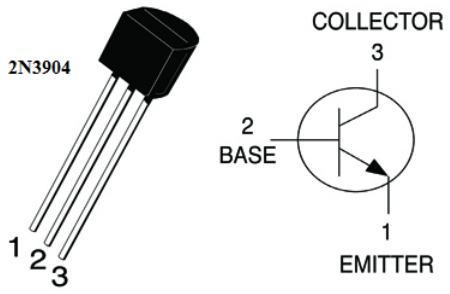


Figure 2. Pin configuration of 2N304

Observations and Calculations:

Table 1. Output voltage response with R_L =10Ω, 5W

S.no.	ON-Time	Duty Cycle Ratio (DCR)	V_{out}(practical)	V_{out}(theoretical)
1				
2				
3				
4				
5				

POST LAB QUESTIONS:

1. Sketch the waveforms for following points on your lab notebooks neat and clean.
    a. Plot the voltage waveform across the load resistance.
    b. Plot the variation of output voltage with respect to the duty cycle

2. Design a DC step-up chopper circuit, namely BOOST regulator, using a MOSFET. The circuit must work on the switching of the MOSFET, and must be able to provide 12 V, 0.8 A at the output, if the input is 5 V.

EXPERIMENT 07

IMPLEMENTATION OF A SIMPLE SERIES VOLTAGE REGULATOR

Objective

To design a series voltage regulator that has a better regulation as compared to a simple ZENER regulator (made without a transistor).

Material and Equipment

1. Transistor (D313)
2. ZENER Diode (4.7 V)
3. Resistor **R** of designed value (1kΩ - 1.2 kΩ)
4. Assorted resistor for Load
5. Digital Multimeter
6. DC Supply
7. Breadboard

Circuit Diagram

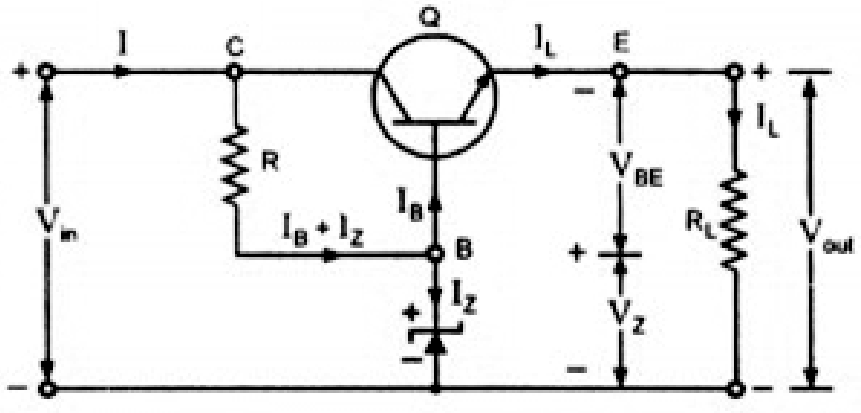


Figure 1. Simple series voltage regulator

Task

1. Design the circuit shown in Figure 1.
2. Record the readings for observations sets 1 and 2.
3. Plot the graphs of V_{out} vs V_{in} and V_{out} vs I_L.

4. Evaluate load and line regulations for the regulator.

Design Procedure

The design specifications for a voltage regulator include the desired DC output voltage, the maximum load current that is allowed to flow and the range of input voltage variation. For the given values of these design spec, use the following procedure.

1. Select a transistor Q such that it can handle the specified load current $I_{L.}$
2. Select a ZENER diode such that it can provide specified output voltage V_{out}. The zener voltage V_Z is selected using the equation:

$$\boldsymbol{V_Z = V_{out} + V_{BE}}$$

where V_{BE} can be noted from datasheet of Q

3. The value of the resistor can be designed by using the equation:

$$\boldsymbol{R = \frac{V_{R(min)}}{I_R} = \frac{V_{in(min)} - V_{Z(max)}}{I_R}}$$

where I_R is the current through **R** when the maximum load current $I_{L(max)}$ flows. I_R is given by:

$$\boldsymbol{I_R = I_{B(max)} + I_{Zt}}$$

where $I_{B(max)}$is the maximum base current that is made to flow through transistor Q and is given by:

$$\boldsymbol{I_{B(max)} = \frac{I_{E(max)}}{\beta_{min}} = \frac{I_{L(max)}}{\beta_{min}}}$$

where $I_{E(max)}$ is the maximum emitter current that is made to flow through Q and is equal to the maximum load current $I_{L(max)}$. Current gain β of Q can be noted for the datasheet. The current I_R must be enough to allow current I_{Zt} to follow through the ZENER diode such that:

$$\boldsymbol{I_{Zk} < I_{Zt} << I_{Z(max)}}$$

This will ensure that the ZENER diode operates in a safe reverse break-down region providing a constant zener voltage operation. Here I_{Zk} is the reverse knee current of the ZENER diode and $I_{Z(max)}$ is its maximum reverse current. I_{Zk} can be noted from the datasheet and $I_{Z(max)}$ is given by:

$$\boldsymbol{I_{Z(max)} = \frac{P_{Z(max)}}{V_{Z(max)}}}$$

Where $P_{Z(max)}$ is the power rating of ZENER diode given in its datasheet. Using the aforementioned procedure, fill the Table 1 and 2.

Load Regulation and Line Regulation are measured as follows:

Load Regulation= $\frac{\text{Change in } V_{out}}{\text{Mean } V_{out}}$, Line Regulation= $\frac{\text{Change in } V_{out}}{\text{Change in } V_{in}}$

Observations and Calculations:

Table 1. Load-regulation for V_{in} = 10V

$R_L(\Omega)$	V_{out}	$I_L = V_{out} / R_L$
1k		
1.5k		
10k		
100k		
Open circuit (∞)		

Load Regulation = _____

Table 2. Line-regulation

R_L = 1 kΩ		R_L = 10 kΩ	
V_{in}(V)	V_{out}	V_{in}	V_{out}
8			
10			
12			
14			
16			

Line Regulation = _____

POST LAB QUESTIONS:

1. Sketch all those waveforms mentioned in above experiment on your lab manual.
2. Plot V_{out} vs I_L curve using the data collected for the observation set no. 1 in your Lab Notebook.
3. Plot two V_{out} vs V_{in} curves (both on the same graph), one for the 100 Ω and the other for the 1.0 kΩ load.

EXPERIMENT 8

DESIGNING A VARIABLE VOLTAGE REGULATOR (OPEN-ENDED LAB)

Design a series variable-output linear voltage regulator using discrete circuit components to yield 5.0 V at the output. You can use additional BJT's and op-amps in the design. Outline the experimental procedure adopted to design and implement the aforementioned circuit. Investigate the circuit's regulation capability, load regulation, line regulation, and submit a detailed. For load-regulation, use an input of 10.0 V. For line regulation use a load of 1.0 kΩ.What can be done to provide short-circuit protection to the circuit?

Attach your lab results here.

EXPERIMENT 09

ANALYZING A BUCK REGULATOR

Objective

To understand the function of a fixed DC step-down switching (buck) regulator

Material and Equipment

1. Switching Regulator (LM2576-5)
2. Schottky Diode (1N4148)
3. Capacitors (100 µF, 1000µF, 2200 µF)
4. Inductor (100 µH)
5. Assorted resistors
6. Variable resistor of designed value
7. Digital Multimeter
8. DC Supply
9. Breadboard

Circuit Diagram

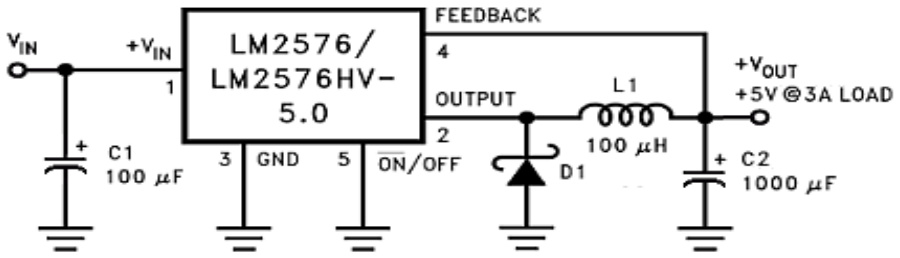


Figure 1. Buck regulator

Task

1. Connect the circuit of a switching step-down (BUCK) regulator as shown in Figure 1.
2. Given a particular value of V_{in}, V_{out} and I_L, select IC regulator capable of sustaining load current of 3 A and output voltage rating such that the combinations of inductor coil, capacitance and regulator voltages result in the required value of output voltage (as assigned by the instructor).

Observations and Calculations:

Table 1. Load-regulation for V_{in} = 10V

$R_L(\Omega)$	V_{out}	$I_L = V_{out} / R_L$
680		
1k		
1.2k		
1.5k		

Load Regulation = _____

Table 2. Line-regulation

R_L = 1kΩ		R_L = 1.5 kΩ	
V_{in}	V_{out}	V_{in}	V_{out}

Line Regulation = _____

POST LAB QUESTIONS:

1. Plot V_{out} vs I_L curve using the data collected for the observation set no. 1 and 3.
2. Plot V_{out} vs V_{in} curves (on the same graph), for load resistances between 10 Ω to 1.5 kΩ.
3. How can we convert it into an adjustable DC step-up switching (buck) regulator?

EXPERIMENT 10

ANALYZING A SINGLE-PHASE UNCONTROLLED HALF-WAVE RECTIFIER

Part 1:

Objective

- To practically analyze the working and performance of a single phase half-wave rectifier
- Observe the effect of inductive load on working of a rectifier

Material and Equipment

1. Diodes (1N4007)
2. Resistor(1 kΩ)
3. Inductor (150mH)
4. Signal Generator
5. Breadboard

Circuit Diagram 1

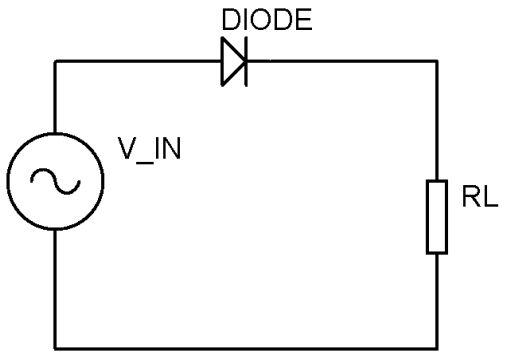


Figure 1. Half bridge rectifier

Task

1. Arrange the circuit as shown in Figure 1.
2. Take the output across the load resistance (1.0 kΩ – 5.6 kΩ)
3. Using signal generator to provide a sine-wave of 10 V_{P-P}, 500 Hz.
4. Sketch input voltage waveform
5. Sketch output voltage waveform
6. Sketch voltage waveform across the diode.

7. **Performance Parameters**

   Peak output Voltage = V_M = _____

   Average value of output voltage = $V_{DC} = 0.318V_M$ = _____

   Average value of output current = $I_{DC} = V_{DC} / R_L$ = _____

   RMS value of output voltage = $0.5V_M$ = _____

   RMS value of output current = $I_{rms} = V_{rms} / R_L$ = _____

   Output DC power = $P_{DC} = V_{DC} I_{DC}$ = _____

Circuit Diagram 2

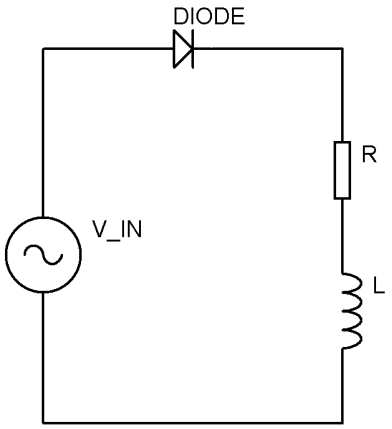


Figure 2. Half bridge rectifier with inductive load

Task

1. Arrange the circuit as shown in Figure 2.
2. Take the output across the load resistance (1.0 kΩ – 5.6 kΩ) and inductance (0.4 – 0.5 H)
3. Using signal generator, to provide a sine-wave of 10 V_{P-P}, 500 Hz.
4. Sketch output voltage waveform
5. Sketch voltage waveform across the diode

Circuit Diagram 3

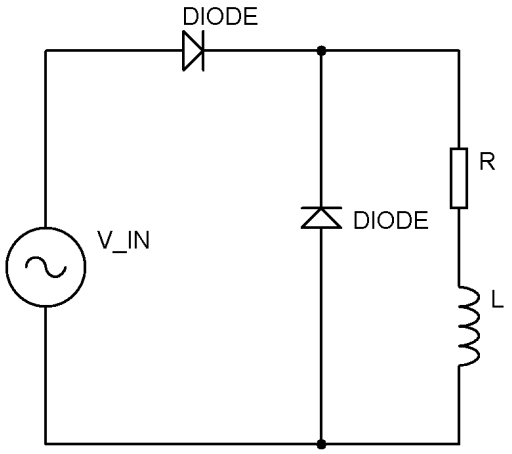


Figure 3. Half bridge rectifier with inductive load and free-wheeling diode

Task

1. Arrange the circuit as shown in Figure 3.
2. Take the output across the load resistance (1.0 kΩ – 5.6 kΩ) and inductance (0.4 – 0.5 H)
3. Using signal generator, provide a sine-wave of 10 V_{P-P}, 500 Hz.
4. Sketch output voltage waveform
5. Sketch voltage waveform across the main diode
6. Sketch voltage waveform across the free-wheeling diode

POST LAB QUESTIONS:

1. Sketch all those waveforms mentioned in above experiment on your lab manual
2. Explain the difference between output voltage waveforms for circuit 1 and 2.
3. Explain the difference between output voltage waveforms for circuit 2 and 3.

Part 2:

SINGLE-PHASE UNCONTROLLED FULL-WAVE RECTIFIER

Objective

- To practically analyze the working and performance of a single phase Full-Wave rectifier
- Observe the effect of inductive load on working of a rectifier

Material and Equipment

1. Diodes (1N4007)
2. Resistor (1 kΩ)
3. Inductor (150 mH)
4. 12V Transformer
5. Signal Generator
6. Breadboard

Circuit Diagram 1

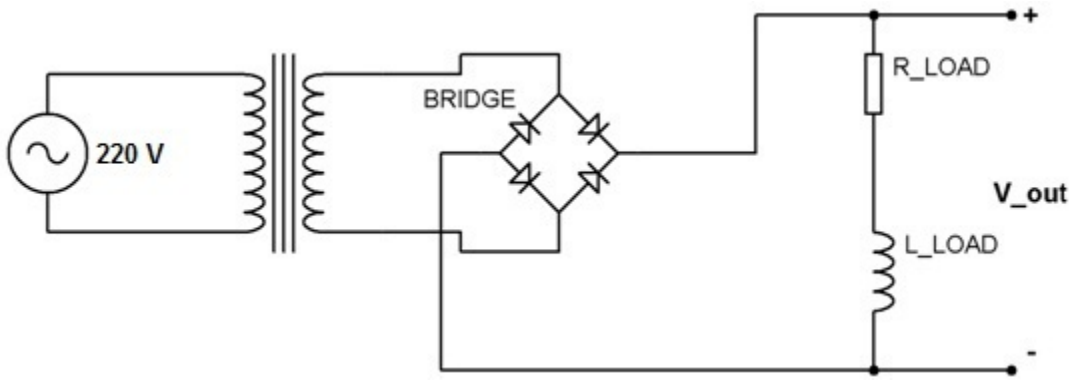


Figure 3. Full-wave rectifier

Task

1. Arrange the circuit as shown in Figure 3.
2. Take the output across the load resistance (1.0 kΩ – 5.6 kΩ) and inductance (0.4 – 0.5 H)
3. Sketch Output Voltage Waveform with Resistive Load only
4. Sketch Output Voltage Waveform with R-L Load

POST LAB QUESTIONS:

1. Sketch all the waveforms mentioned in above experiment on your lab manual.
2. Explain the difference between output voltage waveforms for different kind of loads used in the experiments.

Attach your lab results here.

EXPERIMENT 11

IMPLEMENTATION OF A HALF WAVE RECTIFIER USING R AND RC TRIGGERING

Part 1:

Objective

To practically analyze the resistive firing/triggering of a silicon controlled rectifier (SCR)

Material and Equipment

1. Diodes (1N4007)
2. SCR (MCR 100-6)
3. Assorted resistors (820 Ω, 10 kΩ)
4. Variable resistor (1.0MΩ)
5. Signal Generator
6. Oscilloscope
7. Breadboard

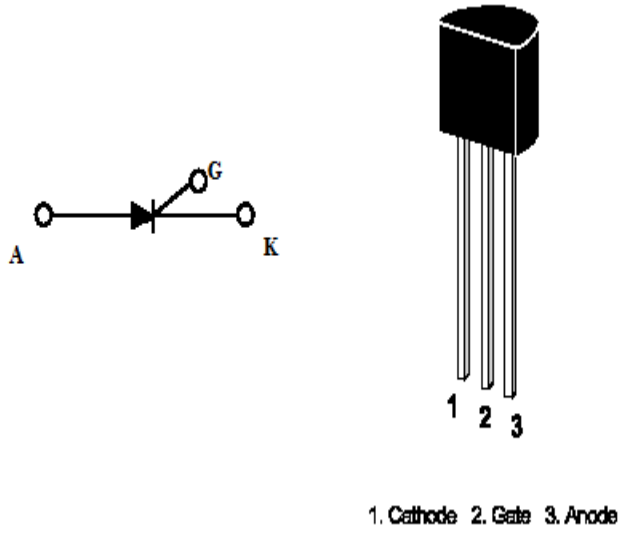


Figure 1. Pin configuration of SCR

Circuit Diagram 1

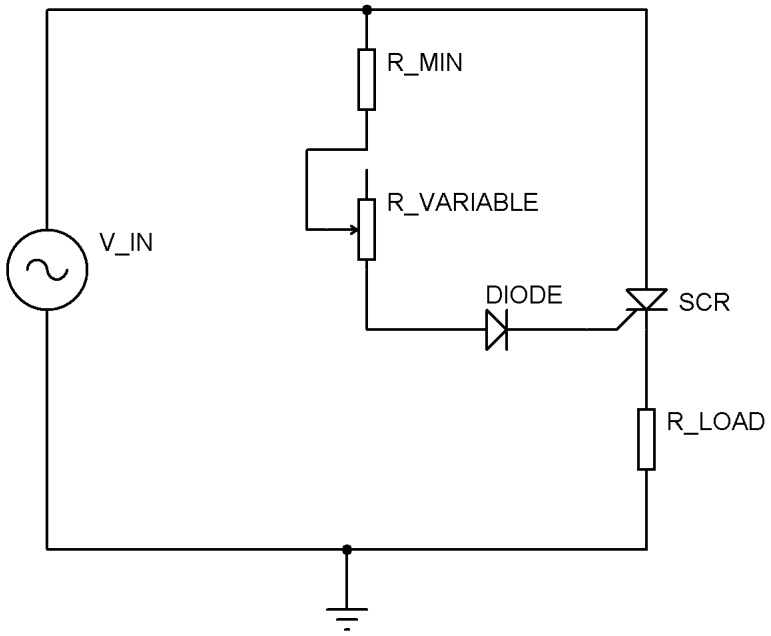


Figure 2. Half wave rectifier using R-triggering

Design Procedure

1. Arrange the circuit as shown in Figure 2. Use the pin configuration shown in Figure 1.
2. The R_{min} can be found using the following formula,
   a. $R_{min} = \frac{V_{S(max)}}{I_{g(max)}} =$
3. The $R_{variable}$ can be found using the following formula,
   a. $R_{variable} + R_{min} \leq \frac{V_S - V_{G(min)} - V_D}{I_G} =$
   b. The maximum current that can flow through the gate of the SCR is 200 µA – 250 µA. The minimum current that can flow through the SCR is 50 µA - 80µA.
4. Using signal generator, provide a sine-wave of 10 V_{P-P}, 50 Hz at the input of the circuit.
5. Connect a resistance of 820 Ω as the load.
6. Initially, keep the variable resistors to its maximum value so that the I_G is very small.
7. Decrease the gate resistance such that the SCR is fired as shown in Figure 3.
8. Record your observations in Table 1 for at least 5 different firing angles over the entire range of observations. Set the DMM to measure DC voltage across the load.
9. Find $V_{out\ (DC)}$ (theoretical) using the following expressions.

$$V_{out(DC)} = \frac{V_P}{2\pi}(1 + \cos\theta) \qquad \text{and} \qquad Firing\ Angle\ (\theta) = sin^{-1}(\frac{V_x}{V_p})$$

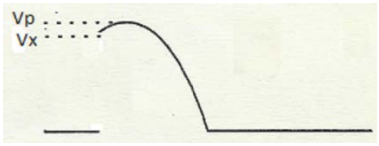


Figure 3. Firing angle waveform

Observations and Calculations

Table 1. Output-voltage response

Sr. No.	Firing Angle	V_{out}(practical)	V_{out}(theoretical)
1			
2			
3			
4			
5			

10. Sketch Output Voltage Waveform across the load resistance for firing angle in reading 2
11. Sketch Voltage Waveform across the SCR for firing angle used in the above waveform.
12. Sketch Output Voltage Waveform across the load resistance for firing angle in reading 4
13. Sketch Voltage Waveform across the SCR for firing angle used in the above waveform.

POST LAB QUESTIONS:

1. What is the effect of R-triggering on the performance of half wave rectifier?
2. Sketch all those waveforms mentioned in above experiment in your lab notebooks.
3. Explain the difference that you observe in output voltage waveforms for different firing angles.

Part 2:

HALF WAVE RECTIFIER USING RC-TRIGGERING

Objective

To practically analyze the resistive-capacitive firing/triggering of a silicon controlled rectifier (SCR)

Material and Equipment

1. Diodes (1N4007)
2. SCR (MCR 100-6)
3. Capacitance (0.1 µF non-polar)
4. Assorted resistors(820 Ω, 10 kΩ)
5. 1.0MΩ variable resistor
6. Signal Generator
7. Oscilloscope
8. Breadboard

Circuit Diagram 1

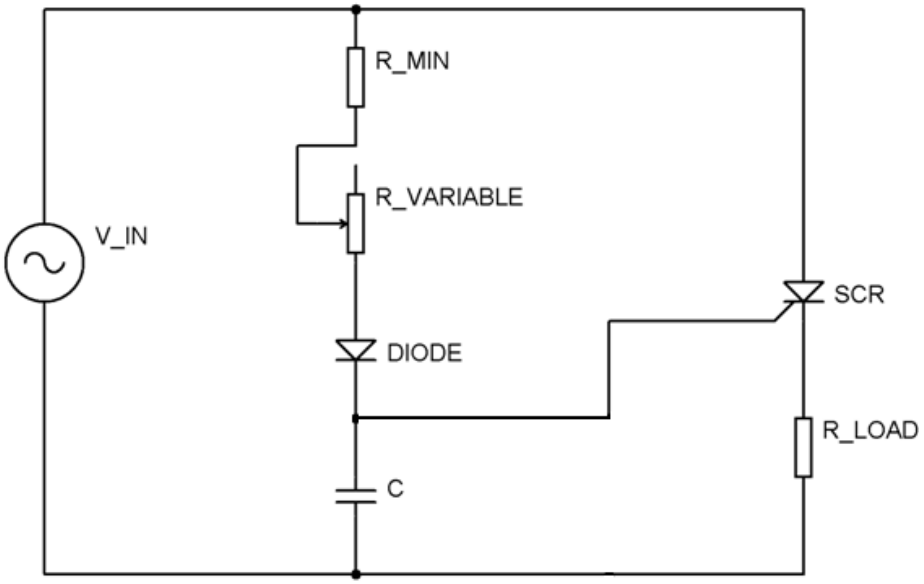


Figure 4. Half wave rectifier using RC-triggering

Design Procedure

1. Arrange the circuit as shown in Figure 4.
2. The R_{min} can be found using the following formula,
   a. $R_{min} = \frac{V_{S(max)}}{I_{g(max)}} =$
3. The $R_{variable}$ can be found using the following formula,
   a. $R_{variable} + R_{min} \leq \frac{V_S - V_{G(min)} - V_D}{I_G} =$
   b. The maximum current that can flow through the gate of the SCR is 200 µA – 250 µA. The minimum current that can flow through the SCR is 50 µA - 80µA.
4. Using signal generator, provide a sine-wave of 10 $V_{P\text{-}P}$, 50 Hz at the input of the circuit.
5. Add a resistance of 820 Ω as the load.
6. Initially, keep the variable resistors to its maximum value so that the I_G is very small.
7. Decrease the gate resistance such that the SCR is fired as shown in Figure 5.
8. Record your observations in Table 2 for at least 5 different firing angles over the entire range of observations. Set the DMM to measure DC voltage across the load.
9. Find $V_{out(DC)}$ (theoretical) using the following expressions.

$$V_{out(DC)} = \frac{V_P}{2\pi}(1 + \cos\theta)$$

$$Firing\ Angles:$$

$$\theta = sin^{-1}(\frac{V_x}{V_p})$$

$$\theta = 180^{\circ} - sin^{-1}(\frac{V_x}{V_p})\text{(for firing angles greater than } 90^{\circ}\text{)}$$

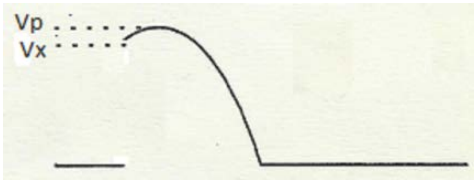


Figure 5. Firing angle waveform

Observations and Calculations

Table 2. Output-voltage response

Sr. No.	Firing Angle	V_{out}(practical)	V_{out}(theoretical)
1			
2			
3			
4			
5			

10. Sketch output voltage waveform across the load resistance for firing angle in reading 2
11. Sketch voltage waveform across the SCR for firing angle used in the above waveform.
12. Sketch output voltage waveform across the load resistance for firing angle in reading 4
13. Sketch voltage waveform across the SCR for firing angle used in the above waveform.

POST LAB QUESTIONS:

1. What is the effect of RC-Triggering on the performance of half wave rectifier?
2. Sketch the waveforms mentioned in above experiment in your lab notebooks neat and clean.
3. Explain the difference that you observe in output voltage waveforms for different firing angles.

Attach your lab results here.

EXPERIMENT 12

IMPLEMENTATION OF A FULL WAVE RECTIFIER USING R AND RC TRIGGERING

Part 1:

Objective

To practically analyze the resistive-capacitive firing/triggering of a silicon controlled rectifier (SCR)

Material and Equipment

1. PN Junction Diodes (1N4007)
2. SCR (MCR 100-6)
3. Assorted resistors(820 Ω,10 kΩ)
4. 1.0MΩ variable resistor
5. 12V Transformer
6. Signal Generator
7. Oscilloscope
8. Breadboard

Circuit Diagram

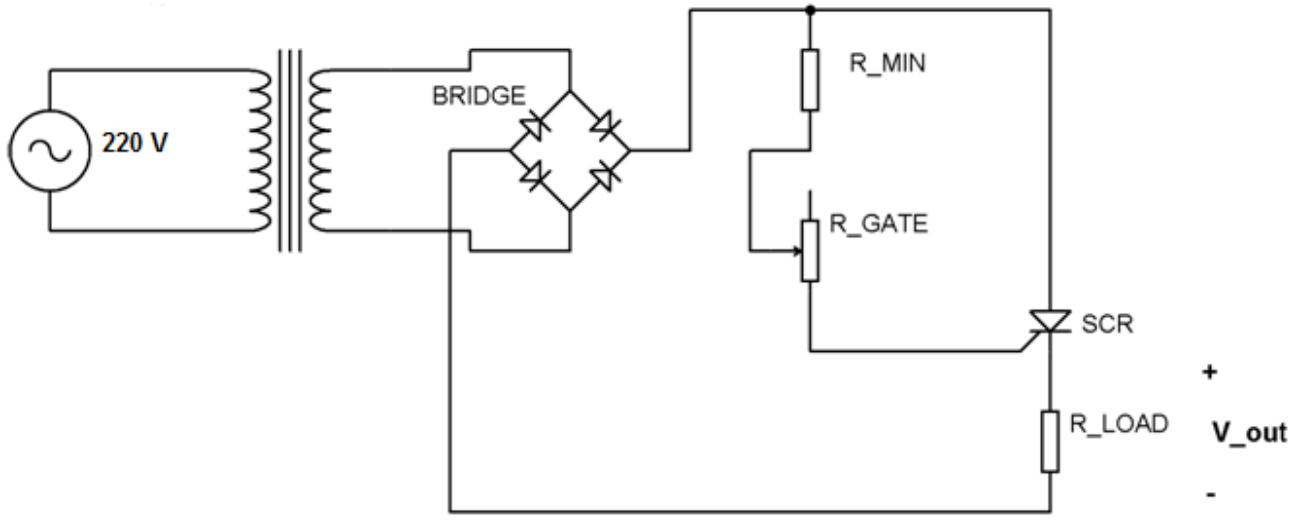


Figure 1. Full wave rectifier using R-triggering

Design Procedure

1. Arrange the circuit as shown in Figure 1.
2. The R_{min} can be found using the following formula,
   a. $R_{min} = \frac{V_{S(max)}}{I_{g(max)}} =$
3. The $R_{variable}$ can be found using the following formula,
   a. $R_{variable} + R_{min} \leq \frac{V_S - V_{G(min)}}{I_G} =$
   b. The maximum current that can flow through the gate of the SCR is 200 µA – 250 µA. The minimum current that can flow through the SCR is 50 µA - 80µA.
4. Using signal generator, provide a sine-wave of 10 V_{P-P} at 50 Hz at the input of the circuit.
5. Add a resistance of 820 Ω as the load.
6. Initially, keep the variable resistors to its maximum value so that the I_G is very small.
7. Decrease the gate resistance such that the SCR is fired as shown in Figure 2.
8. Record your observations in Table 1 for at least 5 different firing angles over the entire range of observations. Set the DMM to measure DC voltage across the load.
9. Find $V_{out(DC)}$ (theoretical) using the following expressions.

$$V_{out(DC)} = \frac{V_P}{\pi}(1 + \cos\theta) \qquad \text{and} \qquad Firing\ Angle\ (\theta) = sin^{-1}(\frac{V_x}{V_p})$$

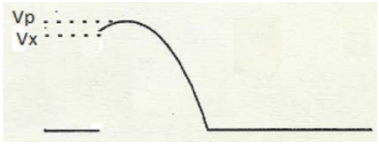


Figure 2. Firing angle waveform

Observations and Calculations

Table 1. Output-voltage response

Sr. No.	Firing Angle	V_{out}(practical)	V_{out}(theoretical)
1			
2			
3			
4			
5			

10. Sketch output voltage waveform across the load resistance for firing angle in reading 2
11. Sketch voltage waveform across the SCR for firing angle used in the above waveform.
12. Sketch output voltage waveform across the load resistance for firing angle in reading 4
13. Sketch voltage waveform across the SCR for firing angle used in the above waveform.

POST LAB QUESTIONS:

1. What is the effect of R-Triggering on the performance of full wave rectifier?
2. Sketch the waveforms mentioned in above experiment in your lab notebooks.
3. Explain the difference that you observe in output voltage waveforms for different firing angles.

Part 2

FULL WAVE RECTIFIER USING RC-TRIGGERING

Objective

To practically analyze the full-wave resistive-capacitive firing/triggering of a silicon controlled rectifier (SCR)

Material and Equipment

1. PN Junction Diodes (1N4007)
2. SCR (MCR 100-6)
3. Capacitance (0.1 µF, non-polar)
4. Assorted resistors(820 Ω, 10 kΩ)
5. 1.0MΩ variable resistor
6. 12V Transformer
7. Signal Generator
8. Oscilloscope
9. Breadboard

Circuit Diagram

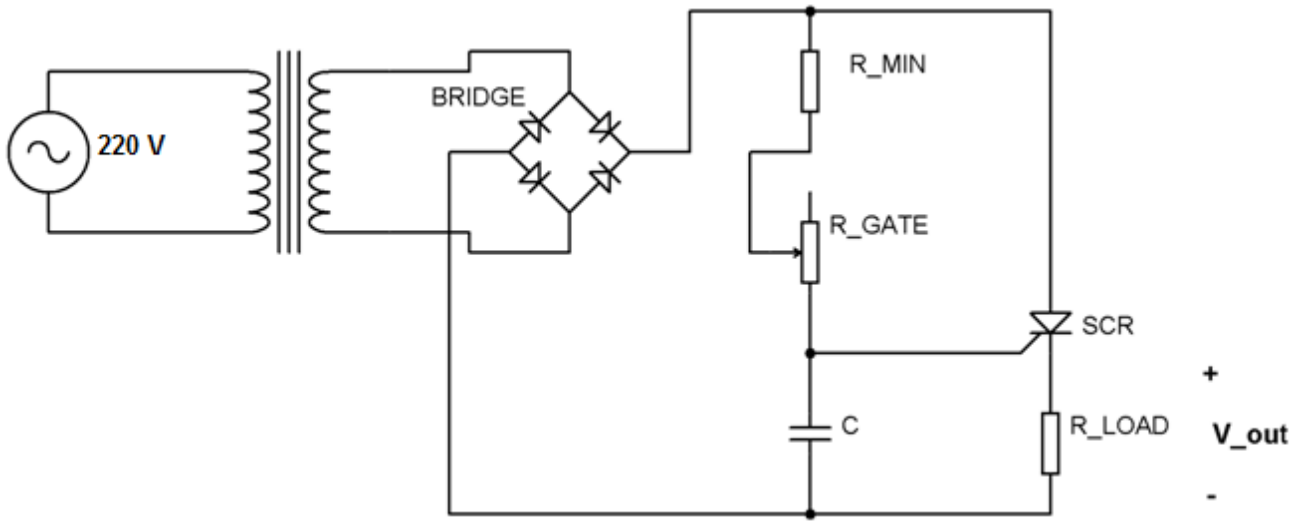


Figure 3. Full wave rectifier using RC-triggering

Design Procedure

2. Arrange the circuit as shown in Figure 3.
3. The R_{min} can be found using the following formula,
   a. $R_{min} = \frac{V_{S(max)}}{I_{g(max)}} =$
4. The $R_{variable}$ can be found using the following formula,
   a. $R_{variable} + R_{min} \leq \frac{V_S - V_{G(min)}}{I_G} =$
   b. The maximum current that can flow through the gate of the SCR is 200 µA – 250 µA. The minimum current that can flow through the SCR is 50 µA - 80µA.
5. Using signal generator, provide a sine-wave of 10 V_{P-P} at 50 Hz at the input of the circuit.
6. Connect a resistance of 820 **Ω** as the load.
7. Initially, keep the variable resistors to its maximum value so that the I_G is very small.
8. Decrease the gate resistance such that the SCR is fired as shown in Figure 4.
9. Record your observations in Table 2 for at least 5 different firing angles over the entire range of observations. Set the DMM to measure DC voltage across the load.
10. Find $V_{out(DC)}$ (theoretical) using,

$$V_{out(DC)} = \frac{V_P}{\pi}(1 + \cos\theta)$$

$$Firing\ Angles:$$

$$\theta = sin^{-1}(\frac{V_x}{V_p})$$

$$\theta = 180^{\circ} - sin^{-1}(\frac{V_x}{V_p}) \quad \text{(for firing angles greater than } 90^{\circ})$$

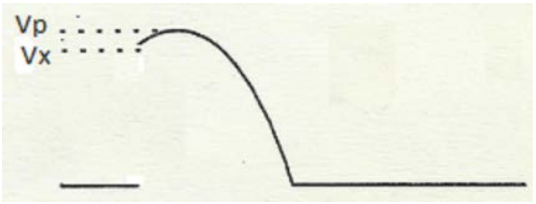


Figure 4. Firing angle waveform

Observations and Calculations

Table 2. Output-voltage response

S.no.	Firing Angle	V_{out}(practical)	V_{out}(theoretical)
1			
2			
3			
4			
5			

11. Sketch output voltage waveform across the load resistance for firing angle in reading 2.
12. Sketch voltage waveform across the SCR for firing angle used in the above waveform.
13. Sketch output voltage waveform across the load resistance for firing angle in reading 4.
14. Sketch voltage waveform across the SCR for firing angle used in the above waveform.

POST LAB QUESTIONS:

1. What is the effect of RC-Triggering on the performance of full wave rectifier?
2. Sketch all those waveforms mentioned in above experiment in your lab notebooks.
3. Explain the difference that you observe in the output voltage waveforms for different firing angles.

Attach your lab results here.

EXPERIMENT 13

ANALYZING A THREE-PHASE HALF-WAVE RECTIFIER

Objective

To practically analyze the working and performance of a three phase Half-Wave rectifier

Material and Equipment

1. Diodes (1N4007)
2. Resistor(1 kΩ)
3. Signal Generator
4. Breadboard

Explanation:

The diode in a particular phase conducts during the period, when voltage on that phase is higher than those on the other two phases. Unlike single phase rectifier circuit, the conduction angle of each diode is $\frac{2\pi}{3}$instead ofπ. If diode D conducts from $\frac{\pi}{6}$to $\frac{5\pi}{6}$. therefore using following equation average value can be found as

$$V_{dc} = \frac{3}{2\pi}\int_{\frac{\pi}{6}}^{\frac{5\pi}{6}} V_m \sin\theta d\theta$$

$$V_{dc} = V_m \frac{3}{\pi}\frac{\sqrt{3}}{2} = 0.827\ V_m$$

Circuit Diagram

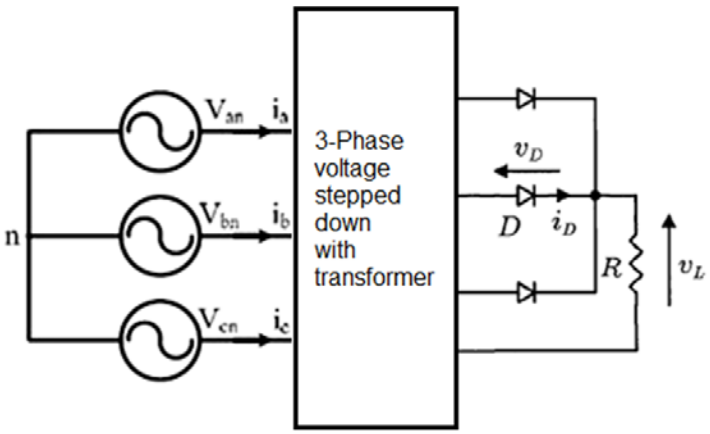


Figure 1. Three-phase half-wave rectifier

Task

1. Arrange the circuit as shown in Figure 1.
2. Take the output across the load resistance (1.0 kΩ – 5.6 kΩ)
3. Sketch input voltage waveform
4. Sketch output voltage waveform
5. Sketch voltage waveform across the diode

Performance Parameters

Peak output Voltage = V_M = _____

Average value of output voltage = $V_{DC} = 0.827V_M$ = _____

Average value of output current = $I_{DC} = V_{DC} / R_L$ = _____

RMS value of output voltage = $0.84V_M$ = _____

RMS value of output current = $I_{rms} = V_{rms} / R_L$ = _____

Output DC power = $P_{DC} = V_{DC} I_{DC}$ = _____

Draw Three-phase output waveform across the load.

POST LAB QUESTIONS:

1. Sketch all the waveforms mentioned in above experiment in your lab notebooks.
2. Plot the voltage waveforms for each phase and the load.
3. Why the conduction angle of each diode is $\frac{2\pi}{3}$instead ofπ ?

Attach your lab results here.

EXPERIMENT 14

ANALYZING A THREE-PHASE BRIDGE RECTIFIER

Objective

To practically analyze the working and performance of a three phase bridge rectifier

Equipment

1. Diodes (1N4007)
2. Resistor (1 kΩ)
3. Three phase power supply
4. Step down transformers
5. Oscilloscope
6. Breadboard, Connecting wires

Three-Phase Full Wave rectifiers

The three-phase bridge rectifiers are commonly used for high power applications because they have the highest possible transformer utilization factor for a three phase system. The circuit diagram of a three-phase full-wave diode rectifier is shown in Figure 1.

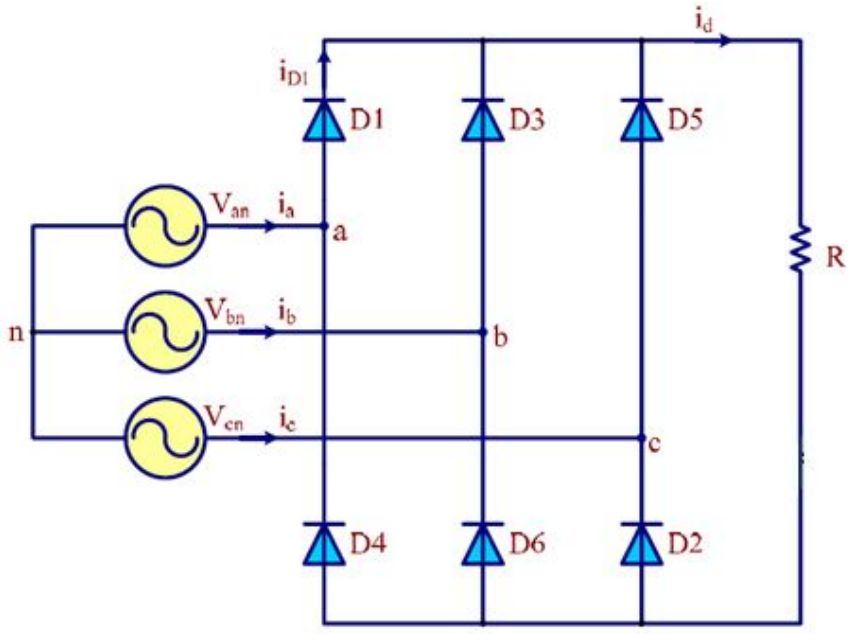


Figure 1. Three-phase full-wave bridge rectifier

The performance parameters of the rectifier with a purely resistive load are given by:

1. RMS input voltage, V_s.
2. Peak input voltage,$V_m = \sqrt{2}V_s$
3. Supply frequency, f_s
4. $v_{an} = V_m \sin(\omega t); v_{bn} = V_m \sin(\omega t - 120^o); v_{cn} = V_m \sin(\omega t - 240^o);$
5. $v_{ab} = 3\,V_m \sin(\omega t + 30^o); v_{bc} = 3\,V_m \sin(\omega t - 90^o); v_{ca} = 3\,V_m \sin(\omega t + 90^o);$
6. Average value of the output (load) voltage,

$$\mathbf{V_{DC} = \frac{2}{2\pi/6}\int_0^{\pi/6} \sqrt{3}\,V_m \cos(\omega t)\,.\,d(\omega t) = \frac{3\sqrt{3}}{\pi}V_m = 1.654\,V_m}$$

7. Average value of the output (load) current,

$$\mathbf{I_{o(dc)} = V_{o(dc)} / R = 1.654\,V_m/R}$$

8. Output DC power, $\mathbf{P_{o(dc)} = V_{o(dc)}\,.I_{o(dc)}}$
9. RMS value of the output voltage,

$$\mathbf{V_{o(rms)} = \left(\frac{3}{2} + \frac{9\sqrt{3}}{4\pi}\right)^{1/2} V_m = 1.6554\,V_m}$$

10. RMS value of the output current, $\mathbf{I_{o(rms)} = V_{o(rms)}/R = 1.6554\,V_m/R.}$

Circuit Diagram

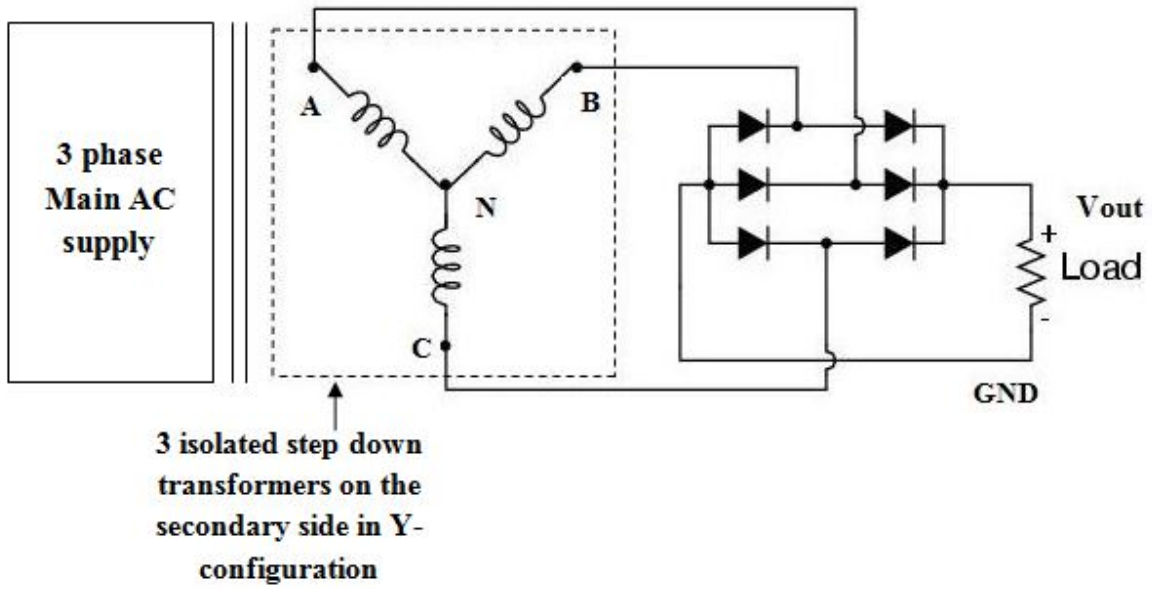


Figure 2. Three-phase full-wave bridge rectifier circuit diagram for implementation

Procedure

1. Arrange the circuit as shown in Figure 2. Use the three step down transformers and connect them on the secondary side in Y-configuration as shown in figure.
2. Take the output across the load resistance (1 kΩ - 5.6 kΩ)
3. View the output voltage (Vout) across the load on the oscilloscope and sketch the waveform.
4. Observe two phases of the input from transformers by viewing them simultaneously on the oscilloscope. Calculate the phase difference between the waveforms.

Performance Parameters

Peak output Voltage = V_M = _____

Average value of output voltage = $V_{DC} = 1.654V_M$ = _____

Average value of output current = $I_{DC} = V_{DC} / R_L$ = _____

RMS value of output voltage = $V_{rms} = 1.6554V_M$ = _____

RMS value of output current = $I_{rms} = V_{rms}/ R_L$ = _____

Output DC power = $P_{DC} = V_{DC}.I_{DC}$ = _____

Draw Three-phase output waveform across the load.

Waveform:

POST LAB QUESTIONS:

Compare the performance of a three phase bridge rectifier and the three phase half-wave rectifier of Experiment 13.

Attach your lab results here.

Appendix A: Lab Evaluation Criteria

Labs with projects

1. Class Participation 10%
2. Lab Work 40%
3. Quiz (2) 20%
4. Project 30%
    a. Project Demonstration 20%
    b. Project Report 5%
    c. Project Quiz 5%

Labs without projects

1. Class Participation 10%
2. Lab Work 40%
3. Quiz (2) 20%
4. Lab Final 30%
    a. Lab Final (Practical) 20%
    b. Lab Final (Written) 10%

Appendix B: Safety around Electricity

In all the Electrical Engineering (EE) labs, with an aim to prevent any unforeseen accidents during conduct of lab experiments, following preventive measures and safe practices shall be adopted:

- Remember that the voltage of the electricity and the available electrical current in EE labs has enough power to cause death/injury by electrocution. It is around 50V/10 mA that the "cannot let go" level is reached. "The key to survival is to decrease our exposure to energized circuits."
- If a person touches an energized bare wire or faulty equipment while grounded, electricity will instantly pass through the body to the ground, causing a harmful, potentially fatal, shock.
- Each circuit must be protected by a fuse or circuit breaker that will blow or "trip" when its safe carrying capacity is surpassed. If a fuse blows or circuit breaker trips repeatedly while in normal use (not overloaded), check for shorts and other faults in the line or devices. Do not resume use until the trouble is fixed.
- It is hazardous to overload electrical circuits by using extension cords and multi-plug outlets. Use extension cords only when necessary and make sure they are heavy enough for the job. Avoid creating an "octopus" by inserting several plugs into a multi-plug outlet connected to a single wall outlet. Extension cords should ONLY be used on a temporary basis in situations where fixed wiring is not feasible.
- Dimmed lights, reduced output from heaters and poor monitor pictures are all symptoms of an overloaded circuit. Keep the total load at any one time safely below maximum capacity.
- If wires are exposed, they may cause a shock to a person who comes into contact with them. Cords should not be hung on nails, run over or wrapped around objects, knotted or twisted. This may break the wire or insulation. Short circuits are usually caused by bare wires touching due to breakdown of insulation. Electrical tape or any other kind of tape is not adequate for insulation!
- Electrical cords should be examined visually before use for external defects such as: Fraying (worn out) and exposed wiring, loose parts, deformed or missing parts, damage to outer jacket or insulation, evidence of internal damage such as pinched or crushed outer jacket. If any defects are found the electric cords should be removed from service immediately.
- Pull the plug not the cord. Pulling the cord could break a wire, causing a short circuit.
- Plug your heavy current consuming or any other large appliances into an outlet that is not shared with other appliances. Do not tamper with fuses as this is a potential fire hazard. Do not overload circuits as this may cause the wires to heat and ignite insulation or other combustibles.
- Keep lab equipment properly cleaned and maintained.
- Ensure lamps are free from contact with flammable material. Always use lights bulbs with the recommended wattage for your lamp and equipment.
- Be aware of the odor of burning plastic or wire.
- ALWAYS follow the manufacturer recommendations when using or installing new lab equipment. Wiring installations should always be made by a licensed electrician or other qualified person. All electrical lab equipment should have the label of a testing laboratory.
- Be aware of missing ground prong and outlet cover, pinched wires, damaged casings on electrical outlets.
- Inform Lab engineer / Lab assistant of any failure of safety preventive measures and safe practices as soon you notice it. Be alert and proceed with caution at all times in the laboratory.
- Conduct yourself in a responsible manner at all times in the EE Labs.

- Follow all written and verbal instructions carefully. If you do not understand a direction or part of a procedure, ASK YOUR LAB ENGINEER / LAB ASSISTANT BEFORE PROCEEDING WITH THE ACTIVITY.
- Never work alone in the laboratory. No student may work in EE Labs without the presence of the Lab engineer / Lab assistant.
- Perform only those experiments authorized by your teacher. Carefully follow all instructions, both written and oral. Unauthorized experiments are not allowed.
- Be prepared for your work in the EE Labs. Read all procedures thoroughly before entering the laboratory. Never fool around in the laboratory. Horseplay, practical jokes, and pranks are dangerous and prohibited.
- Always work in a well-ventilated area.
- Observe good housekeeping practices. Work areas should be kept clean and tidy at all times.
- Experiments must be personally monitored at all times. Do not wander around the room, distract other students, startle other students or interfere with the laboratory experiments of others.
- Dress properly during a laboratory activity. Long hair, dangling jewelry, and loose or baggy clothing are a hazard in the laboratory. Long hair must be tied back, and dangling jewelry and baggy clothing must be secured. Shoes must completely cover the foot.
- Know the locations and operating procedures of all safety equipment including fire extinguisher. Know what to do if there is a fire during a lab period; "Turn off equipment, if possible and exit EE lab immediately."