Interrupt	Flag bit (Register)	Enable bit (Register)	Priority (Register)
Timer0	TMR0IF (INTCON)	TMR0IE (INTCON)	TMR0IP (INTCON2)
Timer1	TMR1IF (PIR1)	TMR1IE (PIE1)	TMR1IP (IPR1)
Timer2	TMR2IF (PIR1)	TMR2IE (PIE1)	TMR2IP (IPR1)
Timer3	TMR3IF (PIR3)	TMR3IE (PIE2)	TMR3IP (IPR2)
INT1	INT1IF (PIR1)	INT1IE (PIE1)	INT1IP (INTCON3)
INT2	INT2IF (PIR1)	INT2IE (PIE1)	INT2IP (INTCON)
TXIF	TXIF (PIR1)	TXIE (PIE1)	TXIP (IPR1)
RCIF	RCIF (PIR1)	RCIE (PIE1)	RCIP (IPR1)

R/W-0	U-0	U-0	R/W-1	R-1	R-1	R/W-0	R/W-0
IPEN	—	—	$\overline{RI}$	$\overline{TO}$	$\overline{PD}$	$\overline{POR}$	$\overline{BOR}$

EEPGD	CFGS	--	FREE	WRERR	WERN	WR#	RD#

RCON register bits

INTCON REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x
GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF
bit 7							bit 0

	INTEDG0	INTEDG1	INTEDG2				

INTCON2 Register

1.

TMR0ON	T08BIT	T0CS	T0SE	PSA	T0PS2	T0PS1	T0PS0

TMR0ON D7 Timer0 ON and OFF control bit
1 = Enable (start) Timer0
0 = Stop Timer0

T08BIT D6 Timer0 8-bit/16-bit selector bit
1 = Timer0 is configured as an 8-bit timer/counter.
0 = Timer0 is configured as a 16-bit timer/counter.

T0CS D5 Timer0 clock source select bit
1 = External clock from RA4/T0CKI pin
0 = Internal clock (Fosc/4 from XTAL oscillator)

T0SE D4 Timer0 source edge select bit
1 = Increment on H-to-L transition on T0CKI pin
0 = Increment on L-to-H transition on T0CKI pin

PSA D3 Timer0 prescaler assignment bit
1 = Timer0 clock input bypasses prescaler.
0 = Timer0 clock input comes from prescaler output.

T0PS2:T0PS0 D2D1D0 Timer0 prescaler selector

0 0 0 = 1:2	Prescale value (Fosc / 4 / 2)
0 0 1 = 1:4	Prescale value (Fosc / 4 / 4)
0 1 0 = 1:8	Prescale value (Fosc / 4 / 8)
0 1 1 = 1:16	Prescale value (Fosc / 4 / 16)
1 0 0 = 1:32	Prescale value (Fosc / 4 / 32)
1 0 1 = 1:64	Prescale value (Fosc / 4 / 64)
1 1 0 = 1:128	Prescale value (Fosc / 4 / 128)
1 1 1 = 1:256	Prescale value (Fosc / 4 / 256)

RD16	—	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR1ON

RD16 D7 16-bit read/write enable bit
1 = Timer1 16-bit is accessible in one 16-bit operation.
0 = Timer1 16-bit is accessible in two 8-bit operations.

D6 Not used

T1CKPS2:T1CKPS0 D5 D4 Timer1 prescaler selector

0 0 = 1:1	Prescale value
0 1 = 1:2	Prescale value
1 0 = 1:4	Prescale value
1 1 = 1:8	Prescale value

T1OSCEN D3 Timer1 oscillator enable bit
1 = Timer1 oscillator is enabled.
0 = Timer1 oscillator is shutoff.

T1SYNC D2 Timer1 synchronization (used only when TMR1CS = 1 for counter mode to synchronize external clock input)
If TMR1CS = 0 this bit is not used.

TMR1CS D1 Timer1 clock source select bit
1 = External clock from pin RC0/T1CKI
0 = Internal clock (Fosc/4 from XTAL)

TMR1ON D0 Timer1 ON and OFF control bit
1 = Enable (start) Timer1
0 = Stop Timer1

Figure 9-10. T1CON (Timer 1 Control) Register

- `ADDLW Literal`
- `ANDLW Literal`
- `SUBLW Literal`
- `XORLW Literal`
- `MULLW Literal`
- `ADDWF fileReg, d`

- ADDWFC fileReg, d
- ANDWF fileReg, d
- IORWF fileReg, d
- SUBWFB fileReg, d
- SUBWF fileReg, d
- SUBWFB fileReg, d
- XORWF fileReg, d
- COMF fileReg, d
- DECF fileReg, d
- DECFSZ fileReg, d
- DECFSNZ fileReg, d
- INCF fileReg, d
- INCFSZ fileReg, d
- INCSNZ fileReg, d
- MOVF fileReg, d
- NEGF fileReg, d
- RLCF fileReg, d
- RNCF fileReg, d
- RRCF fileReg, d
- RRNCF fileReg, d
- SWAPF fileReg, d

- BTSC fileReg, bit
- BSF fileReg, bit
- BCF fileReg, bit
- MOVFF fileReg1, fileReg2
- GOTO addr
- BTFSC fileReg, bit
- BTFSS fileReg, bit
- CALL addr
- RCALL addr
- RETURN
- RETFIE
- NOP
- CLRF fileReg
- CLRW
- SETF fileReg
- STATUS
- C - Carry flag
- DC - Digital Carry flag
- Z - Zero flag
- OV - Overflow flag
- N - Negative flag

- CPFSGT fileReg, d
- CPFSEQ fileReg, d
- CPFSLT fileReg, d
- VAR_NAME EQU Literal/Location
- ORG
- BTG fileReg, bit

Interrupt	Flag bit	Register	Enable bit	Register
Timer0	TMR0IF	INTCON	TMR0IE	INTCON
Timer1	TMR1IF	PIR1	TMR1IE	PIE1
Timer2	TMR2IF	PIR1	TMR2IE	PIE1
Timer3	TMR3IF	PIR3	TMR3IE	PIE2
INT0 (RB0)	INT0IF	INTCON	INT0IE	INTCON
INT1 (RB1)	INT1IF	INTCON3	INT1IE	INTCON3
INT2 (RB2)	INT2IF	INTCON3	INT2IE	INTCON3
TXIF (Transmit)	TXIF	PIR1	TXIE	PIE1
RCIF (Receive)	RCIF	PIR1	RCIE	PIE1
High Priority	0008H			
Low Priority	0018H			