

McGill University

ECSE 415 PROJECT

Cat and Dog

Jaeho Lee 260633759

Raymond So 260640297

Team name: You thought it was an original team name, but it was me, DIO!

submitting to Prof. James CLARK

ECSE 415 Project Cat and Dog

Jaeho Lee * and Raymond So †
Department of Electrical Engineering, McGill University
*jaeho.lee2@mail.mcgill.ca, †raymond.su@mail.mcgill.ca

1. Introduction

Most research for object classification was more focused on classifying images that are completely different (ex. horse and ship). In this project, we classify whether the image contains a picture of dog or cat. We were given 5906 images from [Cat and Dog paper]. We trained animal body detection and classification using 1500 images of cat and dog each. We used Haar features to detect the portion of the image containing the animal. Computation of the LBP histogram provides feature of the image for the classification. And then, we used SVM to define whether the image contains dogs or cats.

2. Problem Representation

The goal of this project is to devise a machine learning algorithm to analyse images and classify them to their respective categories. The datasets for training and testing, which consist of 7384 images, were given from [kaggle website]. The ratio of dog and cat images in given dataset was 2:1. In order to fix training bias due to data inequality, we used external dataset from [cat face] which includes 4004 cat face, and 2271 cat ear images.

In order to tackle this problem, we built face detection and body detection in order to limit features to classify. Face detection is prior to be classified because it is easier and more accurate to classify if the detection system can detect face. If we include the entire body, there are numerous different data exists depends on gesture of the animal and photo inclusion of the animal (i.e photo includes only face, chest and up or the entire body). In [McGill Cat and Dog project paper], using classification based on face detection performed better than body detection. We used Haar feature detection from [Viola and Jones 2001] for both face detection and body detection

We used Local Binary Pattern (LBP) histogram from [LBP paper] to extract histogram data for classification. Consider we are using face detection, LBP histogram has advantage of face classification because LBP is fast and proven to perform well in classification based on face feature [LBP face detection]. After extract histogram data, Linear Support

Vector Machine (LSVM) was used to classify whether the image includes cat or dog.

3. Algorithm selection and implementation

For object detection, we used Haar feature detection from [Viola and Jones 2001] for cascade trainer. Haar feature detection was chosen because we prior to use face detection and Haar performs fast and accurately [Viola Jones 2001]. We used pre-built OpenCV annotation program to select face and body region from the image. For body detection training, we used 3000 images from [kaggle website] dataset. For face detection training, we used 8000 images from [kaggle website] and [cat face] dataset. A vector file of image data was created before training in order to store annotated image data. After creating vector file, we trained the cascade to create a xml file. We used 14 stages for face detection and 17 stages for body detection. Before detect the face with test image, we use Gaussian filter to simplify features which increases detecting performance. Figure 1 addresses succeed and failed face detection example, figure 2 addresses succeed and failed body detection example.

After object detection, we use LBP from [LBP paper] and get histogram of face or body part. If the face detection program failed to detect face, body detection activates instead. We trained 2804 images for LBP from [kaggle website]. Single cell LBP was used because consider the face detection succeed, the image indicates the face of dog/cat is very small, therefore it would not be worth to use multiple cell LBP.

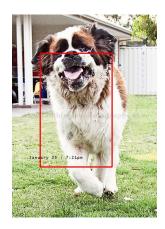
LSVM from sklearn library [sklearn library] was used to give linear line to separate dog and cat feature.

4. Testing

The project is separated into two different section, object detection and classification. Both sections tested separately before merged. This section describes how they were tested and the result of the project.







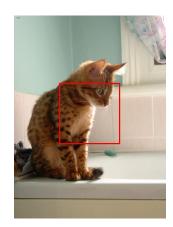
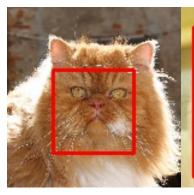


Figure 1. Body detection result (left: succeed, right: failed)



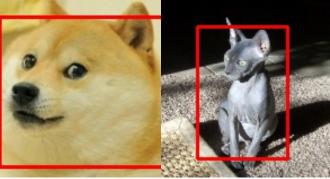




Figure 2. Face detection result (left: succeed, right: failed)

4.1. Object Detection

For both face and body detection, we trained the xml file with different number of stages, different distribution of face type, and different section of faces. With 4000 face images, cat detector performed best with 14 16 stages. Above 16 stages, the detector could not detect face

4.2. Classification

4.3. Kaggle Result

5. Discussion

5.1. Circuit description

The CMOS two-stage amplifier consists of two current mirrors, a differential amplifier and a cascade circuit. The circuit diagram is drawn in figure 1. For ease of calculation, the circuit is designed to have 1V V_{ov} for all MOSFETs. A value of $50k\Omega$ was chosen for reference resistor, R_ref and 0.1pF was chosen for compensation capacitor, C_c . Using Equation (1) , this design is calculated to generate an openloop gain, A_o , of 1254 which satisfies the requirements.

Using the circuit, simulated result clearly does not satisfies the design requirement. The output voltage, V_o , has a massive continuous pulse which does not satisfy the design requirement which addresses that both R_ref and C_c values have to be changed. This is depicted in figure 2.

In industry, normally 100Ω to $50M\Omega$ resistors and 0.1pF to $10\mu F$ capacitors are used for circuit design. Consider these values are design restriction, $15M\Omega$ resistor 25pF capacitor are chosen for R_ref and C_c . Since very high resistance value was chosen for reference resistor, it is obvious that current goes through second layer amplifier, cascade amplifier, would be low. In order to fix this issue, 2 PMOSs and 2 NMOSs are added for cascade amplifier to triple MOSFET width. Figure 3 presents the circuit diagram. A detail figure is provided in appendices

5.2. Open-Loop Analysis

To simplify calculations, the amplifier is designed to give identical V_{ov} for all MOSFETs. Equation (1) was used to calculate A_o .

$$A_o = \frac{2 * V_{an} * V_{ap}}{V_{ov} * (V_{an} + V_{ap})}^2 \tag{1}$$

The gain in decibel is simply calculated by:

$$A_{dB} = 20\log_{10}(A_o)$$

A Microsoft Excel spreadsheet was created for the calculation. The comparison between calculated values and SPICE simulated values are as follows:

	Calculation	Simulation
V_{d1}	-4.782 V	-4.782 V
V_{d2}	-2.068 V	-2.063 V
V_{d3}	5.282	5.286
i_1	773.21 <i>n</i> A	775.49 <i>n</i> A
i_2	$1.546 \mu A$	$1.551 \mu A$
i_4	776.70nA	775.49 <i>n</i> A
i_5	769.70nA	796.11 <i>n</i> A
i_6	776.70nA	796.11 <i>n</i> A
i_8	776.70nA	840.66nA
V_{ov}	68.3mV	69.15mV
A_{dB}	110.70 dB	112.54 dB

TABLE 1. CALCULATION & SIMULATION COMPARISON

The graph with gain in decibel and phase margin at 0dB is provided in figure 4.

The graph addresses that based on equation (4), the phase margin is positive which states the circuit is stable. The table above indicates that the predicted voltage values and current values made by the student are fairly close to SPICE simulation values. The calculated gain based on the equation (1) is 110.49 dB where the simulated gain is 112.54 dB.

The entire amplifier is running in 2*6.85V=13.7V. The current goes through voltage source, $V_{dd}\&V_{ss}$ is -4.8900 μ A. Therefore the power consumption of the amplifier is $13.7V*-4.8900\mu$ A =67.0 μ W

5.3. Closed-Loop Analysis

In order to start closed loop analysis, few equations must be discussed. Poles are critical components in order to stabilize the circuit. 4 poles are observed in this amplifier design where two poles are on the same spot. Open-loop simulation result is provided in figure 4, Closed-loop is provided in figure (5). Poles define bandwidth of the circuit. Required closed-loop bandwidth for the project is $\tau \geq 7.96kHz$. Where τ can be represented as follow equation (2) and the bandwidth is addressed on equation (3). Phase margin calculation is on equation (4).

$$\tau = \sum_{n=1}^{N} C_n R_n \tag{2}$$

$$\omega = \frac{1}{2\pi\tau} \tag{3}$$

$$PM = f_0 + 180^{\circ} \tag{4}$$

In both Closed-Loop and Open-Loop simulation, the phase margin is positive which addresses the circuit is stable. To predict where would each pole appears, following equations were used.

$$\omega_1 = \frac{1}{R_o * C_c} \tag{5}$$

$$\omega_2 = \frac{1}{R_{o2} * C_L} \tag{6}$$

$$\omega_3 = \frac{1}{2 * R_{o6,7} * C_{gs2}} \tag{7}$$

These equations were used to guide the estimation so we could predict around where the pole would exist with different values. However since the difference between prediction and simulation was fairly high, various simulations were made to adjust amplifier in order to satisfy the requirements. Based on figure (5), the bandwidth of the amplifier is 389.02kHz which satisfies the design requirements from table (1)

With the fully built Closed-Loop amplifier circuit, the simulation results to verify whether the design satisfies requirements are following on figure (6), (7).

Both figures address that the amplifier satisfies all requirements, peak overshoot, settling time and steady-state error. Based on the results, table 3 was made to conclude that the design successfully satisfy all the requirements.

	Requirements	Result
Settling time (s)	$< 100 \mu s$	$\approx 30 \mu s$
Input Step (V)	10mV	9.9999mV
Overshoot Voltage (V)	$\leq 10.5mV$	10.389mV
Steady-State Error (V)	$< 10 \mu V$	$8.19 \mu V$
Amplifier Gain	$A_o \ge 999,60dB$	112.5dB
Closed-loop Bandwidth	$\geq 7.96kHz$	389.02kHz

TABLE 2. REQUIREMENTS AND RESULT

6. Conclusion

References

 K. Smith, A. Smith, Microelectronic circuits(Oxford series in electrical and computer engineering (Hardco), 7th ed. New York, NY, United States: Oxford University Press, 2014.

7. Appendices

SPICE Netlist: