MCGILL UNIVERSITY

ECSE 415 PROJECT

Cat and Dog

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Team name: You thought it was an original team name,
but it was me, DIO!

submitting to
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1. Introduction

Most research for object classification was more focused on classifying images that are completely different (ex. horse and ship). In this project, we classify whether the image contains a picture of dog or cat. We were given 5906 images from [Cat and Dog paper]. We trained animal body detection and classification using 1500 images of cat and dog each. We used Haar features to detect the portion of the image containing the animal. Computation of the LBP histogram provides feature of the image for the classification. And then, we used SVM to define whether the image contains dogs or cats.

1.1. Amplifier requirements

The student id of the student is 260633759. The supply voltage level can be calculated based on the equation:

$$V_{ss} = 5 + \frac{4^{th} + 3^{rd} \textit{ digits from the end}}{20}$$

the minimum gain A_o is:

$$A_c = \frac{1}{1 + \frac{1}{A_o}}$$

Since settling time is 100 μs, and *settling time* $\approx 5\tau$ where the equation for bandwidth is:

$$\frac{1}{2\pi\tau}$$

From the project description and after all calculation were made, a table for requirements is follow:

DC Output Supply Voltage (V)	$\pm 6.85V$
Settling time (s)	$< 100\mu$s
Input Step (V)	$10mV$
Overshoot Voltage (V)	$\leq 10.5mV$
Steady-State Error (V)	$< 10\mu V$
Transistors	MOSFET CD4007
Load Capacitor	$5pF$
Amplifier Gain	$A_o \geq\ 999,60dB$
Closed-loop Bandwidth	$\geq 7.96kHz$

TABLE 1. AMPLIFIER REQUIREMENTS

2. Problem Representation

3. Discussion

3.1. Circuit description

The CMOS two-stage amplifier consists of two current mirrors, a differential amplifier and a cascade circuit. The circuit diagram is drawn in figure 1. For ease of calculation, the circuit is designed to have 1V V_{ov} for all MOSFETs. A value of $50k\Omega$ was chosen for reference resistor, R_ref and $0.1pF$ was chosen for compensation capacitor, C_c. Using Equation (1) , this design is calculated to generate an open-loop gain, A_o, of 1254 which satisfies the requirements. Using the circuit, simulated result clearly does not satisfies the design requirement. The output voltage, V_o, has a massive continuous pulse which does not satisfy the design requirement which addresses that both R_ref and C_c values have to be changed. This is depicted in figure 2.

In industry, normally 100Ω to $50M\Omega$ resistors and $0.1pF$ to $10\mu F$ capacitors are used for circuit design. Consider these values are design restriction, $15M\Omega$ resistor $25pF$ capacitor are chosen for R_ref and C_c. Since very high resistance value was chosen for reference resistor, it is obvious that current goes through second layer amplifier, cascade amplifier, would be low. In order to fix this issue, 2 PMOSs and 2 NMOSs are added for cascade amplifier to triple MOSFET width. Figure 3 presents the circuit diagram. A detail figure is provided in appendices

3.2. Open-Loop Analysis

To simplify calculations, the amplifier is designed to give identical V_{ov} for all MOSFETs. Equation (1) was used to calculate A_o.

$$A_o = \frac{2 * V_{an} * V_{ap}}{V_{ov} * (V_{an} + V_{ap})}^{\ 2} \tag{1}$$

The gain in decibel is simply calculated by:

$$A_{dB} = 20\log_{10}(A_o)$$

A Microsoft Excel spreadsheet was created for the calculation. The comparison between calculated values and

SPICE simulated values are as follows:

	Calculation	Simulation
V_{d1}	-4.782 V	-4.782 V
V_{d2}	-2.068 V	-2.063 V
V_{d3}	5.282	5.286
i_1	773.21nA	775.49nA
i_2	1.546μA	1.551μA
i_4	776.70nA	775.49nA
i_5	769.70nA	796.11nA
i_6	776.70nA	796.11nA
i_8	776.70nA	840.66nA
V_{ov}	68.3mV	69.15mV
A_{dB}	110.70 dB	112.54 dB

TABLE 2. CALCULATION & SIMULATION COMPARISON

The graph with gain in decibel and phase margin at 0dB is provided in figure 4.

The graph addresses that based on equation (4), the phase margin is positive which states the circuit is stable. The table above indicates that the predicted voltage values and current values made by the student are fairly close to SPICE simulation values. The calculated gain based on the equation (1) is 110.49 dB where the simulated gain is 112.54 dB.

The entire amplifier is running in $2 * 6.85V = 13.7V$. The current goes through voltage source, V_{dd}&V_{ss} is -4.8900μA. Therefore the power consumption of the amplifier is 13.7V *-4.8900μA =67.0μW

3.3. Closed-Loop Analysis

In order to start closed loop analysis, few equations must be discussed. Poles are critical components in order to stabilize the circuit. 4 poles are observed in this amplifier design where two poles are on the same spot. Open-loop simulation result is provided in figure 4, Closed-loop is provided in figure (5). Poles define bandwidth of the circuit. Required closed-loop bandwidth for the project is $\tau \geq 7.96kHz$. Where τ can be represented as follow equation (2) and the bandwidth is addressed on equation (3). Phase margin calculation is on equation (4).

$$\tau = \sum_{n=1}^{N} C_n R_n \tag{2}$$

$$\omega = \frac{1}{2\pi\tau} \tag{3}$$

$$PM = f_0 + 180^\circ \tag{4}$$

In both Closed-Loop and Open-Loop simulation, the phase margin is positive which addresses the circuit is stable. To predict where would each pole appears, following equations were used.

$$\omega_1 = \frac{1}{R_o * C_c} \tag{5}$$

$$\omega_2 = \frac{1}{R_{o2} * C_L} \tag{6}$$

$$\omega_3 = \frac{1}{2 * R_{o6,7} * C_{gs2}} \tag{7}$$

These equations were used to guide the estimation so we could predict around where the pole would exist with different values. However since the difference between prediction and simulation was fairly high, various simulations were made to adjust amplifier in order to satisfy the requirements. Based on figure (5), the bandwidth of the amplifier is $389.02kHz$ which satisfies the design requirements from table (1)

With the fully built Closed-Loop amplifier circuit, the simulation results to verify whether the design satisfies requirements are following on figure (6), (7).

Both figures address that the amplifier satisfies all requirements, peak overshoot, settling time and steady-state error. Based on the results, table 3 was made to conclude that the design successfully satisfy all the requirements.

	Requirements	Result
Settling time (s)	$< 100\mu$s	$\approx 30\mu$s
Input Step (V)	$10mV$	$9.9999mV$
Overshoot Voltage (V)	$\leq 10.5mV$	$10.389mV$
Steady-State Error (V)	$< 10\mu V$	$8.19\mu V$
Amplifier Gain	$A_o \geq 999,60dB$	$112.5dB$
Closed-loop Bandwidth	$\geq 7.96kHz$	$389.02kHz$

TABLE 3. REQUIREMENTS AND RESULT

4. Conclusion

References

[1] K . Smith, A . Smith, *Microelectronic circuits(Oxford series in electrical and computer engineering (Hardco)*, 7th ed. New York, NY, United States: Oxford University Press, 2014.

5. Appendices

SPICE Netlist: