

CEG 3155 Summary Sheet

Well this course is so unreasonable its ridiculous. Who knows what will get done. I have a lot of words I want to say to the administration of this course, but I will hold back. One thing is for certain, despite what they claim, uOttawa does not care about the health at all of their students. They expect students to dedicate their whole life to school, not sleep well, not eat well, and really sacrifice their whole health. Many people can deal with this, but some people cannot. This is not right for some people to feel like they are out of options and have to end everything because of the actions of the university.

Basically so far it is about asm design, and some fsm design. :-/

Also, this course has a lot of processes that in my opinion are quite hard to explain. They need to be done to understand them. So I don't think putting them here would really help me learn. But hey, I'll see.

- 1 Miscellaneous Topics**
- 2 VHDL**
- 3 ASM Design**
- 4 Arithmetic**
- 5 FSM Design**
- 6 Asynchronous Circuit Design**
- 7 Brief introduction to Verilog**
- 8 Brief introduction to SystemC**
- 9 Appendix**