Registers	
R0	S
R1	S
R2	S
R3	S
R4	P
R5	P
R6	P
R7	P
R8	P
R9 SB/TR	
R10	P
R11 FP	P
R12 IP	S
R13 SP	P
R14 LR	S
R15 PC	S
xPSR	S
CONTROL	

Op2 | Sft*
#const
Rm
ASR #n *
LSL #n *
LSR #n *
ROR #n
RRX

Adr
[Rn]
[Rn, Rm]
[Rn,#offs]
[Rn,#offs]!
[Rn],#offs

Arithmetic			
ADD[S]	Rd,Rn,Op2	Rd ← Rn + Op2	[N Z C V]
ADC[S]	Rd,Rn,Op2	Rd ← Rn + Op2 + C	[N Z C V]
SUB[S]	Rd,Rn,Op2	Rd ← Rn – Op2	[N Z C V]
SBC[S]	Rd,Rn,Op2	Rd ← Rn – Op2 – C	[N Z C V]
RSB[S]	Rd,Rn,Op2	Rd ← Op2 – Rn	[N Z C V]
MUL[S]	Rd,Rn,Op2	Rd ← Rn × Op2	[N Z]
MLA[S]	Rd,Rn,Rm,Ra	Rd ← Ra + Rn × Rm	[N Z]
MLS[S]	Rd,Rn,Rm,Ra	Rd ← Ra – Rn × Rm	[N Z]
{S,U}MULL	RdL,RdH,Rn,Rm	Rd ← Rn × Rm	
{S,U}MLAL	RdL,RdH,Rn,Rm	Rd ← Rd + Rn × Rm	
{S,U}MLSL	RdL,RdH,Rn,Rm	Rd ← Rd – Rn × Rm	
{S,U}DIV	Rd,Rn,Rm	Rd ← Rn ÷ Rm	
{S,U}XT{B,H}	Ra,Rb	Ra ← Extend(Rb)	
{S,U}SAT	Rd,#n,Rm,Sft	Rd ← Sat(Sft(Rm))	Q
CLZ[S]	Rd,Rn	Rd ← CountLeadingZeros(Rn)	

Shift, Rotate, Swap			
LSL[S]	Rd,Rm,Rs	Rd ← Rm << Rs	[N Z C]
LSR[S]	Rd,Rm,Rs	Rd ← Rm >> Rs	[N Z C]
ASR[S]	Rd,Rm,Rs	Rd ← SgnExt(Rm >> Rs)	[N Z C]
ROR[S]	Rd,Rm,Rs	Rotate right	[N Z C]
RRX[S]	Rd,Rm,Rs	Rd ← Rm >> 1	[N Z C]
REV	Ra,Rb	Ra $B_0B_1B_2B_3$ ← Rb $B_3B_2B_1B_0$	
REV16	Ra,Rb	Ra $B_2B_3B_0B_1$ ← Rb $B_3B_2B_1B_0$	
REVSH	Ra,Rb	Ra $B_1B_0B_3B_2$ ← Rb $B_3B_2B_1B_0$	

Bitfields		
BFC	Rd,#b,#w	Rd ← Rd & ~((2^w–1) << b)
BFI	Rd,Rn,#b,#w	Rd ← (Rd & ~((2^w–1) << b)) | (Rn << b)
{S,U}BFX	Rd,Rn,#b,#w	Rd ← (Rn >> b) & (2^w–1)

Condition Codes						*S* U
EQ	NE	*MI*	*PL*			AL
GE	*LT*	*LE*	*GT*	*VS*	*VC*	
HS	LO	LS	HI	CS	CC	

Miscellaneous	
IT[T,E][T,E][T,E]	cond
WFI	Wait for interrupt
NOP	No operation

Bitwise			
MVN[S]	Ra,Rb	Ra ← ~Rb	[N Z C]
AND[S]	Rd,Rn,Op2	Rd ← Rn & Op2	[N Z C]
ORR[S]	Rd,Rn,Op2	Rd ← Rn | Op2	[N Z C]
EOR[S]	Rd,Rn,Op2	Rd ← Rn ^ Op2	[N Z C]
BIC[S]	Rd,Rn,Op2	Rd ← Rn & ~Op2	[N Z C]

Compare & Test			
CMP	Rn,Op2	Rn – Op2	N Z C V
CMN	Rn,Op2	Rn + Op2	N Z C V
TST	Rn,Op2	Rn & Op2	N Z C
TEQ	Rn,Op2	Rn ^ Op2	N Z C

Branch			
B	label	PC ← label	
BX	Rm	PC ← Rm	
BL	label	LR ← PC + 4 ; PC label	
BLX	Rm	LR ← PC + 4 ; PC ← Rm	
TBB	Rn,Rm	PC ← PC+4 + [Rn+Rm]	
TBH	Rn,Rm,LSL #1	PC ← PC+4 + [Rn+2*Rm]	
CBZ	Rn,label	Rn == 0: PC ← label	
CBNZ	Rn,label	Rn != 0: PC ← label	

Data Transfer			
ADR	Rd,label	Rd ← label	
MOV[S]	Rd,Op2	Rd ← Op2	[N Z C]
MOV[S]	Rd,#imm16	Rd ← imm16	[N Z C]
MOVT	Rd,#imm16	Rd ← Rd | imm16 << 16	
{LD,ST}R[H,B,SH,SB]			Rt,Adr
{LD,ST}RD			Rt,Rt2,Adr
LDM[IA|FD,IB|ED,DA|FA,DB|EA]			Rn[!],{Regs}
STM[DB|FD,DA|EA,IB|FA,IA|EA]			Rn[!],{Regs}
{PUSH,POP} {Regs} ⇔ {ST,LD}MFD SP!,{Regs}			
MRS	Rd,SpecR	Rd ← SpecR	
MSR	SpecR,Rm	SpecR ← Rm	N Z C V