ELG 2136 Course Summary

1 Physics

Electric Conduction can happen due to 2 different mechanisms.

1. Forced **Drift** (When an Electric Field is applied)
2. Natural **Diffusion** (Free charges tend to move to less densely charged areas)

We define J as the **current density** which is just $\frac{\text{total current}}{\text{area}}$. J can be calculated for Drift, or Diffusion but we need a few more things defined.

We define n_i as the density of electrons/holes, which depends on the boltzmann constant k, the temperature T, and the material specific bandgap energy E_g.

$$n_i = 5.2 \times 10^{15} T^{\frac{3}{2}} e^{\frac{-E_g}{2kT}}$$

We define q as the charge of a single electron/hole, μ_n, μ_p as the mobility constants of the electrons (n) and holes (p), D_n, D_p as the diffusion constants, n and p are the electron and hole concentrations, and E is the electric field applied.

$$J_{drift} = q(\mu_n n + \mu_p p)E \qquad J_{diffusion} = qD_n \frac{dn}{dx} - qD_p \frac{dp}{dx}$$

1.1 Doping

While pure silicon is neutral, we can dope the silicon with boron (extra proton) or phosphorus (extra electron).

We define n_n, p_p as the number of free electrons and protons in a material at thermal equilibrium.

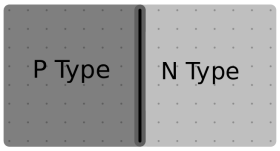
If the material has majority positive (p-type), we say: $n_p, p_p, p_p \cdot n_p = n_i^2$

If the material has majority negative (n-type), we say: $n_n, p_n, p_n \cdot n_n = n_i^2$

We can put a p-type and n-type material adjacent (PN Junction), and that creates a **diode**.

1.2 At a PN Junction

This is a junction of two materials, specifically a positive (P) and negative (N) material.



We have constants of L_p and L_n for the spacial exponential decay of the P or N charges.

Then the numbers N_A and N_D are porportional to the number of positive and negative charges respectively. They are the number of *acceptor* or *donor* atoms.

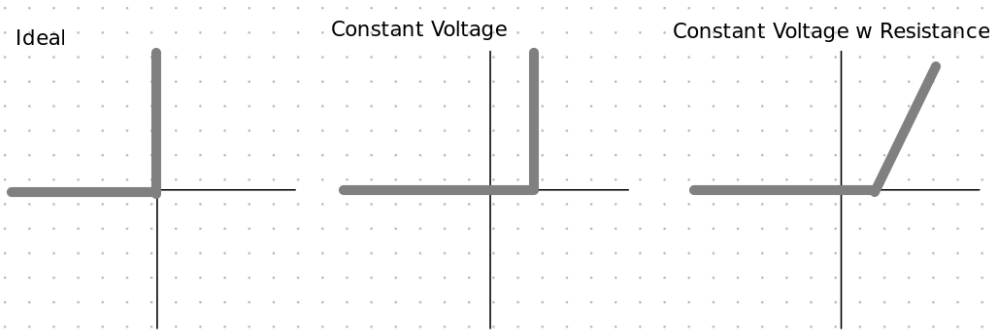
If A is the area, then we say that the total diffusion current density is:

$$J_{diff\_tot} = Aqn_i^2 \left(\frac{D_p}{L_p N_D} + \frac{D_n}{L_n N_A} \right) \left(e^{\frac{v}{V_t}} - 1 \right)$$

This is also the total current since the drift current in a PN junction is small due to the generated electric field.

2 Circuit Analysis with Diodes

We have three models for diodes. There is the ideal, constant voltage (ideal with voltage source), and constant voltage with resistance (ideal with voltage source and resistance). All of these model the real diode.



An ideal diode can be either in the ON state (where current passes through in the correct direction) or the OFF state (where it acts as an open circuit). The other models just have this ideal diode with the voltage and resistance in series.

To determine the state of the diode, we need to assume a state (OFF or ON) and then check if it makes sense.

- If it is ON, then current MUST go from anode to cathode.
- If it is OFF, then voltage at cathode must be HIGHER than voltage at anode.

If either of these criteria are wrong, then our assumption is on, and we need to try another one.

NOTE: There can only be **one** combination that works with a circuit. So if we have 2 diodes, and the first try it works, then it MUST be ONLY that combination.

Ex.

2.1 Plotting

For these problems, we have a circuit, and we have an input voltage (x axis) and another value such as output voltage, or output current, and we need to **plot the output as a function of the inputs**.

This is a lot of work since we have diodes, and when each diode changes, as will the relation between the input and the output.

This is the procedure:

1. Replace all diodes with their model (Ideal, Constant Voltage, CV with Resistance)
2. Assume very low value for X (input) and find the state of each diode using this low value.
3. Analyse the circuit to find Y (output) as a function of X (input)
4. Find out which diode will switch its state **first** (let ON diode current=0, or OFF diode voltage=0)
5. Replace the diode whose state changes first with its new state and *return to step 3*.
6. STOP analysis once no more diodes will change state (diodes only change states at most 1 time).

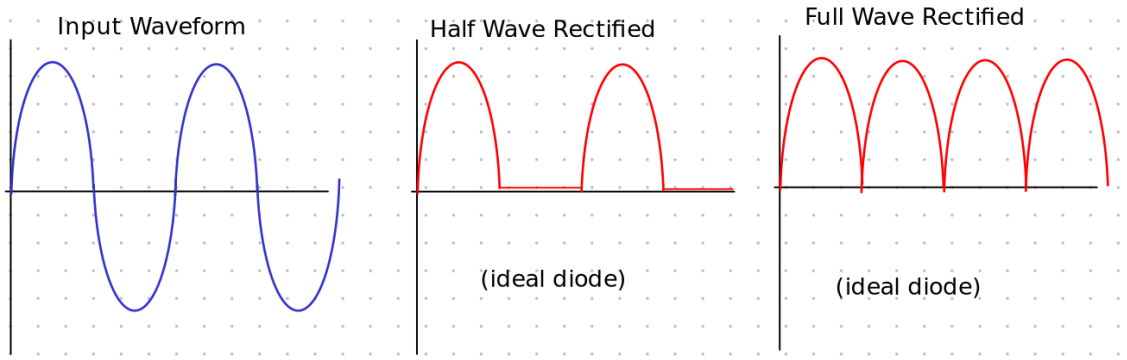
Ex.

3 DC Power Supply

This is a very important application of diodes. This will convert an AC time dependant source to a DC constant source.

3.1 Rectifier

The rectifyer will take an AC source, and make the output be positive.



A Half wave rectifier (1 diode) will just kill the negative part of the wave, while a Full wave rectifier (2 diodes) will keep the positive part, and invert the negative part.

A Bridge rectifyer is a special type of full wave rectifier that has 4 diodes instead of 2.

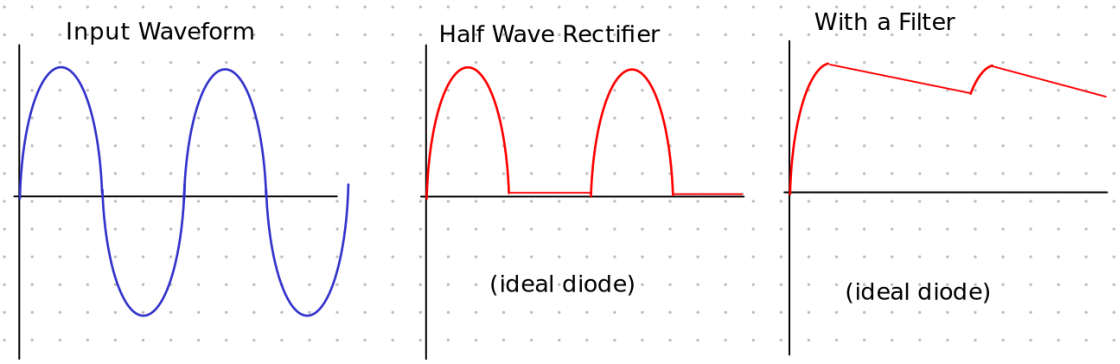
A useful statistic is the PIV (Peak Inverse Voltage) across a diode. To find this, we take a diode that we want to find the PIV across, then we find what would be the maximum negative voltage across this diode (note the diode will be OFF) when the source is at its inverse peak.

Typically we di a KVL through the circuit. Note that we find the voltage across the whole diode (including voltage and resistance if using that model).

Ex.

3.2 Filter

The Filter is just adding a capacitor in parallel with the load resistor. This will **smooth out the big inflections**, but there will still be a ripple.



We call V_p the peak voltage of the wave, V_r as the ripple voltage (if it fluctuates between 9 and 11 V, then $V_4 = 2V$), and V_k as the minimum voltage.

$$V_p = V_k + V_r$$

We can make some approxmiations (with ideal diodes) to see that:

$$V_r = \frac{V_p}{fRC} \text{ for a half wave rectifier or}$$

$$V_r = \frac{V_p}{2fRC} \text{ for a full wave}$$

$$\omega\Delta t = \sqrt{\frac{2V_r}{V_p}} \text{ for both types of rectifiers}$$

$$\text{Current through diode average } i_{Davg} = I_L(1 + \pi\sqrt{\frac{2V_p}{V_r}}) \text{ for half wave}$$

$$\text{or for full wave } i_{Davg} = I_L(1 + \pi\sqrt{\frac{V_p}{2V_r}})$$

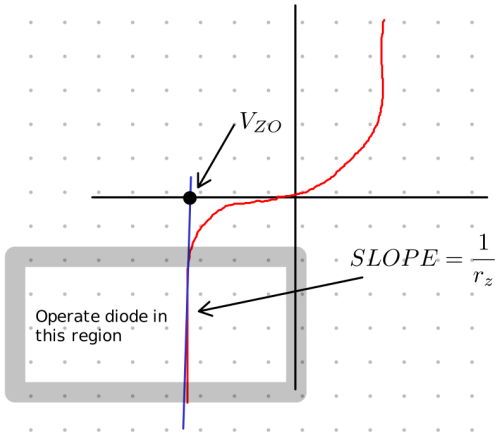
$$\text{Current through diode MAX } i_{Dmax} = I_L(1 + 2\pi\sqrt{\frac{2V_p}{V_r}}) \text{ for half wave}$$

$$\text{or for full wave } i_{Dmax} = I_L(1 + 2\pi\sqrt{\frac{V_p}{2V_r}})$$

If we are working with a different model, such as the constant voltage model, then we will need to modify the equations such as increasing the peak voltage by 0.7V. The one exception is the conduction angle formula $\omega\Delta t$ since that is not affected by te extra 0.7V.

3.3 Regulator

The regulator is a function that takes in a voltage source with unwanted ripples, and greatly **reduces these ripples**. It does this with a diode working in the breakdown region (zener diode).



r_z is the internal resistance of the diode. V_{ZO} is the internal voltage source of the diode.

We need to ensure that the zener operates **only in the breakdown region** for no fluctuations in the output voltage. We do this by finding the minimum and maximum current allowed for the diode to stay in the breakdown region (straight line part).

We want to maintain the output voltage to be as constant as possible, and this is measured using the line and load regulation.

$$\text{Line Regulation} = \frac{\Delta V_O}{\Delta V_s} = \frac{r_z}{r_z + R} \qquad \text{Load Regulation} = \frac{\Delta V_O}{\Delta I_L} = -\frac{r_z \times R}{r_z + R} = -r_z//R$$

Ex.

4 Bipolar Junction Transistor (BJT)

A BJT transistor has 2 PN junctions.

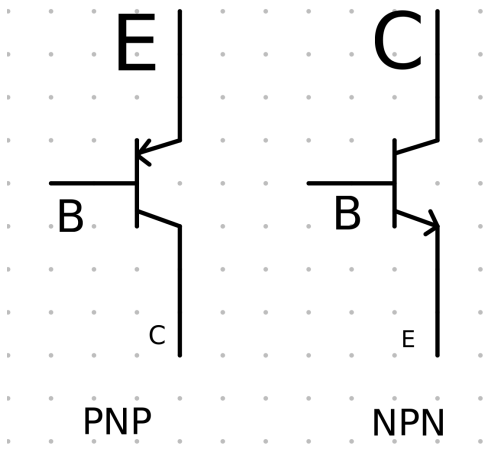
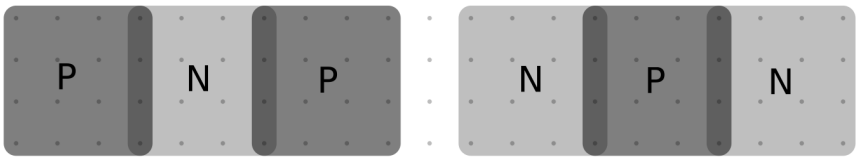


Figure 1: Active Mode Bias

The BJT can either have P type sandwiched between 2 N types (NPN), or N type sandwiched between 2 P types (PNP).



A BJT has three terminals called the **Emitter, Collector, and Base**. Each of these terminals needs to have a DC voltage applied. Depending on how these voltages relate to each other (biassing of each PN junction) makes the transistor operate differently.

In this course we only care about the **active** mode which is where for PNP, the emitter is the largest, followed by base, followed by collector, and for NPN, collector is largest, followed by base, followed by emitter.

In all cases, the BE junction has a difference of 0.7 volts due to the diode.

Going back to the PNP or NPN model, if the current flows from P to N, we say that junction is in forward bias. While if the current flows from N to P, we say that junction is in reverse bias.

Mode	E-B Junction	C-B Junction
Cutoff	Reverse	Reverse
Active	Forward	Reverse
Reverse Active	Reverse	Forward
Saturation	Forward	Forward

4.1 DC Analysis

To do the DC analysis, we need to figure out what mode the transistor is in. Typically for this course it is either in Cutoff mode (no current), or active mode (see Figure 1).

So we **assume active mode**, and see if there is a contradiction (such as negative or 0 current).

We have some very useful relations for the currents which are:

$$I_E = I_B + I_C \qquad\qquad I_C = \beta I_B$$

β is a parameter of the specific BJT given in the **datasheet**.

4.2 AC Analysis

We need to introduce a new notation for this. We say that lowercase means ac, and uppercase means DC. Mixed case means a mixed signal.

v_A	ac and DC Signal
v_a	Pure ac Signal
V_A	Pure DC signal

To get the current, *sometimes* we are given the I_S parameter. This gives:

$$i_C = I_S e^{\frac{v_{BE}}{V_T}} \text{ for NPN or replace } V_{BE} \text{ with } V_{EB} \text{ for PNP}$$

Here V_T is a known value that is given on the **datasheet**.

With ac analysis, we generally do not know the ac currents or voltages since these fluxuate with time. But we do know the resistances and the DC currents. Through this information we can get the following parameters:

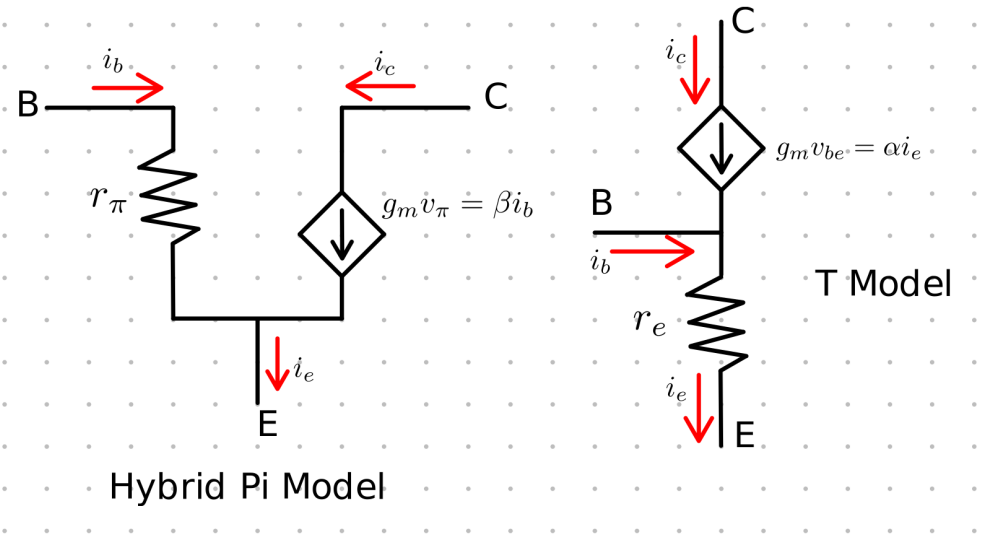
$$g_m = \frac{I_C}{V_T} \qquad r_\pi = \frac{\beta}{g_m} = \frac{V_T}{I_B} \qquad r_e = \frac{\alpha}{g_m} \qquad \alpha = \frac{\beta}{\beta + 1}$$

Then we also have other parameters that we need to find through circuit analysis such as KVL or KCL. These are things such as:

$A_V = \frac{v_{out}}{v_{in}}$	Voltage Gain
$G_v = \frac{v_{out}}{v_{sig}}$	Overall Voltage Gain
$A_i = \frac{i_{out}}{i_{in}}$	Current Gain
R_{in}	Input Resistance
R_{out}	Output Resistance

When doing these, the answer **MUST NOT be in terms of time dependant values** such as ac current, or ac voltage.

To do this, we need to change the BJT transistor for a **model**. We have the Hybrid Pi model, or the T model.



4.3 ac and DC Analysis Combined

When combining the two analyses, we can consider each one individually and follow the following technique:

- DC Analysis

  Short Circuit all ac voltage sources and Open Circuit all ac current sources

  Short circuit all inductors, and open circuit all capacitors

  Find C, B, E currents and voltages, find g_m, and confirm it is in active mode.

- ac Analysis

  Short Circuit all DC voltage sources and Open Circuit all DC current sources

  Short circuit all capacitors, and open circuit all inductors

  Solve for what we want (such as A_V or R_{in})

Ex.

4.4 Early Effect

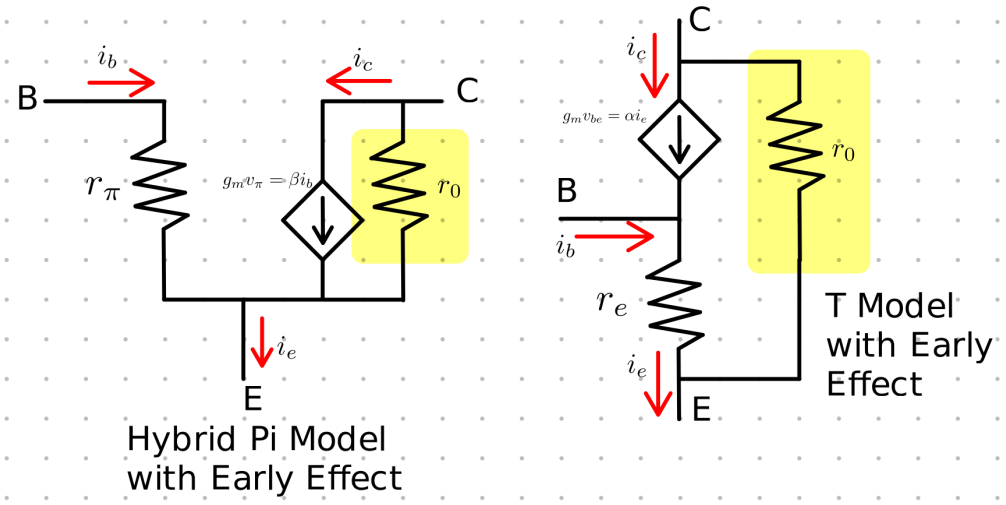
In the real world the current has a dependance on the voltage. This is called the Early effect. To model this, we can add a **resistor** with resistance r_0 between the collector and base.

When dealing with the early effect, we are given a voltage valus V_A which is specific to the BJT we are working with. This allows us to calculate r_0.

$$r_0 = \frac{V_A}{I_C}$$

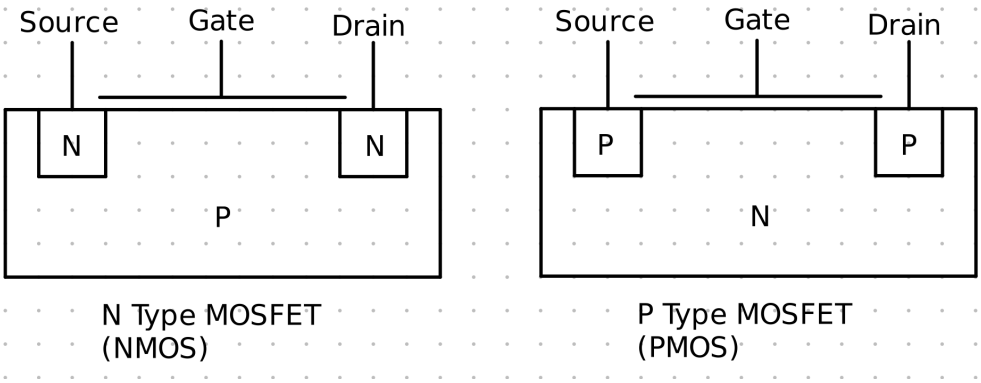
Then we can just proceed with the analysis steps as normal. The analysis does get more complex, but it is the same general process.

We just need to change the models to:

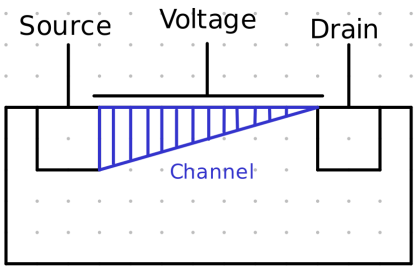


5 Metal Oxide Semiconductor Field Effect Transistor (MOSFET)

A MOSFET has 3 connections. The **Source, Gate, and Drain**. There is **no current in the gate** since it does not directly touch the materials (therefore **source current and drain current are same**). It is just used to generate an electric field to move the charges.



When we apply a voltage at the gate, a channel is created where the electrons will flow from the Source to the Drain (for NMOS or Drain to Source for PMOS).



MOSFETs have three modes they can be in:

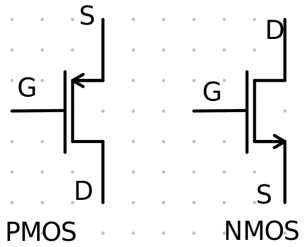
- Cutoff (No current)
- Saturation (Constant current)
- Triode (Changing current)

We have some parameters for the MOSFET. These are unique to each MOSFET and given on the datasheet.

$$\mu C_{ox}\frac{W}{L} \qquad\qquad V_t$$

For NMOS, $V_t > 0$, and for PMOS, $V_t < 0$.

The symbols are:



5.1 DC Analysis

To do the DC analysis, we use the following process:

1. Test for cutoff mode (No current)
2. **If not cutoff**, Assume Saturation or Triode mode
3. Use the transistor current equation to get I_D AKA I_S
4. Do more circuit analysis if required
5. Verify the two conditions for the assumed mode (from step 2)
6. **If conditions are not met**, then return to step 2 and assume the other mode.

The conditions and transistor current equation are different for NMOS or PMOS. They depend on V_t which is also referred to as V_TH.

NMOS ($V_{TH} > 0$)

$V_{GS} < V_{TH}$	$I_D = I_S = 0$	Cutoff Conditions and Current
$V_{GS} > V_{TH}$	$V_{DS} < V_{GS} - V_{TH}$	Triode Conditions
$I_D = I_S = \mu_n C_{ox} \frac{W}{L} \left((V_{GS} - V_{TH}) V_{DS} - \frac{1}{2} V_{DS}^2 \right)$		Triode Current
$V_{GS} > V_{TH}$	$V_{DS} \geq V_{GS} - V_{TH}$	Saturation Conditions
$I_D = I_S = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 (1 + \lambda V_{DS})$		Saturation Current

PMOS ($V_{TH} < 0$)

$V_{GS} > V_{TH}$	$I_D = I_S = 0$	Cutoff Conditions and Current
$V_{GS} < V_{TH}$	$V_{DS} \geq V_{GS} - V_{TH}$	Triode Conditions
$I_D = I_S = \mu_p C_{ox} \frac{W}{L} \left((V_{SG} - \lvert V_{TH} \rvert) \lvert V_{DS} \rvert - \frac{1}{2} V_{DS}^2 \right)$		Triode Current
$V_{GS} < V_{TH}$	$V_{DS} < V_{GS} - V_{TH}$	Saturation Conditions
$I_D = I_S = \frac{1}{2} \mu_p C_{ox} \frac{W}{L} (V_{SG} - \lvert V_{TH} \rvert)^2 (1 + \lambda \lvert V_{DS} \rvert)$		Saturation Current

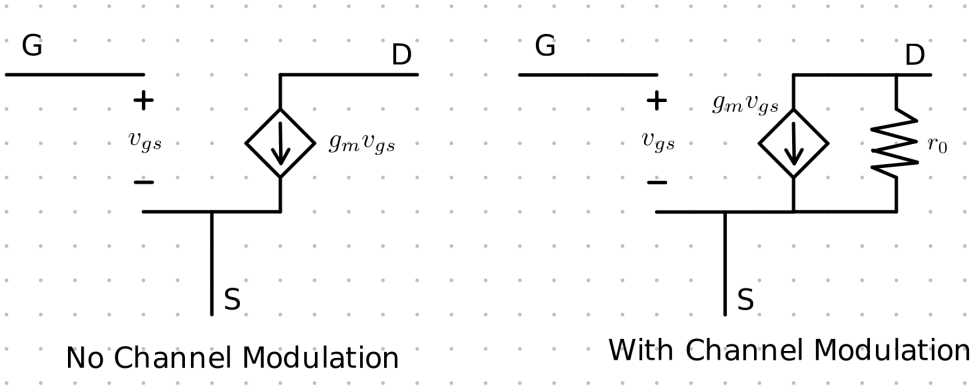
5.2 AC Analysis

When we are doing the ac analysis just like the BJT we cannot have any answers with a time dependant current or voltage.

We often want to find the same parameters such as the voltage gain, or current gain.

We follow a similar procedure to the BJT where we first do DC analysis to find the operating mode, then we go into ac mode and sub in the ac model. Then we can find what we want to find.

The ac model is:



Ex.

5.3 Channel Modulation

This is the same idea of early effect for BJT but for MOSFET.

As the channel width increases, its resistance changes. So we need to account for this.

We have the parameter $\frac{1}{V_A} = \lambda$.

This only affects the saturation mode equation hence the term $1 + \lambda V_{DS}$ at the end of those current equations.

We add a resistor r_0 with value of:

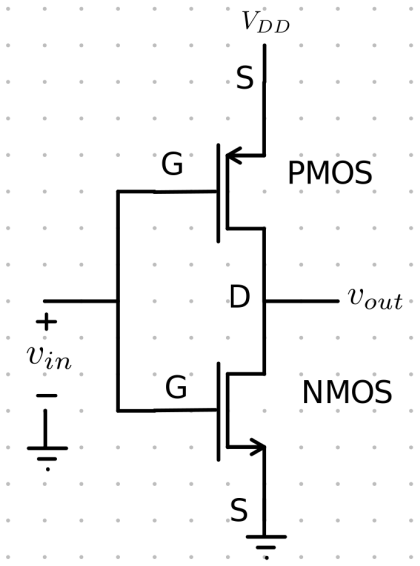
$$r_0 = \frac{1}{I_D \lambda}$$

6 Complementary MOSFET (CMOS) Inverter

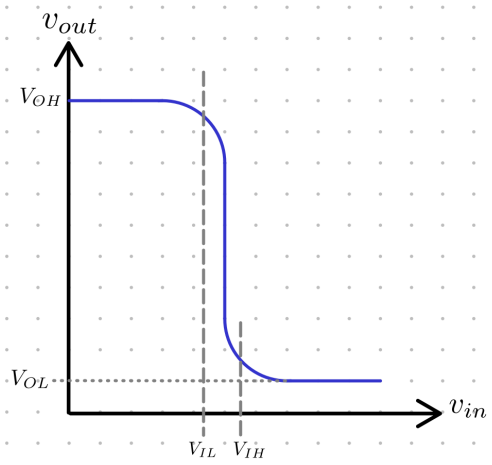
A CMOS is a circuit with 2 MOSFETS, one of which is a PMOS, one is an NMOS.

The Inverter is a circuit that will take a low voltage and turn it into a high voltage, and take a high voltage and turn it into a low voltage.

It is the `NOT` gate.

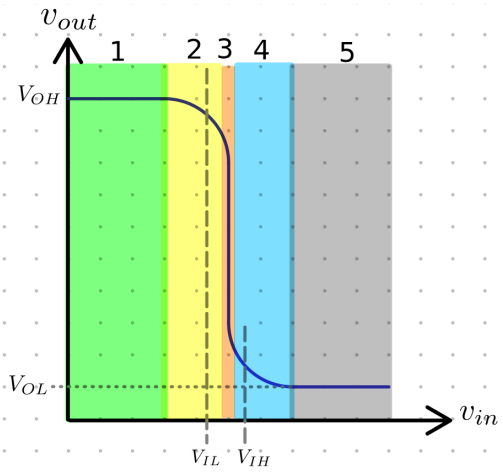


6.1 Voltage Transfer Characteristic (VTC) of CMOS



Through the VTC, we can see that there are 5 main areas.

- First area when $V_{out} = V_{OH}$ when the output is constant HIGH
- Second area where V_{out} decreases, but is still HIGH
- Third area where V_{out} is in the middle, neither HIGH or LOW (Between V_{IL} and V_{IH})
- Fourth area where V_{out} is decreasing, but reached te LOW section
- Fifth area where V_{out} is constant LOW



We can figure out through using the circuit diagram, and the MOSFET equations the states of the MOSFETs in all 5 regions:

Most of the values are fairly straightforward to calculate, such as the main input voltage in region 3 is just half of the max input voltage V_{DD}. The low end of the HIGH part V_{IL} and

Region	NMOS	PMOS
1	Cutoff	Triode
2	Saturation	Triode
3	Saturation	Borderline of Triode/Saturation
4	Triode	Saturation
5	Triode	Cutoff

the high end of the LOW part V_{IH} are:

$$V_{IH} = \frac{1}{8}(5V_{DD} - 2V_t) \qquad V_{IL} = \frac{1}{8}(3V_{DD} + 2V_t)$$

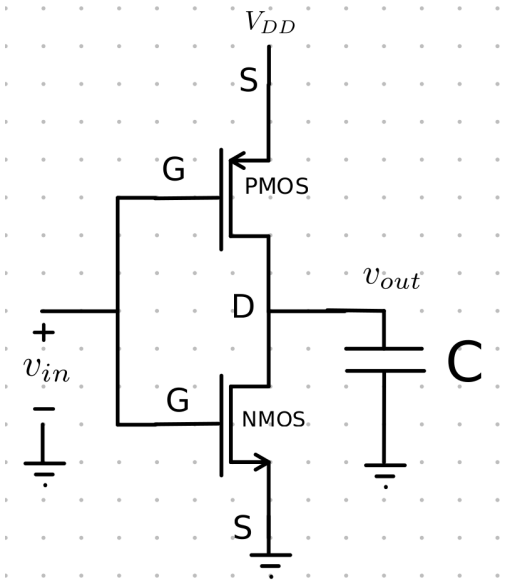
Ex.

6.2 Delay in the CMOS Inverter

In real life, the inverter does not change from HIGH to LOW, or from LOW to HIGH instantaneously. There is some delay.

We define the time it takes for the inverter to go from LOW to halfway to HIGH as t_{PLH} and from HIGH to halfway to LOW as t_{PHL}.

We can see this quite obviously if we have a capacitor connected to the output voltage of the CMOS inverter. By definition, the voltage of the capacitor cannot change instantaneously. So there must be some delay.



We have the following equations to calculate the times given a capacitence C:

$$t_{PHL} = \frac{a_n C}{\mu_n C_{ox} \left(\frac{W}{L}\right)_n V_{DD}} \qquad \alpha_n = \frac{2}{\frac{7}{4} - \frac{3V_{tn}}{V_{DD}} + \left(\frac{V_{tn}}{V_{DD}}\right)^2}$$

$$t_{PHL} = \frac{a_p C}{\mu_p C_{ox} \left(\frac{W}{L}\right)_p V_{DD}} \qquad \alpha_p = \frac{2}{\frac{7}{4} - \frac{3|V_{tp}|}{V_{DD}} + \left(\frac{V_{tp}}{V_{DD}}\right)^2}$$

7 Appendix

7.1 Short Formula Sheet

This is just a summary of all the important formulas:

Semiconductor Physics:

$$n_i = 5.2 \times 10^{15} T^{\frac{3}{2}} e^{\frac{-E_g}{2kT}}$$

$$J_{drift} = q(\mu_n n + \mu_p p)E \qquad J_{diffusion} = qD_n \frac{dn}{dx} - qD_p \frac{dp}{dx}$$

$$p_p \propto N_A \qquad n_n \propto N_D$$

$$p_p n_p = n_n p_n = n_i^2$$

$$J_{diff\_tot} = Aqn_i^2 \left(\frac{D_p}{L_p N_D} + \frac{D_n}{L_n N_A} \right) \left(e^{\frac{v}{V_t}} - 1 \right) \text{ For PN Junction}$$

Rectifyer with Filter: Half wave rectifyer with single ideal diode

$$V_r = \frac{V_p}{fRC} \qquad \omega \Delta t = \sqrt{\frac{2V_r}{V_p}}$$

$$i_{Davg} = I_L(1 + \pi\sqrt{\frac{2V_p}{V_r}}) \qquad i_{Dmax} = I_L(1 + 2\pi\sqrt{\frac{2V_p}{V_r}})$$

Zener Diode

$$\text{Line Regulation} = \frac{\Delta V_O}{\Delta V_s} = \frac{r_z}{r_z + R} \qquad \text{Load Regulation} = \frac{\Delta V_O}{\Delta I_L} = -\frac{r_z \times R}{r_z + R} = -r_z//R$$

BJT

$$g_m = \frac{I_C}{V_T} \qquad r_\pi = \frac{\beta}{g_m} \qquad r_0 = \frac{V_A}{I_C} \qquad r_e = \frac{\alpha}{g_m} \qquad \alpha = \frac{\beta}{\beta + 1}$$

NMOS ($V_{TH} > 0$)

$V_{GS} < V_{TH}$	$I_D = I_S = 0$	Cutoff
$V_{GS} > V_{TH}$	$V_{DS} < V_{GS} - V_{TH}$	Triode
$I_D = I_S = \mu_n C_{ox} \frac{W}{L} \left((V_{GS} - V_{TH}) V_{DS} - \frac{1}{2} V_{DS}^2 \right)$		Triode
$V_{GS} > V_{TH}$	$V_{DS} \geq V_{GS} - V_{TH}$	Saturation
$I_D = I_S = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 (1 + \lambda V_{DS})$		Saturation

PMOS ($V_{TH} < 0$)

$V_{GS} > V_{TH}$	$I_D = I_S = 0$	Cutoff

$$V_{GS} < V_{TH} \qquad V_{DS} \geq V_{GS} - V_{TH} \qquad \text{Triode}$$

$$I_D = I_S = \mu_p C_{ox} \frac{W}{L} \left((V_{SG} - |V_{TH}|)|V_{DS}| - \frac{1}{2} V_{DS}^2 \right) \qquad \text{Triode}$$

$$V_{GS} < V_{TH} \qquad V_{DS} < V_{GS} - V_{TH} \qquad \text{Saturation}$$

$$I_D = I_S = \frac{1}{2} \mu_p C_{ox} \frac{W}{L} (V_{SG} - |V_{TH}|)^2 (1 + \lambda |V_{DS}|) \qquad \text{Saturation}$$

Small Signal Parameters for NMOS or PMOS

$$g_m = \sqrt{2 \mu C_{ox} \frac{W}{L} I_D} = \mu C_{ox} \frac{W}{L} (V_{GS} - V_T H) \qquad r_0 = \frac{1}{\lambda I_D}$$

CMOS Inverter

$$V_{IH} = \frac{1}{8}(5V_{DD} - 2V_t) \qquad V_{IL} = \frac{1}{8}(3V_{DD} + 2V_t)$$

$$t_{PHL} = \frac{a_n C}{\mu_n Cox \frac{W}{L}_n V_{DD}} \qquad \alpha_n = \frac{2}{\frac{7}{4} - \frac{3V_{tn}}{V_{DD}} + \left(\frac{V_{tn}}{V_{DD}} \right)^2}$$

$$t_{PHL} = \frac{a_p C}{\mu_p Cox \frac{W}{L}_p V_{DD}} \qquad \alpha_p = \frac{2}{\frac{7}{4} - \frac{3|V_{tp}|}{V_{DD}} + \left(\frac{V_{tp}}{V_{DD}} \right)^2}$$