Software Defined Radio:

A brief presentation to outline the definition, requirements, plan of action, and reporting of our proposed senior project.

By:

- Tadd Bliss, Project Engineer
- Mishaal Fallatah, Development Engineer
- Shaun McKnight, System Engineer
- Justin Owen, Design Engineer

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1.0 Project Definition:

1.1 Functions:

This project aims to build a direct conversion receiver using the Hartley demodulator and an FPGA. When all is finished we should have a receiver capable of:

- 0-50MHz Bandwidth
- AM Reception Upper and Lower Sidebands
- Continuous Wave Reception
- Fourier Transform on a Display
- Audio on Speakers

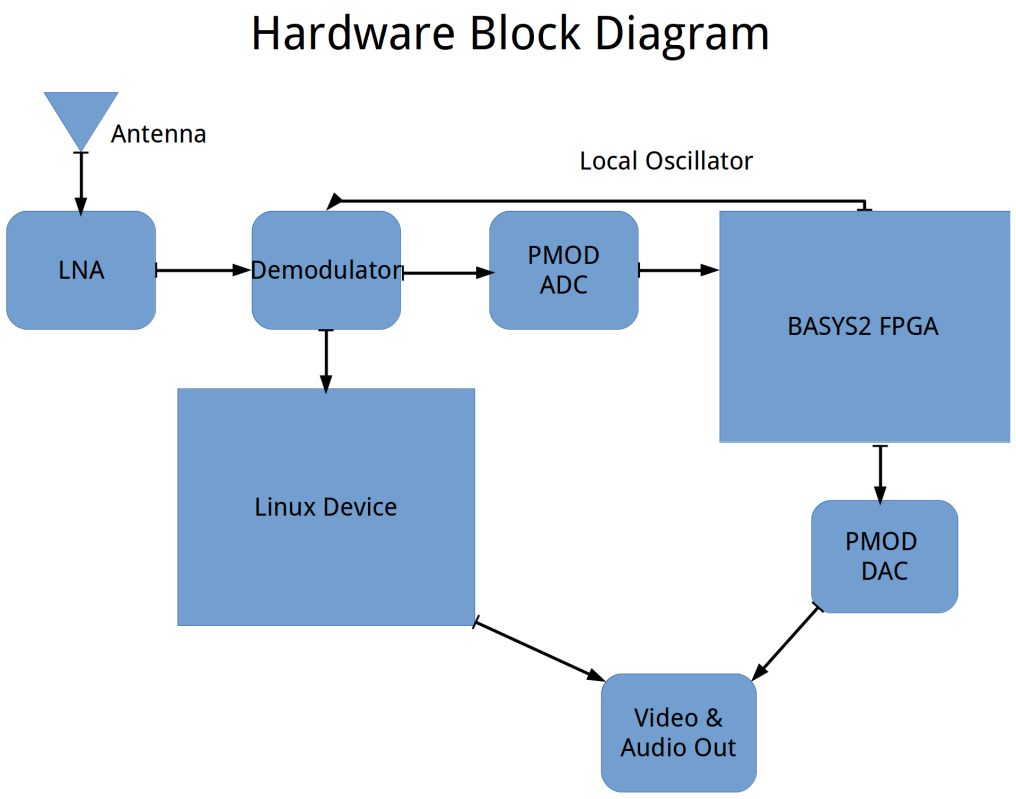


Figure 1: Preliminary Block Diagram

1.2 Customer:

Dr. Antone Kusmanoff
Oklahoma State University
Senior Design Instructor
Contact Information:

- Email: antone.kusmanoff@okstate.edu
- Phone: (405) 744-5716

1.3 Team Identity:

Team Name:

- Precision Engineering

Project Name:

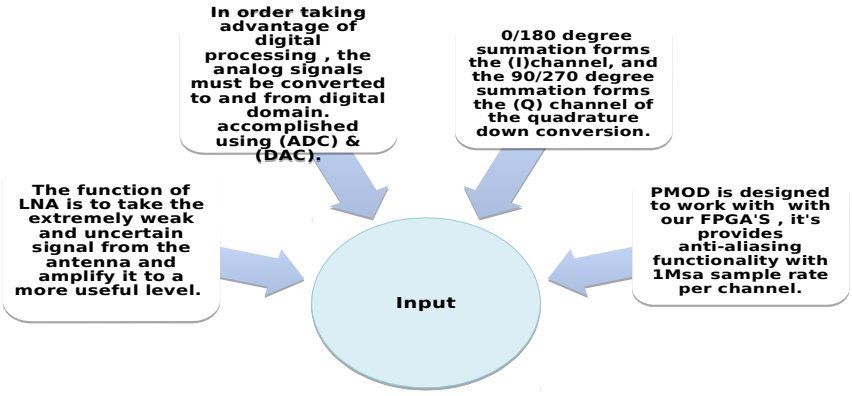
- Software Defined Radio

Team Engineers:

- Tadd Bliss, Project Engineer
- Mishaal Fallatah, Development Engineer
- Shaun McKnight, System Engineer
- Justin Owen, Design Engineer

2.0 Project Requirements:

2.1 Requirements:



2.2 SWAP:

- Even medium performance SDR tends to require more power for a given function than equipment designed specifically for purpose with optimum analogue/digital architectural partitioning.
- Ultra Low Power equipment's not requiring large frequency ranges or modulation types are currently still better implemented in conventional architectures
- Total power should be < 5 W.
- We going to use the DC power supply (HY3003-3) in the lab.
- The weight of the system will be approximately 50g for the LNA and 300g for the FPGA and Demodulation system.

2.3 COTS Products:

- Raspberry pi
- PMOD ADC
- BASYS 2 (FPGA)
- PMOD DAC
- Monitor
- Speaker
- COAX cables (RF)
- AV cables

2.4 System Limitations:

- There are technology limits on achievable RF performances.
- The choice of architecture depends on the available technology e.g. ADC performance, semiconductor technology.
- Software reliability may define overall radio reliability, rather than hardware limitations.

2.5 Assumptions:

- Learn the fundamental definitions, architectures, and the tradeoffs involved in dynamic characteristics such as data rate, channel bandwidth, and demodulation schemes

- The system must operate across several orders of frequencies; the antenna must be tuned by some means to track the operation frequency to maintain operating efficiency.

- Since our device is going to be very prone to oscillations we are going to target quality Low dropout Linear Regulators for the project.

- AM is the main focus. We hope to have single side band working as well.

- Radio Frequency 0 – 50 MHz

3.0 Plan of Action:

3.1 Tasks:

Tadd Bliss, Project Engineer	Mishaal Fallatah, Development Engineer

• Project Identities
• Quad Chart
• Planning
  ➢ Integrated Master Plan (IMP)
  ➢ Statement Of Work (SOW)
  ➢ Work Breakdown Structure (WBS)
  ➢ Task Assignments
  ➢ Cost Estimating and Budget
  ➢ Project Risk Assessment
  ➢ Acquisition Process
• Project Schedule
  ➢ Integrated Master Plan (IMP)
  ➢ Milestones
	-Primary-
	• Hardware Requirements (Voltages, Calculations, etc.)
	• Hardware Low Level Architecture
	• Preliminary and Detailed Design
	• Component Selection and Procurement
	• Hardware Fabrication
	• Hardware Unit and Component Testing with Results Documented
	-Supplemental-
	• Proposal Report Document
	  • Project Requirements

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Project Logging and Reporting
Project Risk Management

Communications

Customer

Milestone Matrix
Program Deviation Report
Weekly Email

Team

Video Chat (Google Hangouts)
Weekly Meetings
Email
SharePoint

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System Modifications
Testing and Recording
System Efficiency

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Shaun McKnight, Systems Engineer

-Primary-

Technical

Supervision
Plans
Baseline
Risk Assessment

System Research
System Functional Requirements
System Architecture
High Level
System Signal Flowchart
Possible Features/Functions
Systems Engineering Plan (SEP)
System Performance Specifications
System Functional Baseline Documentation (Allocated)

-Supplemental-

Proposal Report Document
Testing Events
Bill Of Material (BOM)
PDR/CDR
Case Design and Development

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Justin Owen, Design Engineer

-Primary-

Software Requirements
Software Low Level Architecture
Software Preliminary and Detailed Design
Software Package Information
Coding/ Debugging
Software Testing and Results Documentation

-Supplemental-

Proposal Report Document
Functions
Final Report
System Modifications
Testing and Recording
System Efficiency
Case Design and Development

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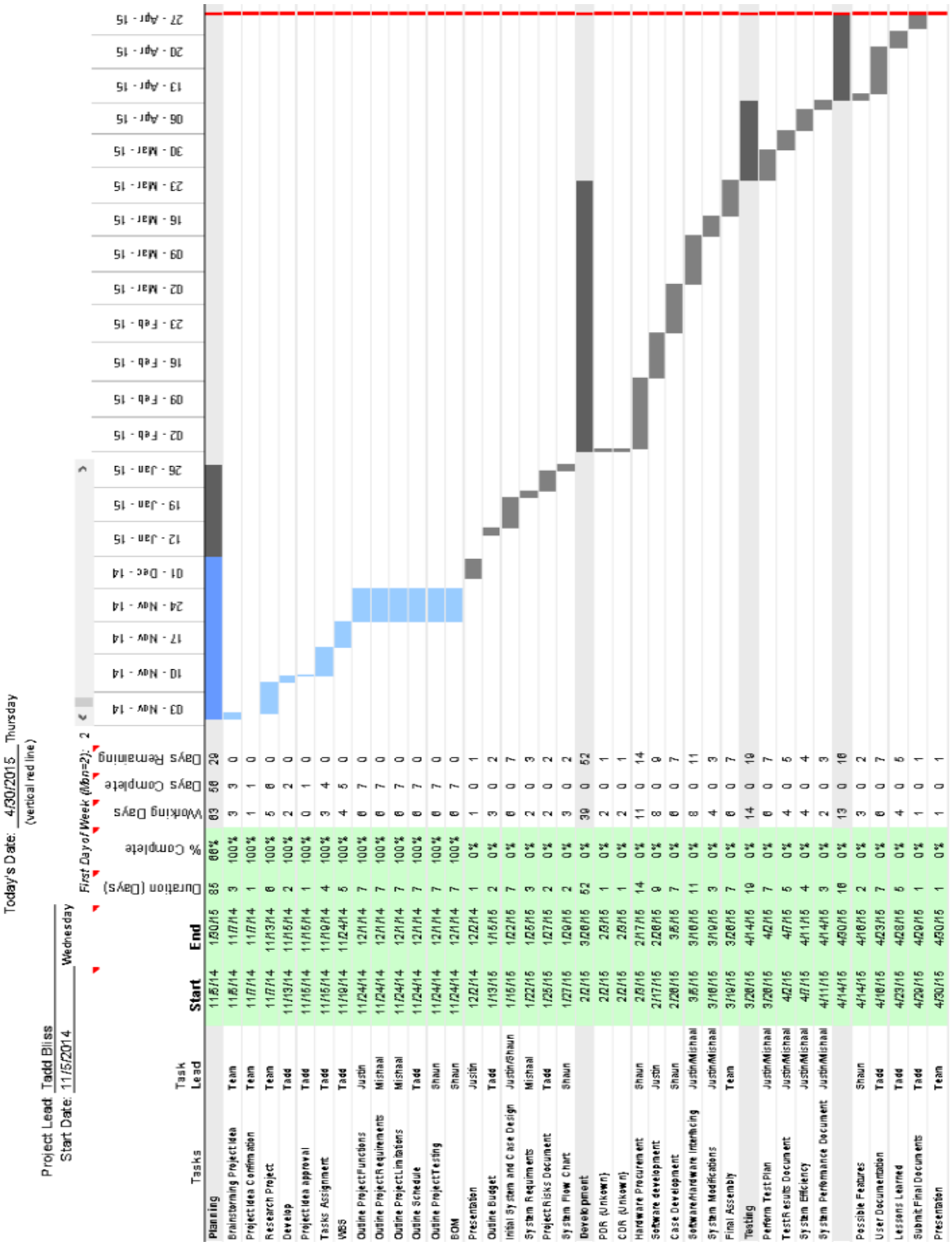
3.3 Gantt Chart:



Tasks	Task Lead	Start	End	Duration (Days)	% Complete	Working Days	Days Complete	Days Remaining
Planning		11/5/14	1/30/15	85	68%	83	58	29
Brainstorming Project Idea	Team	11/5/14	11/7/14	3	100%	3	3	0
Project Idea Confirmation	Team	11/7/14	11/7/14	1	100%	1	1	0
Research Project	Team	11/7/14	11/13/14	6	100%	5	6	0
Develop	Tadd	11/13/14	11/15/14	2	100%	2	2	0
Project Idea approval	Tadd	11/15/14	11/15/14	1	100%	0	1	0
Tasks Assignment	Tadd	11/15/14	11/19/14	4	100%	3	4	0
WBS	Tadd	11/19/14	11/24/14	5	100%	4	5	0
Outline Project Functions	Justin	11/24/14	12/1/14	7	100%	6	7	0
Outline Project Requirements	Mishaal	11/24/14	12/1/14	7	100%	6	7	0
Outline Project Limitations	Mishaal	11/24/14	12/1/14	7	100%	6	7	0
Outline Schedule	Tadd	11/24/14	12/1/14	7	100%	6	7	0
Outline Project Testing	Shaun	11/24/14	12/1/14	7	100%	6	7	0
BOM	Shaun	11/24/14	12/1/14	7	100%	6	7	0
Presentation	Justin	12/2/14	12/2/14	1	0%	1	0	1
Outline Budget	Tadd	1/13/15	1/15/15	2	0%	3	0	2
Initial System and Case Design	Justin/Shaun	1/16/15	1/22/15	7	0%	6	0	7
System Requirments	Mishaal	1/22/15	1/25/15	3	0%	2	0	3
Project Risks Document	Tadd	1/25/15	1/27/15	2	0%	2	0	2
System Flow Chart	Shaun	1/27/15	1/29/15	2	0%	3	0	2
Development		2/2/15	3/26/15	52	0%	30	0	52
PDR (Unkown)		2/2/15	2/3/15	1	0%	2	0	1
CDR (Unkown)		2/2/15	2/3/15	1	0%	2	0	1
Hardware Procurement	Shaun	2/5/15	2/17/15	14	0%	11	0	14
Software development	Justin	2/17/15	2/26/15	9	0%	8	0	9
Case Development	Shaun	2/26/15	3/5/15	7	0%	6	0	7
Software/Hardware Interfacing	Justin/Mishaal	3/5/15	3/16/15	11	0%	8	0	11
System Modifications	Justin/Mishaal	3/16/15	3/19/15	3	0%	4	0	3
Final Assembly	Team	3/19/15	3/26/15	7	0%	6	0	7
Testing		3/26/15	4/14/15	19	0%	14	0	19
Perform Test Plan	Justin/Mishaal	3/26/15	4/2/15	7	0%	6	0	7
Test Results Document	Justin/Mishaal	4/2/15	4/7/15	5	0%	4	0	5
System Efficiency	Justin/Mishaal	4/7/15	4/11/15	4	0%	4	0	4
System Performance Document	Justin/Mishaal	4/11/15	4/14/15	3	0%	2	0	3
		4/14/15	4/30/15	16	0%	13	0	16
Possible Features	Shaun	4/14/15	4/16/15	2	0%	3	0	2
User Documentation	Tadd	4/16/15	4/23/15	7	0%	6	0	7
Lessons Learned	Tadd	4/23/15	4/28/15	5	0%	4	0	5
Submit Final Documents	Tadd	4/29/15	4/29/15	1	0%	1	0	1
Presentation	Team	4/30/15	4/30/15	1	0%	1	0	1

4.0 Reporting:

4.1 Communications:

Precision engineering will convey information of progress to the faculty advisor in the following ways:

- A Milestone matrix to describe the progress of each milestone
- A Program Deviation Report to inform the faculty advisor of unplanned deviation
- Weekly emails of project performance and progress
- Daily emails (as needed) copying the faculty advisor of team communication

4.2 Testing Events:

Figure 55 shows the proper way of testing the LNA circuit for gain and bandwidth measurements. Connect the output of the network analyzer to the inductor FB and the input to the iron core transformer and then vary the gain for the opamp.

Figure 56 shows the proper way of testing the LNA circuit for the frequency response for source impedance matching. Connect the output of the network analyzer to the inductor FB via a 10kΩ potentiometer. Replace the 270Ω resistor with a 10kΩ potentiometer and add a variable capacitor. Tune the variable components and the vary the gain of the output.

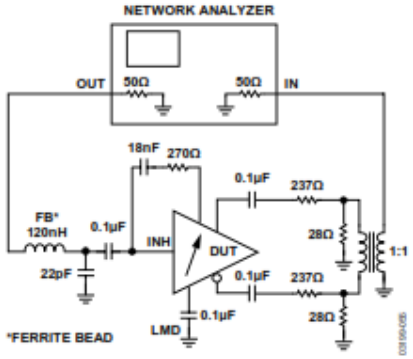


Figure 55. Test Circuit—Gain and Bandwidth Measurements

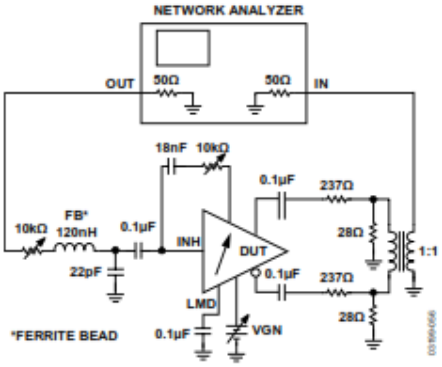
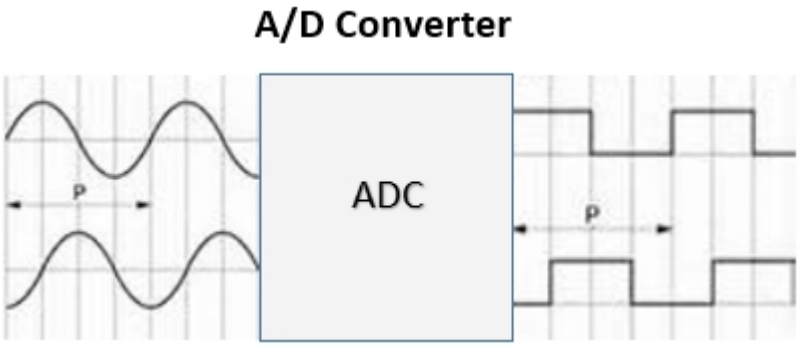
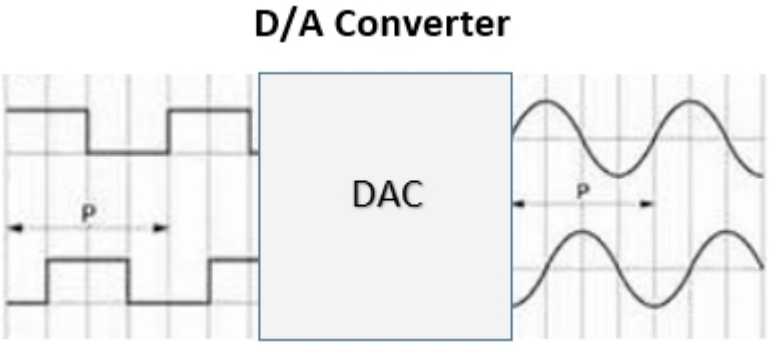


Figure 56. Test Circuit—Frequency Response for Various Matched Source Impedances



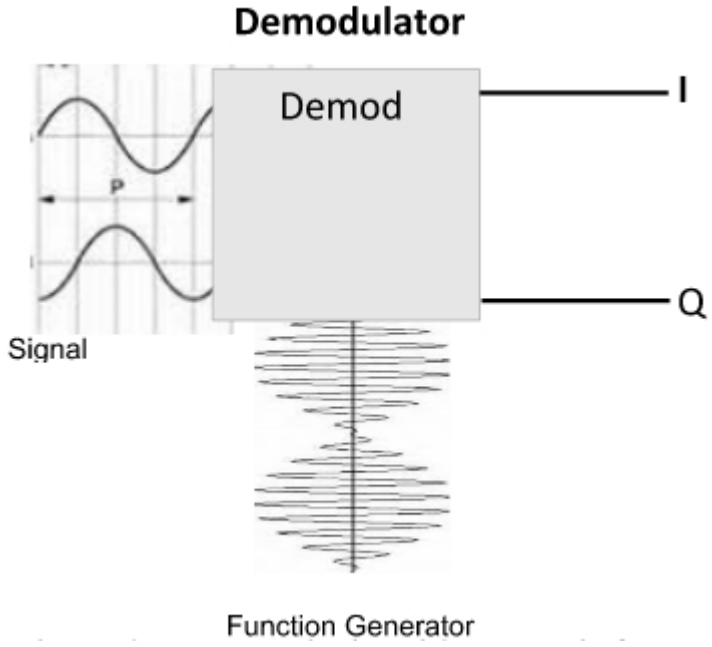
Adjust the ADC until a 90˚ out of phase square wave output has been achieved.



Adjust the DAC until a 90˚ out of phase sine wave output has been achieved.

BASYS2 Field Programmable Gate Array

Perform unit tests for each component.



Connect the function generator and a signal generator to the demodulator. Vary the function generator and look if the I and Q outputs changed accordingly.

4.3 BOM:

Part Description	Part Number	Manufacturer	Vender	Unit price	Quanti ty	Price
Coaxial Connector	CONSMA002-ND	Linx Technologies Inc	Digi-Key Corporation	$3.31	5	$16.55
Dual VGA, Ultralow Noise Pre Amp	AD8332ACPZ-R7	Analog Devices Inc	Digi-Key Corporation	$12.68	1	$12.68
Dual I/Q Demodulator & Phase Shifter	AD8333ACPZ-REEL7	Analog Devices Inc	Digi-Key Corporation	$9.06	1	$9.06
Low Noise, High Speed Amp	AD8021ARMZ	Analog Devices Inc	Digi-Key Corporation	$1.54	2	$3.08
4 channel 12-bit A/D converter	410-217P	Digilent Inc	Digilent Inc	$24.99	1	$24.99
Basys2 Spartan-3E FPGA Board	410-155P-KIT	Digilent Inc	Digilent Inc	$69.00	1	$69.00
Two 12-bit D/A outputs	410-113P	Digilent Inc	Digilent Inc	$28.99	1	$28.99
				Total		$164.35

end of presentation

- _____
  Tadd Bliss, Project Engineer
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  Mishaal Fallatah, Development Engineer
- _____
  Shaun McKnight, System Engineer
- _____
  Justin Owen, Design Engineer

