EE3408C Integrated Analog Design

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1 MOSFET I-V characteristics

1.1 NMOS

S at ground, D at V_{DD}. $V_G \leq V_S$, **cut-off** region. $I_D = 0$.
Otherwise, suppose $V_G > V_S + V_{THN}$
If $V_G \geq V_D + V_{THN}$, in **linear (triode)** region.
If $V_G < V_D + V_{THN}$, in **saturation** region. Constant I_D.
NPN. $V_G > V_S$ to draw electrons upwards to form bridge.

1.2 PMOS

S at V_{DD}, D at ground. $V_G \geq V_S$, **cut-off** region.
Otherwise, suppose $V_G < V_S + V_{THP}$,
If $V_G \leq V_D + V_{THP}$, it is in **linear** region.
If $V_G > V_D + V_{THP}$, it is in **saturation** region.
To convert NMOS formulas to PMOS, substitute V_{GS} by V_{SG}, V_{DS} by V_{SD}, V_{THN} by V_{THP}.

1.3 Current Equations

In Linear region, $I_D = k_n' \frac{W}{L}\left[(V_{GS} - V_{THN})V_{DS} - \frac{1}{2}V_{DS}^2\right]$
$I_D \approx k_n' \frac{W}{L}(V_{GS} - V_{THN})V_{DS}$; $R_{DS} = \frac{1}{k_n'(W/L)(V_{GS} - V_{THN})}$
In Saturation region, $V_{OD} = V_{GS} - V_{THN}$ (at least $200mV$)

$$I_D = \frac{1}{2}k_n' \frac{W}{L}(V_{GS} - V_{THN})^2(1 + \lambda V_{DS}) \quad \lambda \propto \frac{1}{L}$$

1.4 Small-Signal Model

1.4.1 Simplified Model (In saturation)

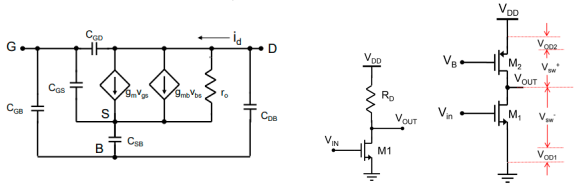
$i_d = g_m v_{gs}$
$g_m = \frac{\partial I_D}{\partial V_{GS}} = k_n' \frac{W}{L}(V_{GS} - V_{TH}) = \sqrt{2k_n' \frac{W}{L} I_D} = \frac{2I_D}{V_{GS} - V_{TH}}$

1.4.2 Output Resistance

Takes into account channel length modulation.
$i_d = g_m v_{gs} + \frac{v_{ds}}{r_o}$, $r_o = \frac{1}{\partial I_D / \partial V_{DS}} = \frac{1}{\lambda I_D}$

1.4.3 Body Effect (bulk, source at diff voltage)

$V_{THN} = V_{TH0} + \gamma\left[\sqrt{|2\Phi_F - V_{BS}|} - \sqrt{|2\Phi_F|}\right]$
$\gamma = \frac{\sqrt{2q\epsilon_{si}N_{sub}}}{C_{ox}}$, $\Phi_F = \pm\frac{kT}{q}\ln\frac{N_{sub}}{n_i}$ (+ NMOS,− PMOS)
$g_{mb} = \frac{\partial I_D}{\partial V_{BS}} = g_m \frac{\gamma}{2\sqrt{|2\Phi_F - V_{BS}|}} = \eta g_m$
$i_d = g_m(v_{gs} + \eta v_{bs}) + \frac{v_{ds}}{r_o}$



2 Common Source Amplifier

- $V_{swing} = 2 \times \min(V_{sw}^+, V_{sw}^-)$
- With resistive load, $A_v = -g_m R_D \quad (R_D \ll r_0)$. $V_{out} = V_{DD} - I_D R_D$, so increasing gain by increasing R_D results in reduced V_{swing}.
- Current source has high AC resistance but low DC resistance. $A_v = -g_{m1}(r_{o1} \parallel r_{o2})$

2.1 Buffer

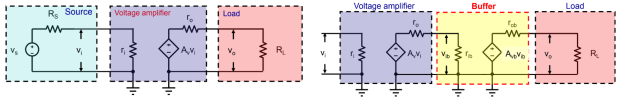
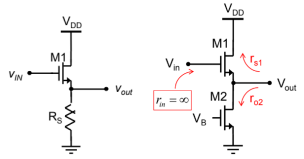


Figure 1: Two port amplifier, with buffer (right)

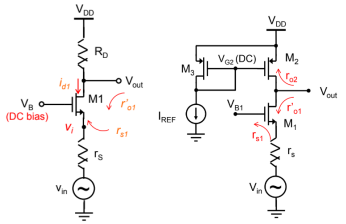
(L) $A_{ov} = \frac{r_i}{r_i + R_S} A_v \frac{R_L}{r_o + R_L}$, so small r_i or R_L reduces gain.
(R) $A_{ov} = A_v \frac{r_{ib}}{r_{ib} + r_o} A_{vb} \frac{R_L}{R_L + r_{ob}}$, ideal buffer has $r_{ib} = \infty$ and $r_{ob} = 0$, source follower has those characteristics.

2.2 Source Follower



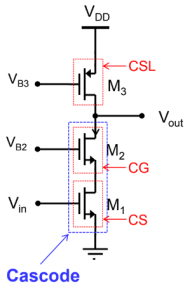
$$A_v = \frac{g_{m1}}{g_{m1} + g_{mb1} + \frac{1}{r_{o1}} + \frac{1}{r_{o2}}} \approx \frac{g_{m1}}{g_{m1} + g_{mb1}} = \frac{1}{1 + \eta}$$
$$r_{out} = (r_{s1} \parallel r_{o2}) = \left(\frac{1}{(1+\eta)g_{m1}} \parallel r_{o2}\right) \approx \frac{1}{(1+\eta)g_{m1}}$$

2.3 Common Gate Amplifier

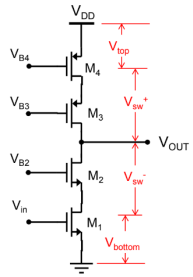


$$A_v \approx (g_{m1} + g_{mb1})(r_{o1} \parallel r_{o2})$$

2.4 Cascode Amplifier

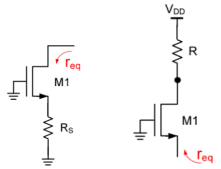


$A_v = -g_{m1} r_{o3}$
about twice the gain of CS amplifier



$A_v = -g_{m1} g_{m3} r_{o4} r_{o3}/2$
$r_{out} = (g_{m2} + g_{mb2}) r_{o1} r_{o2} \parallel g_{m3} r_{o3} r_{o4}$
Max. swing is $V_{DD} - 4V_{OD}$

2.5 Equivalent Resistance Patterns



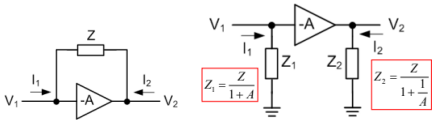
(L) $r_{eq} = [1 + (g_{m1} + g_{mb1})R_s] r_{o1}$
(R) $r_{eq} \approx \frac{1}{g_{m1} + g_{mb1}}$

r_{eq} through a reverse diode connection is $\frac{1}{g_m}$

3 Frequency Response

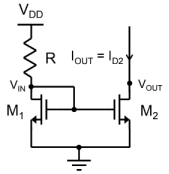
- Poles correspond to capacitors shunting to ground (low-pass filters). Multiply by input impedance, at $f = \frac{1}{2\pi RC}$
- Zeroes correspond to capacitors across inverting amplifiers, creating destructive interference.
- For capacitance along signal path across amplifier with non-zero input resistance, it also behaves as a miller cap, becoming a capacitor shunting to ground at the amplifier input but with a capacitance multiplied by the gain.
- Miller theorem misses a zero by removing the feedforward path

- If lowest pole is separated from other poles by at least 4x, then that pole is the dominant pole, and 3dB frequency can be estimated as that pole
- Associate poles with nodes, zeros with feedforward paths across capacitors, for CS amplifier, poles are $\frac{1}{RC}$, zero is in the right half plane at $\frac{g_m}{C_{GD}}$



4 Current Sources

- Transistor in saturation behaves like a current source
- Simple current source is to use resistor divider to set V_G to put transistor in saturation - not good because PVT (process, voltage, temperature) variation affects V_{GS} and I_D is related to V_{GS}^2



Current Mirror
$\frac{I_{out}}{I_{in}} = \frac{W_2/L_2}{W_1/L_1}$

- Current mirror is less affected by PVT since only depends on single resistor
- Current mirror is like a I-to-V-to-I converter
- $V_{out} \geq V_{GS} - V_{TH} = V_{OD}$ so minimum V_{out} is 1 overdrive voltage
- Gain Error (Systematic Error)

$$E_{rr} = \frac{I_{out} - I_{out,ideal}}{I_{out,ideal}} = \frac{\lambda(V_{out} - V_{in})}{1 + \lambda V_{in}} \approx \lambda(V_{out} - V_{in})$$

- Mismatch Error (Random Error) can be reduced by using same W & L but multiple fingers to "vary" W

4.1 Cascode Current Mirror

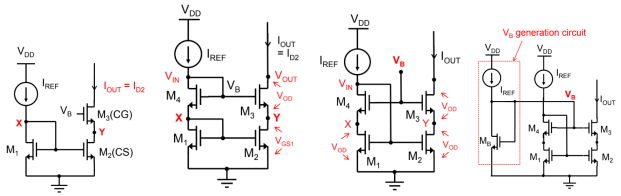


Figure 2: Cascode Current Mirror v1, v2, v3, final

Cascode current mirrors eliminate systematic gain error by matching V_{in} and V_{out}
(1) $r_{out} = (1 + g_{m3}r_{o2})r_{o3}$
(2) $V_{omin} = V_{th} + 2V_{OD}$
(3) $V_{omin} = 2V_{OD}$, $r_{out} \approx g_{m3}r_{o2}r_{o3}$
(4) To generate V_B for (3)

5 Differential Amplifier

- Differential input: $v_{id} = v_{i1} - v_{i2}$
- Differential output: $v_{od} = v_{o2} - v_{o1}$
- Common-mode input: $v_{ic} = (v_{i1} + v_{i2})/2$
- Common-mode output: $v_{oc} = (v_{o2} + v_{o1})/2$

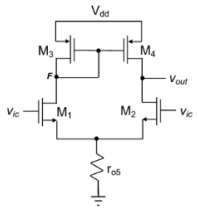
Single-ended gain:
$A_{v1} = -\frac{1}{2}g_{m1}(r_{o1}//R_D)$; $A_{v2} = \frac{1}{2}g_{m2}(r_{o2}//R_D)$
Differential gain: $A_{vd} = g_{m1}(r_{o1}//R_D)$
Maximum differential input voltage is input range such that after amplifying, output range is within the swing.

5.1 Offset Voltage

Output offset voltage is the output when $v_{id} = 0$.
Input offset voltage is the input v_{id} to make output offset voltage equal to 0.

5.2 Common-mode Gain

$A_{cm} = \frac{v_{o2} - v_{o1}}{v_{ic}}$
For single-ended matched current source load,
$A_{cm,s} = \frac{-g_{m2}/g_{m3}}{1+2g_{m2}r_{o5}}$



Common-mode Rejection Ratio (CMRR)

$$CMRR(dB) = 20\log(\frac{A_{vd}}{A_{cm}})$$

6 Operational Amplifiers

Two stage op amp typically for voltage output
Cascode op amp typically for current output because of high output impedance
Two stage op amp is differential pair cascaded with cs amplifier
systematic offset is assuming no difference between differential inputs, then distance of output away from half vdd

7 Frequency Response (2)

Barkhausen Criteria for amplifier instability
Gain condition $|A(\omega)\beta(\omega)| = 1$
Phase condition $\angle A(\omega)\beta(\omega) = -180°$
Gain margin is 0 dB - gain when phase shift is $-180°$
Phase margin is phase when gain is 1 - $(-180°)$

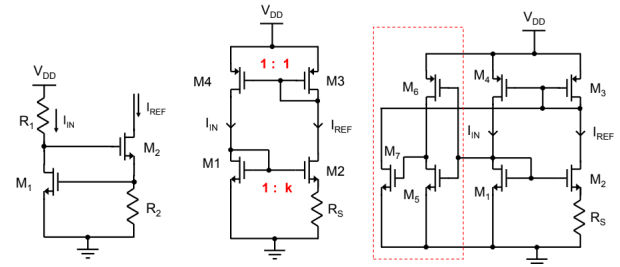
7.1 Compensation Capacitor

Moves the lower pole lower and the high pole higher, by increasing C_{gd5}.
But it also moves the zero closer to the imaginary axis, introducing more lagging phase shift.

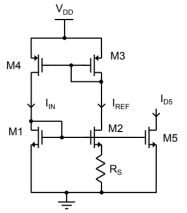
7.2 Lead Compensation

Add resistor R_c and capacitor C_c across amplifying transistor.
Effect is $\omega_z = \frac{1}{C_c(\frac{1}{g_{m5} - R_c})}$, originally $\frac{g_{m5}}{C_{gd5}}$
Choose ω_z slightly higher than ω_u, the unity gain bandwidth, e.g. $1.2\omega_u$
If $R_c > \frac{1}{g_{m5}}$ the zero moves to LHP.

8 Bias Circuits



(L) Threshold referenced $I_{REF} = \frac{V_{THN} + \sqrt{2\frac{I_{IN}}{k'_n}\frac{W_1}{L_1}}}{R_2}$
(C) Self-biasing current source $I_{REF} \approx \frac{2}{k'_n \frac{W_1}{L_1} R_S^2}(1 - \frac{1}{\sqrt{k}})^2$,
$g_{m1} = \sqrt{2k'_n \frac{W_1}{L_1} I_{D1}} = \frac{2}{R_S}(1 - \frac{1}{\sqrt{k}})$ (indp. of V_{DD} and V_{th})
(R) Start up circuit, when current is 0, M_5 is off and M_6 is on. when circuit is started, M_5 is on and M_6 is off



$V_{OD1} = V_{OD5}$
$g_{m5} = \frac{W_5/L_5}{W_1/L_1} g_{m1}$ is constant